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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	25MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f6723-e-pt

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PIC18F8723

NOTES:

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F6628 PIC18LF6628
- PIC18F6723 PIC18LF6723
- PIC18F8628 PIC18LF8628
- PIC18F8723 PIC18LF8723
- **Note:** This data sheet documents only the devices' features and specifications that are in addition to the features and specifications of the PIC18F8722 family devices. For information on the features and specifications shared by the PIC18F8723 family and PIC18F8722 family devices, see the *"PIC18F8722 Family Data Sheet"* (DS39646).

The PIC18F8723 family of devices offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high-endurance, Enhanced Flash program memory. In addition to these features, the PIC18F8723 introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power-sensitive applications.

1.1 Special Features

 12-Bit A/D Converter: The PIC18F8723 family implements a 12-bit A/D Converter. A/D Converters in both families incorporate programmable acquisition time. This allows for a channel to be selected and a conversion to be initiated, without waiting for a sampling period and thus, reducing code overhead.

1.2 Details on Individual Family Members

Devices in the PIC18F8723 family are available in 64-pin and 80-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in the following ways:

- Flash program memory (96 Kbytes for PIC18FX628 devices and 128 Kbytes for PIC18FX723).
- A/D channels (12 for PIC18F6628/6723 devices and 16 for PIC18F8628/8723 devices).
- I/O ports (seven bidirectional ports on PIC18F6628/6723 devices and nine bidirectional ports on PIC18F8628/8723 devices).
- External Memory Bus, configurable for 8 and 16-bit operation

All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1-2 and Table 1-3.

Like all Microchip PIC18 devices, members of the PIC18F8723 family are available as both standard and low-voltage devices. Standard devices with Enhanced Flash memory, designated with an "F" in the part number (such as PIC18F6628), accommodate an operating VDD range of 4.2V to 5.5V. Low-voltage parts, designated by "LF" (such as PIC18LF6628), function over an extended VDD range of 2.0V to 5.5V.







Din Nome	Pin Number	Pin	Buffer	Description
Pin Name	TQFP	Туре	Туре	Description
				PORTA is a bidirectional I/O port.
RA0/AN0 RA0 AN0	24	I/O I	TTL Analog	Digital I/O. Analog input 0.
RA1/AN1 RA1 AN1	23	I/O I	TTL Analog	Digital I/O. Analog input 1.
RA2/AN2/VREF- RA2 AN2 VREF-	22	I/O I I	TTL Analog Analog	Digital I/O. Analog input 2. A/D reference voltage (low) input.
RA3/AN3/VREF+ RA3 AN3 VREF+	21	I/O I I	TTL Analog Analog	Digital I/O. Analog input 3. A/D reference voltage (high) input.
RA4/T0CKI RA4 T0CKI	28	I/O I	ST ST	Digital I/O. Timer0 external clock input.
RA5/AN4/HLVDIN RA5 AN4 HLVDIN	27	I/O I I	TTL Analog Analog	Digital I/O. Analog input 4. High/Low-Voltage Detect input.
RA6				See the OSC2/CLKO/RA6 pin.
RA7				See the OSC1/CLKI/RA7 pin.
Legend:TTL = TTL compatible inputCMOS= CMOS compatible input or outputST = Schmitt Trigger input with CMOS levelsAnalog= Analog inputI = InputO= OutputP = Power $l^2 C^{TM}$ = $l^2 C/SMBus input buffer$				

TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)

Note 1: Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

	Pin Number	Pin	Buffer	- · · ·
Pin Name	TQFP	Туре	Туре	Description
				PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/INT0/FLT0 RB0 INT0 FLT0	48	I/O I I	TTL ST ST	Digital I/O. External interrupt 0. PWM Fault input for ECCPx.
RB1/INT1 RB1 INT1	47	I/O I	TTL ST	Digital I/O. External interrupt 1.
RB2/INT2 RB2 INT2	46	I/O I	TTL ST	Digital I/O. External interrupt 2.
RB3/INT3 RB3 INT3	45	I/O I	TTL ST	Digital I/O. External interrupt 3.
RB4/KBI0 RB4 KBI0	44	I/O I	TTL TTL	Digital I/O. Interrupt-on-change pin.
RB5/KBI1/PGM RB5 KBI1 PGM	43	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. Low-Voltage ICSP™ Programming enable pin.
RB6/KBI2/PGC RB6 KBI2 PGC	42	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming clock pin.
RB7/KBI3/PGD RB7 KBI3 PGD	37	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming data pin.
Legena:I I L = I I L compatible inputCMOS = CMOS compatible input or outputST = Schmitt Trigger input with CMOS levelsAnalog = Analog inputI = Input O = Output				

PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED) **TABLE 1-2:**

Р = Power

= I²C/SMBus input buffer l²C™

Note 1: Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

Din Nome	Pin Number	Pin	Buffer	Description	
Pin Name	TQFP	Туре	Туре	Description	
				PORTD is a bidirectional I/O port.	
RD0/PSP0 RD0 PSP0	58	I/O I/O	ST TTL	Digital I/O. Parallel Slave Port data.	
RD1/PSP1 RD1 PSP1	55	I/O I/O	ST TTL	Digital I/O. Parallel Slave Port data.	
RD2/PSP2 RD2 PSP2	54	I/O I/O	ST TTL	Digital I/O. Parallel Slave Port data.	
RD3/PSP3 RD3 PSP3	53	I/O I/O	ST TTL	Digital I/O. Parallel Slave Port data.	
RD4/PSP4/SDO2 RD4 PSP4 SDO2	52	I/O I/O O	ST TTL	Digital I/O. Parallel Slave Port data. SPI data out.	
RD5/PSP5/SDI2/ SDA2 RD5 PSP5 SDI2 SDA2	51	I/O I/O I I/O	ST TTL ST I ² C/SMB	Digital I/O. Parallel Slave Port data. SPI data in. I ² C™ data I/O.	
RD6/PSP6/SCK2/ SCL2 RD6 PSP6 SCK2 SCL2	50	/0 /0 /0	ST TTL ST I ² C/SMB	Digital I/O. Parallel Slave Port data. Synchronous serial clock input/output for SPI mode. Synchronous serial clock input/output for I ² C mode.	
RD7/PSP7/SS2 RD7 PSP7 SS2	49	I/O I/O I	ST TTL TTL	Digital I/O. Parallel Slave Port data. SPI slave select input.	
Legend:TTL = TTL compatible inputCMOS= CMOS compatible input or outputST = Schmitt Trigger input with CMOS levelsAnalog= Analog inputI = InputO= OutputP = Power l^2C^{TM} = $l^2C/SMBus input buffer$					

TABLE 1-2:	PIC18F6628/6723 ((64-PIN	PINOUT I/O DESCRIPTIONS	(CONTINUED)
		••••••		

Note 1: Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

Din Nome	Pin Number	Pin	Buffer	Description
	TQFP	Туре	Туре	Description
				PORTF is a bidirectional I/O port.
RF0/AN5 RF0 AN5	18	I/O I	ST Analog	Digital I/O. Analog input 5.
RF1/AN6/C2OUT RF1 AN6 C2OUT	17	I/O I O	ST Analog —	Digital I/O. Analog input 6. Comparator 2 output.
RF2/AN7/C1OUT RF2 AN7 C1OUT	16	I/O I O	ST Analog —	Digital I/O. Analog input 7. Comparator 1 output.
RF3/AN8 RF3 AN8	15	I/O I	ST Analog	Digital I/O. Analog input 8.
RF4/AN9 RF4 AN9	14	I/O I	ST Analog	Digital I/O. Analog input 9.
RF5/AN10/CVREF RF5 AN10 CVREF	13	I/O I O	ST Analog Analog	Digital I/O. Analog input 10. Comparator reference voltage output.
RF6/AN11 RF6 AN11	12	I/O I	ST Analog	Digital I/O. Analog input 11.
RF7/SS1 <u>RF7</u> SS1	11	I/O I	ST TTL	Digital I/O. SPI slave select input.
Legend:TTL = TTL compatible inputCMOS= CMOS compatible input or outputST = Schmitt Trigger input with CMOS levelsAnalog= Analog inputI= InputO= OutputP= Power I^2C^{TM} = $I^2C/SMBus input buffer$				

TABLE 1-2:	PIC18F6628/6723 (64-PIN) PINOUT I/O DESCR	(CONTINUED)

Note 1: Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

Din Nome	Pin Number	Pin	Buffer	Description
	TQFP	Туре	Туре	Description
RG5/MCLR/Vpp	9			Master Clear (input) or programming voltage (input).
RG5		I	ST	Digital input.
MCLR		I	ST	Master Clear (Reset) input. This pin is an active-low
Vpp		Р		Programming voltage input.
OSC1/CLKI/RA7	49			Oscillator crystal or external clock input.
OSC1		I	ST	Oscillator crystal input or external clock source input.
				ST buffer when configured in RC mode, CMOS
				otherwise.
CLKI		I	CMOS	External clock source input. Always associated with
				pin function OSC1. (See related OSC1/CLKI,
D 4 7				OSC2/CLKO pins.)
RA/		1/0	IIL	General purpose I/O pin.
OSC2/CLKO/RA6	50			Oscillator crystal or clock output.
OSC2		0	—	Oscillator crystal output. Connects to crystal or
0.140				resonator in Crystal Oscillator mode.
CLKO		0	—	In RC mode, OSC2 pin outputs CLKO, which has 1/4 the
				frequency of OSC1 and denotes the
DAG		1/0	тті	Instruction cycle rate.
RAO		1/0	IIL	General purpose 1/O pin.
Legend: TTL = TTL o	compatible inpu	t		CMOS = CMOS compatible input or output
SI = Schr	ntt Trigger inpu	t with CI	VIOS leve	is Analog = Analog input
I = Input				O = Output
P = Powe	er			I ⁺ C [™] /SMB = I ⁺ C/SMBus input buffer

TABLE 1-3:	PIC18F8628/8723 (80-PIN)	PINOUT I/O	DESCRIPTIONS
_				

Note 1: Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).

2: Default assignment for ECCP2 in all operating modes (CCP2MX is set).

3: Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

4: Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

5: Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

Din Nome	Pin Number	Pin	Buffer	Description
	TQFP	Туре	Туре	Description
				PORTG is a bidirectional I/O port.
RG0/ECCP3/P3A RG0 ECCP3	5	1/0 1/0	ST ST	Digital I/O. Enhanced Capture 3 input/Compare 3 output/ PWM3 output.
P3A		0	—	ECCP3 PWM output A.
RG1/TX2/CK2 RG1 TX2 CK2	6	I/O O I/O	ST — ST	Digital I/O. EUSART2 asynchronous transmit. EUSART2 synchronous clock (see related RX2/DT2).
RG2/RX2/DT2 RG2 RX2 DT2	7	I/O I I/O	ST ST ST	Digital I/O. EUSART2 asynchronous receive. EUSART2 synchronous data (see related TX2/CK2).
RG3/CCP4/P3D RG3 CCP4 P3D	8	I/O I/O O	ST ST	Digital I/O. Capture 4 input/Compare 4 output/PWM4 output. ECCP3 PWM output D.
RG4/CCP5/P1D RG4 CCP5 P1D	10	I/O I/O O	ST ST	Digital I/O. Capture 5 input/Compare 5 output/PWM5 output. ECCP1 PWM output D.
RG5				See RG5/MCLR/VPP pin.
Legend: TTL = TTL o ST = Schn I = Input P = Powe	compatible inpu nitt Trigger inpu er	the constraint of the constra		
Note 1: Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).				

TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)

2: Default assignment for ECCP2 in all operating modes (CCP2MX is set).

3: Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

4: Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

5: Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

Din Nome	Pin Number	Pin	Buffer	Description
Pin Name	TQFP	Туре	Туре	Description
				PORTH is a bidirectional I/O port.
RH0/A16	79			
RH0 A16		1/0 1/0	ST TTL	Digital I/O. External memory address/data 16.
RH1/A17	80			
RH1 A17		1/O 1/O	TTL	Digital I/O. External memory address/data 17.
RH2/A18	1			
RH2 A18		1/0 1/0	ST TTL	Digital I/O. External memory address/data 18.
RH3/A19	2			
RH3 A19		1/O 1/O	ST TTL	Digital I/O. External memory address/data 19.
RH4/AN12/P3C	22			
RH4 AN12		1/O	ST Analog	Digital I/O. Analog input 12
P3C ⁽⁵⁾		0		ECCP3 PWM output C.
RH5/AN13/P3B	21			
RH5 AN13		1/O	SI	Digital I/O. Apalog input 13
P3B ⁽⁵⁾		0		ECCP3 PWM output B.
RH6/AN14/P1C	20			
RH6		1/0	ST	Digital I/O.
P1C ⁽⁵⁾		0	Analog	ECCP1 PWM output C.
RH7/AN15/P1B	19			
RH7		I/O	ST	Digital I/O.
AN15 P1B (5)			Analog	Analog input 15. ECCP1 PWM output B
Legend: TTI = TTI	L compatible inpu	<u> </u>	I	CMOS = CMOS compatible input or output
ST = Schn	nitt Trigger inpu	t with Cl	MOS level	ls Analog = Analog input
I = Input O = Output				O = Output
P = Powe	er			I [∠] C [™] /SMB = I [∠] C/SMBus input buffer

TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)

Note 1: Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).

2: Default assignment for ECCP2 in all operating modes (CCP2MX is set).

3: Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

4: Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

5: Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

The analog reference voltage is software selectable to either the device's positive and negative supply voltage (VDD and Vss), or the voltage level on the RA3/AN3/ VREF+ and RA2/AN2/VREF-/CVREF pins.

The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the converter, which generates the result via successive approximation.



A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D Converter can be configured as an analog input or a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/DONE bit (ADCON0<1>) is cleared and the A/D Interrupt Flag bit, ADIF, is set. The block diagram of the A/D module is shown in Figure 2-1.



2.2 Selecting and Configuring Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set. It also gives users the option to use an automatically determined acquisition time.

Acquisition time may be set with the ACQT2:ACQT0 bits (ADCON2<5:3>), which provide a range of 2 to 20 TAD. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

Manual acquisition is selected when ACQT2:ACQT0 = 000. When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This option is also the default Reset state of the ACQT2:ACQT0 bits and is compatible with devices that do not offer programmable acquisition times.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

2.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 13 TAD per 12-bit conversion. The source of the A/D conversion clock is software selectable. There are seven possible options for TAD:

- 2 Tosc
- 4 Tosc
- 8 Tosc
- 16 Tosc
- 32 Tosc
- 64 Tosc
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible, but greater than the minimum TAD (see parameter 130 for more information).

Table 2-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

TABLE 2-1: TAD VS. DEVICE OPERATING FREQUENCIES

A/D Clock S	Assumes TAD Min. = 0.8 μ s	
Operation	ADCS2:ADCS0	Maximum Fosc
2 Tosc	000	2.50 MHz
4 Tosc	100	5.00 MHz
8 Tosc	001	10.00 MHz
16 Tosc	101	20.00 MHz
32 Tosc	010	40.00 MHz
64 Tosc	110	40.00 MHz
RC ⁽¹⁾	x11	1.00 MHz ⁽²⁾

Note 1: The RC source has a typical TAD time of 2.5 μ s.

2: For device frequencies above 1 MHz, the device must be in Sleep for the entire conversion or a Fosc divider should be used instead; otherwise, the A/D accuracy specification may not be met.

2.6 A/D Conversions

Figure 2-4 shows the operation of the A/D Converter after the GO/DONE bit has been set and the ACQT2:ACQT0 bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

Figure 2-5 shows the operation of the A/D Converter after the GO/DONE bit has been set, the ACQT2:ACQT0 bits are set to '010' and a 4 TAD acquisition time has been selected before the conversion starts.

Clearing the GO/DONE bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. This means the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers). After the A/D conversion is completed or aborted, a 2 TcY wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

Note:	The GO/DONE bit should NOT be set in
	the same instruction that turns on the A/D.
	Code should wait at least 2 µs after
	enabling the A/D before beginning an
	acquisition and conversion cycle.

2.7 Discharge

The discharge phase is used to initialize the value of the holding capacitor. The array is discharged before every sample. This feature helps to optimize the unity gain amplifier, as the circuit always needs to charge the capacitor array, rather than charge/discharge based on previous measure values.

FIGURE 2-4: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 000, TACQ = 0)



FIGURE 2-5: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 010, TACQ = 4 TAD)



2.8 Use of the ECCP2 Trigger

An A/D conversion can be started by the Special Event Trigger of the ECCP2 module. This requires that the CCP2M3:CCP2M0 bits (CCP2CON<3:0>) be programmed as '1011' and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/DONE bit will be set, starting the A/D acquisition and conversion, and the Timer1 (or Timer3) counter will be reset to zero. Timer1 (or Timer3) is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving ADRESH:ADRESL to the desired location). The appropriate analog input channel must be selected and the minimum acquisition period is either timed by the user, or an appropriate TACQ time selected before the Special Event Trigger sets the GO/DONE bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the Special Event Trigger will be ignored by the A/D module but will still reset the Timer1 (or Timer3) counter.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	0IF INTOIF RBIF		(3)
PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	CCP1IF TMR2IF T		(3)
PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	(3)
IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP	(3)
PIR2	OSCFIF	CMIF	_	EEIF	BCL1IF	HLVDIF	TMR3IF	CCP2IF	(3)
PIE2	OSCFIE	CMIE	_	EEIE	BCL1IE	HLVDIE	TMR3IE	CCP2IE	(3)
IPR2	OSCFIP	CMIP	_	EEIP	BCL1IP	HLVDIP	TMR3IP	CCP2IP	(3)
ADRESH	A/D Result Register High Byte							(3)	
ADRESL	A/D Result Register Low Byte						(3)		
ADCON0	_	_	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	(3)
ADCON1	_	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	(3)
ADCON2	ADFM	_	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	(3)
TRISA	TRISA7 ⁽¹⁾	TRISA6 ⁽¹⁾	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	(3)
TRISF	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	(3)
TRISH ⁽²⁾	TRISH7	TRISH6	TRISH5	TRISH4	TRISH3	TRISH2	TRISH1	TRISH0	(3)

 TABLE 2-2:
 REGISTERS ASSOCIATED WITH A/D OPERATION

Legend: — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

Note 1: PORTA<7:6> and their direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

2: These registers are not implemented on PIC18F6628/6723 devices.

3: For these Reset values, see the "PIC18F8722 Family Data Sheet" (DS39646).

4.0 ELECTRICAL CHARACTERISTICS

Note: Other than some basic data, this section documents only the PIC18F8723 family's specifications that differ from those of the PIC18F8722 family devices. For detailed information on the electrical specifications shared by the PIC18F8723 family and PIC18F8722 family devices, see the "PIC18F8722 Family Data Sheet" (DS39646).

Absolute Maximum Ratings^(†)

Ambient temperature under bias	40°C to +125°C
Storage temperature	65°C to +150°C
Voltage on any pin with respect to Vss (except VDD and MCLR)	0.3V to (VDD + 0.3V)
Voltage on VDD with respect to Vss	-0.3V to +7.5V
Voltage on MCLR with respect to Vss (Note 2)	0V to +13.25V
Total power dissipation (Note 1)	
Maximum current out of Vss pin	
Maximum current into VDD pin	
Input clamp current, lik (VI < 0 or VI > VDD)	±20 mA
Output clamp current, Iok (Vo < 0 or Vo > VDD)	±20 mA
Maximum output current sunk by any I/O pin	
Maximum output current sourced by any I/O pin	
Maximum current sunk by all ports	
Maximum current sourced by all ports	

- Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD $-\sum$ IOH} + \sum {(VDD - VOH) x IOH} + \sum (VOL x IOL)
 - 2: Voltage spikes below Vss at the RG5/MCLR/VPP pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the RG5/MCLR/ VPP pin, rather than pulling this pin directly to Vss.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



FIGURE 4-2: PIC18F8723 FAMILY VOLTAGE-FREQUENCY GRAPH (EXTENDED)



NOTES:

PIC18F8723 FAMILY PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART N	<u>io. x /xx xxx</u>	Ex	amples:			
Devic	e Temperature Package Pattern Range	a)	 a) PIC18LF6723-I/PT 301 = Industrial temp., TQFP package, Extended VDD limits, QTP pattern #301. 			
Device ^{(1) (2)}	PIC18F6628/6723, PIC18F8628/8723, VDD range 4.2V to 5.5V PIC18LF6628/6723, PIC18LF6628/6723 ⁽ VDD range 2.0V to 5.5V	b)	PIC18F6723-E/PT = Extended temp., TQFP package, standard VDD limits.			
Temperature Range	$I = -40^{\circ}C \text{ to } +85^{\circ}C \text{ (Industrial)}$ $E = -40^{\circ}C \text{ to } +125^{\circ}C \text{ (Extended)}$					
Package	PT = TQFP (Thin Quad Flatpack)					
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)	No	te 1: F = Standard Voltage Range LF = Wide Voltage Range 2: T = in tape and reel TQFP packages only.			