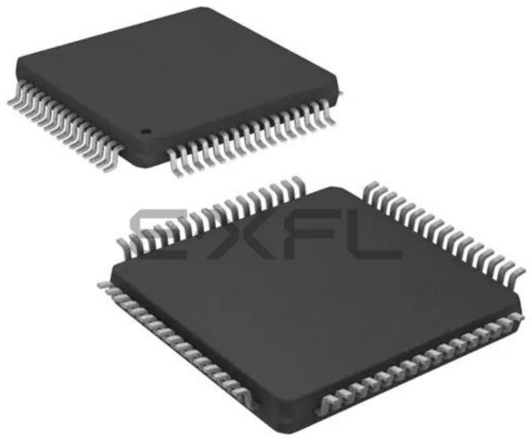

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 40MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, HLVD, POR, PWM, WDT |
| Number of I/O | 54 |
| Program Memory Size | 128KB (64K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 3.8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.2V ~ 5.5V |
| Data Converters | A/D 12x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-TQFP |
| Supplier Device Package | 64-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic18f6723-i-pt |

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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MICROCHIP

# PIC18F8723 FAMILY

## 64/80-Pin, 1-Mbit, Enhanced Flash Microcontrollers with 12-Bit A/D and nanoWatt Technology

### Peripheral Highlights:

- 12-Bit, Up to 16-Channel Analog-to-Digital Converter module (A/D):
  - Auto-acquisition capability
  - Conversion available during Sleep
- Two Master Synchronous Serial Port (MSSP) modules supporting 2/3/4-Wire SPI (all four modes) and $I^2C$™ Master and Slave modes
- Two Capture/Compare/PWM (CCP) modules
- Three Enhanced Capture/Compare/PWM (ECCP) modules:
  - One, two or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart
- Two Enhanced Addressable USART modules:
  - Supports RS-485, RS-232 and LIN 1.2
  - Auto-wake-up on Start bit
  - Auto-Baud Detect
- Dual Analog Comparators with Input Multiplexing
- High-Current Sink/Source 25 mA/25 mA
- Four Programmable External Interrupts
- Four Input Change Interrupts

### External Memory Interface:

- Address Capability of Up to 2 Mbytes
- 8-Bit or 16-Bit Interface
- 8, 12, 16 and 20-Bit Address modes

### Power-Managed Modes:

- Run: CPU on, Peripherals on
- Idle: CPU off, Peripherals on
- Sleep: CPU off, Peripherals off
- Idle mode Currents Down to 15 μA Typical
- Sleep Current Down to 0.2 μA Typical
- Timer1 Oscillator: 1.8 μA, 32 kHz, 2V
- Watchdog Timer: 2.1 μA

### Special Microcontroller Features:

- C Compiler Optimized Architecture:
  - Optional extended instruction set designed to optimize re-entrant code
- 100,000 Erase/Write Cycle Enhanced Flash Program Memory Typical
- 1,000,000 Erase/Write Cycle Data EEPROM Memory Typical
- Flash/Data EEPROM Retention: 100 Years Typical
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 131s
- Single-Supply In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Wide Operating Voltage Range: 2.0V to 5.5V
- Fail-Safe Clock Monitor
- Two-Speed Oscillator Start-up
- nanoWatt Technology

| **Note:** | This document is supplemented by the *"PIC18F8722 Family Data Sheet"* (DS39646). See **Section 1.0 "Device Overview"**. |
|---|---|

| Device | Program Memory | | Data Memory | | I/O | 12-Bit A/D (ch) | CCP/ ECCP (PWM) | MSSP | | | EUSART | Comparators | Timers 8/16-Bit | External Bus |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Flash (bytes) | # Single-Word Instructions | SRAM (bytes) | EEPROM (bytes) | | | | | SPI | Master $I^2C$™ | | | | |
| PIC18F6628 | 96K | 49152 | 3936 | 1024 | 54 | 12 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | N |
| PIC18F6723 | 128K | 65536 | 3936 | 1024 | 54 | 12 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | N |
| PIC18F8628 | 96K | 49152 | 3936 | 1024 | 70 | 16 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | Y |
| PIC18F8723 | 128K | 65536 | 3936 | 1024 | 70 | 16 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | Y |

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An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

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## 1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F6628
- PIC18F6723
- PIC18F8628
- PIC18F8723
- PIC18LF6628
- PIC18LF6723
- PIC18LF8628
- PIC18LF8723

| **Note:** | This data sheet documents only the devices' features and specifications that are in addition to the features and specifications of the PIC18F8722 family devices. For information on the features and specifications shared by the PIC18F8723 family and PIC18F8722 family devices, see the *"PIC18F8722 Family Data Sheet"* (DS39646). |
|---|---|

The PIC18F8723 family of devices offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high-endurance, Enhanced Flash program memory. In addition to these features, the PIC18F8723 introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power-sensitive applications.

### 1.1 Special Features

- **12-Bit A/D Converter:** The PIC18F8723 family implements a 12-bit A/D Converter. A/D Converters in both families incorporate programmable acquisition time. This allows for a channel to be selected and a conversion to be initiated, without waiting for a sampling period and thus, reducing code overhead.

### 1.2 Details on Individual Family Members

Devices in the PIC18F8723 family are available in 64-pin and 80-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in the following ways:

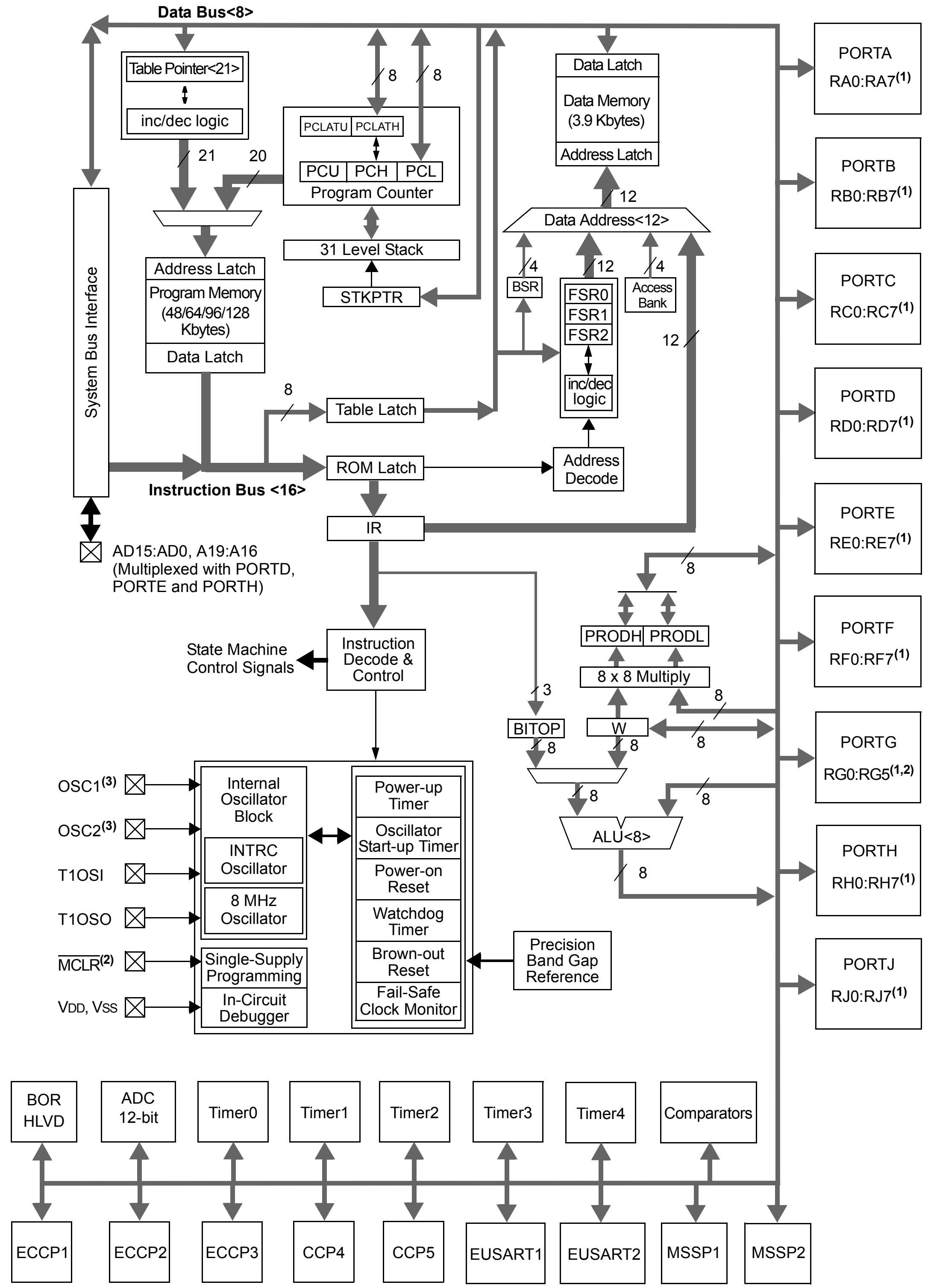
- Flash program memory (96 Kbytes for PIC18FX628 devices and 128 Kbytes for PIC18FX723).
- A/D channels (12 for PIC18F6628/6723 devices and 16 for PIC18F8628/8723 devices).
- I/O ports (seven bidirectional ports on PIC18F6628/6723 devices and nine bidirectional ports on PIC18F8628/8723 devices).
- External Memory Bus, configurable for 8 and 16-bit operation

All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1-2 and Table 1-3.

Like all Microchip PIC18 devices, members of the PIC18F8723 family are available as both standard and low-voltage devices. Standard devices with Enhanced Flash memory, designated with an "F" in the part number (such as PIC18**F**6628), accommodate an operating $V_{DD}$ range of 4.2V to 5.5V. Low-voltage parts, designated by "LF" (such as PIC18**LF**6628), function over an extended $V_{DD}$ range of 2.0V to 5.5V.

**FIGURE 1-2: PIC18F8628/8723 (80-PIN) BLOCK DIAGRAM**




**Note 1:** See Table 1-3 for I/O port pin descriptions.

**2:** RG5 is only available when $\overline{\text{MCLR}}$ functionality is disabled.

**3:** OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, refer to **Section 2.0 "Oscillator Configurations"** of the *"PIC18F8722 Family Data Sheet"* (DS39646).

**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number TQFP | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | | | | PORTA is a bidirectional I/O port. |
| RA0/AN0 | 24 | | | |
| RA0 | | I/O | TTL | Digital I/O. |
| AN0 | | I | Analog | Analog input 0. |
| RA1/AN1 | 23 | | | |
| RA1 | | I/O | TTL | Digital I/O. |
| AN1 | | I | Analog | Analog input 1. |
| RA2/AN2/VREF- | 22 | | | |
| RA2 | | I/O | TTL | Digital I/O. |
| AN2 | | I | Analog | Analog input 2. |
| VREF- | | I | Analog | A/D reference voltage (low) input. |
| RA3/AN3/VREF+ | 21 | | | |
| RA3 | | I/O | TTL | Digital I/O. |
| AN3 | | I | Analog | Analog input 3. |
| VREF+ | | I | Analog | A/D reference voltage (high) input. |
| RA4/T0CKI | 28 | | | |
| RA4 | | I/O | ST | Digital I/O. |
| T0CKI | | I | ST | Timer0 external clock input. |
| RA5/AN4/HLVDIN | 27 | | | |
| RA5 | | I/O | TTL | Digital I/O. |
| AN4 | | I | Analog | Analog input 4. |
| HLVDIN | | I | Analog | High/Low-Voltage Detect input. |
| RA6 | | | | See the OSC2/CLKO/RA6 pin. |
| RA7 | | | | See the OSC1/CLKI/RA7 pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels; Analog = Analog input
I = Input; O = Output
P = Power; $I^2C$™ = $I^2C$/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.
**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number TQFP | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | | | | PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs. |
| RB0/INT0/FLT0 | 48 | | | |
| RB0 | | I/O | TTL | Digital I/O. |
| INT0 | | I | ST | External interrupt 0. |
| FLT0 | | I | ST | PWM Fault input for ECCPx. |
| RB1/INT1 | 47 | | | |
| RB1 | | I/O | TTL | Digital I/O. |
| INT1 | | I | ST | External interrupt 1. |
| RB2/INT2 | 46 | | | |
| RB2 | | I/O | TTL | Digital I/O. |
| INT2 | | I | ST | External interrupt 2. |
| RB3/INT3 | 45 | | | |
| RB3 | | I/O | TTL | Digital I/O. |
| INT3 | | I | ST | External interrupt 3. |
| RB4/KBI0 | 44 | | | |
| RB4 | | I/O | TTL | Digital I/O. |
| KBI0 | | I | TTL | Interrupt-on-change pin. |
| RB5/KBI1/PGM | 43 | | | |
| RB5 | | I/O | TTL | Digital I/O. |
| KBI1 | | I | TTL | Interrupt-on-change pin. |
| PGM | | I/O | ST | Low-Voltage ICSP™ Programming enable pin. |
| RB6/KBI2/PGC | 42 | | | |
| RB6 | | I/O | TTL | Digital I/O. |
| KBI2 | | I | TTL | Interrupt-on-change pin. |
| PGC | | I/O | ST | In-Circuit Debugger and ICSP programming clock pin. |
| RB7/KBI3/PGD | 37 | | | |
| RB7 | | I/O | TTL | Digital I/O. |
| KBI3 | | I | TTL | Interrupt-on-change pin. |
| PGD | | I/O | ST | In-Circuit Debugger and ICSP programming data pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™ = $I^2C$/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number TQFP | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | | | | PORTF is a bidirectional I/O port. |
| RF0/AN5 | 18 | | | |
| RF0 | | I/O | ST | Digital I/O. |
| AN5 | | I | Analog | Analog input 5. |
| RF1/AN6/C2OUT | 17 | | | |
| RF1 | | I/O | ST | Digital I/O. |
| AN6 | | I | Analog | Analog input 6. |
| C2OUT | | O | — | Comparator 2 output. |
| RF2/AN7/C1OUT | 16 | | | |
| RF2 | | I/O | ST | Digital I/O. |
| AN7 | | I | Analog | Analog input 7. |
| C1OUT | | O | — | Comparator 1 output. |
| RF3/AN8 | 15 | | | |
| RF3 | | I/O | ST | Digital I/O. |
| AN8 | | I | Analog | Analog input 8. |
| RF4/AN9 | 14 | | | |
| RF4 | | I/O | ST | Digital I/O. |
| AN9 | | I | Analog | Analog input 9. |
| RF5/AN10/CVREF | 13 | | | |
| RF5 | | I/O | ST | Digital I/O. |
| AN10 | | I | Analog | Analog input 10. |
| CVREF | | O | Analog | Comparator reference voltage output. |
| RF6/AN11 | 12 | | | |
| RF6 | | I/O | ST | Digital I/O. |
| AN11 | | I | Analog | Analog input 11. |
| RF7/$\overline{SS1}$ | 11 | | | |
| RF7 | | I/O | ST | Digital I/O. |
| $\overline{SS1}$ | | I | TTL | SPI slave select input. |

**Legend:** TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I = Input; P = Power; CMOS = CMOS compatible input or output; Analog = Analog input; O = Output; $I^2C$™ = $I^2C$/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number TQFP | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | | | | PORTD is a bidirectional I/O port. |
| RD0/AD0/PSP0 | 72 | | | |
| RD0 | | I/O | ST | Digital I/O. |
| AD0 | | I/O | TTL | External memory address/data 0. |
| PSP0 | | I/O | TTL | Parallel Slave Port data. |
| RD1/AD1/PSP1 | 69 | | | |
| RD1 | | I/O | ST | Digital I/O. |
| AD1 | | I/O | TTL | External memory address/data 1. |
| PSP1 | | I/O | TTL | Parallel Slave Port data. |
| RD2/AD2/PSP2 | 68 | | | |
| RD2 | | I/O | ST | Digital I/O. |
| AD2 | | I/O | TTL | External memory address/data 2. |
| PSP2 | | I/O | TTL | Parallel Slave Port data. |
| RD3/AD3/PSP3 | 67 | | | |
| RD3 | | I/O | ST | Digital I/O. |
| AD3 | | I/O | TTL | External memory address/data 3. |
| PSP3 | | I/O | TTL | Parallel Slave Port data. |
| RD4/AD4/PSP4/SDO2 | 66 | | | |
| RD4 | | I/O | ST | Digital I/O. |
| AD4 | | I/O | TTL | External memory address/data 4. |
| PSP4 | | I/O | TTL | Parallel Slave Port data. |
| SDO2 | | O | — | SPI data out. |
| RD5/AD5/PSP5/SDI2/SDA2 | 65 | | | |
| RD5 | | I/O | ST | Digital I/O. |
| AD5 | | I/O | TTL | External memory address/data 5. |
| PSP5 | | I/O | TTL | Parallel Slave Port data. |
| SDI2 | | I | ST | SPI data in. |
| SDA2 | | I/O | I²C/SMB | I²C™ data I/O. |
| RD6/AD6/PSP6/SCK2/SCL2 | 64 | | | |
| RD6 | | I/O | ST | Digital I/O. |
| AD6 | | I/O | TTL | External memory address/data 6. |
| PSP6 | | I/O | TTL | Parallel Slave Port data. |
| SCK2 | | I/O | ST | Synchronous serial clock input/output for SPI mode. |
| SCL2 | | I/O | I²C/SMB | Synchronous serial clock input/output for I²C mode. |
| RD7/AD7/PSP7/$\overline{SS2}$ | 63 | | | |
| RD7 | | I/O | ST | Digital I/O. |
| AD7 | | I/O | TTL | External memory address/data 7. |
| PSP7 | | I/O | TTL | Parallel Slave Port data. |
| $\overline{SS2}$ | | I | TTL | SPI slave select input. |

**Legend:**
TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
I²C™/SMB = I²C/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).
**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).
**3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).
**4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).
**5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number TQFP | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | | | | PORTH is a bidirectional I/O port. |
| RH0/A16 | 79 | | | |
| RH0 | | I/O | ST | Digital I/O. |
| A16 | | I/O | TTL | External memory address/data 16. |
| RH1/A17 | 80 | | | |
| RH1 | | I/O | ST | Digital I/O. |
| A17 | | I/O | TTL | External memory address/data 17. |
| RH2/A18 | 1 | | | |
| RH2 | | I/O | ST | Digital I/O. |
| A18 | | I/O | TTL | External memory address/data 18. |
| RH3/A19 | 2 | | | |
| RH3 | | I/O | ST | Digital I/O. |
| A19 | | I/O | TTL | External memory address/data 19. |
| RH4/AN12/P3C | 22 | | | |
| RH4 | | I/O | ST | Digital I/O. |
| AN12 | | I | Analog | Analog input 12. |
| P3C(5) | | O | — | ECCP3 PWM output C. |
| RH5/AN13/P3B | 21 | | | |
| RH5 | | I/O | ST | Digital I/O. |
| AN13 | | I | Analog | Analog input 13. |
| P3B(5) | | O | — | ECCP3 PWM output B. |
| RH6/AN14/P1C | 20 | | | |
| RH6 | | I/O | ST | Digital I/O. |
| AN14 | | I | Analog | Analog input 14. |
| P1C(5) | | O | — | ECCP1 PWM output C. |
| RH7/AN15/P1B | 19 | | | |
| RH7 | | I/O | ST | Digital I/O. |
| AN15 | | I | Analog | Analog input 15. |
| P1B(5) | | O | — | ECCP1 PWM output B. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™/SMB = $I^2C$/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).

**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).

**3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

**4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

**5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

**REGISTER 2-2: ADCON1: A/D CONTROL REGISTER 1**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | VCFG1 | VCFG0 | PCFG3 | PCFG2 | PCFG1 | PCFG0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **VCFG1:VCFG0:** Voltage Reference Configuration bits

| | A/D VREF+ | A/D VREF- |
|---|---|---|
| 00 | AVDD | AVSS |
| 01 | External VREF+ | AVSS |
| 10 | AVDD | External VREF- |
| 11 | External VREF+ | External VREF- |

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits:

| PCFG<3:0> | AN15[1] | AN14[1] | AN13[1] | AN12[1] | AN11 | AN10 | AN9 | AN8 | AN7 | AN6 | AN5 | AN4 | AN3 | AN2 | AN1 | AN0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0000 | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| 0001 | D | D | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| 0010 | D | D | D | A | A | A | A | A | A | A | A | A | A | A | A | A |
| 0011 | D | D | D | D | A | A | A | A | A | A | A | A | A | A | A | A |
| 0100 | D | D | D | D | D | A | A | A | A | A | A | A | A | A | A | A |
| 0101 | D | D | D | D | D | D | A | A | A | A | A | A | A | A | A | A |
| 0110 | D | D | D | D | D | D | D | A | A | A | A | A | A | A | A | A |
| 0111 | D | D | D | D | D | D | D | D | A | A | A | A | A | A | A | A |
| 1000 | D | D | D | D | D | D | D | D | D | A | A | A | A | A | A | A |
| 1001 | D | D | D | D | D | D | D | D | D | D | A | A | A | A | A | A |
| 1010 | D | D | D | D | D | D | D | D | D | D | D | A | A | A | A | A |
| 1011 | D | D | D | D | D | D | D | D | D | D | D | D | A | A | A | A |
| 1100 | D | D | D | D | D | D | D | D | D | D | D | D | D | A | A | A |
| 1101 | D | D | D | D | D | D | D | D | D | D | D | D | D | D | A | A |
| 1110 | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | A |
| 1111 | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D |

A = Analog input D = Digital I/O

**Note 1:** AN15 through AN12 are available only on PIC18F8628/8723 devices.

The analog reference voltage is software selectable to either the device's positive and negative supply voltage ($V_{DD}$ and $V_{SS}$), or the voltage level on the RA3/AN3/$V_{REF}$+ and RA2/AN2/$V_{REF}$-/$CV_{REF}$ pins.

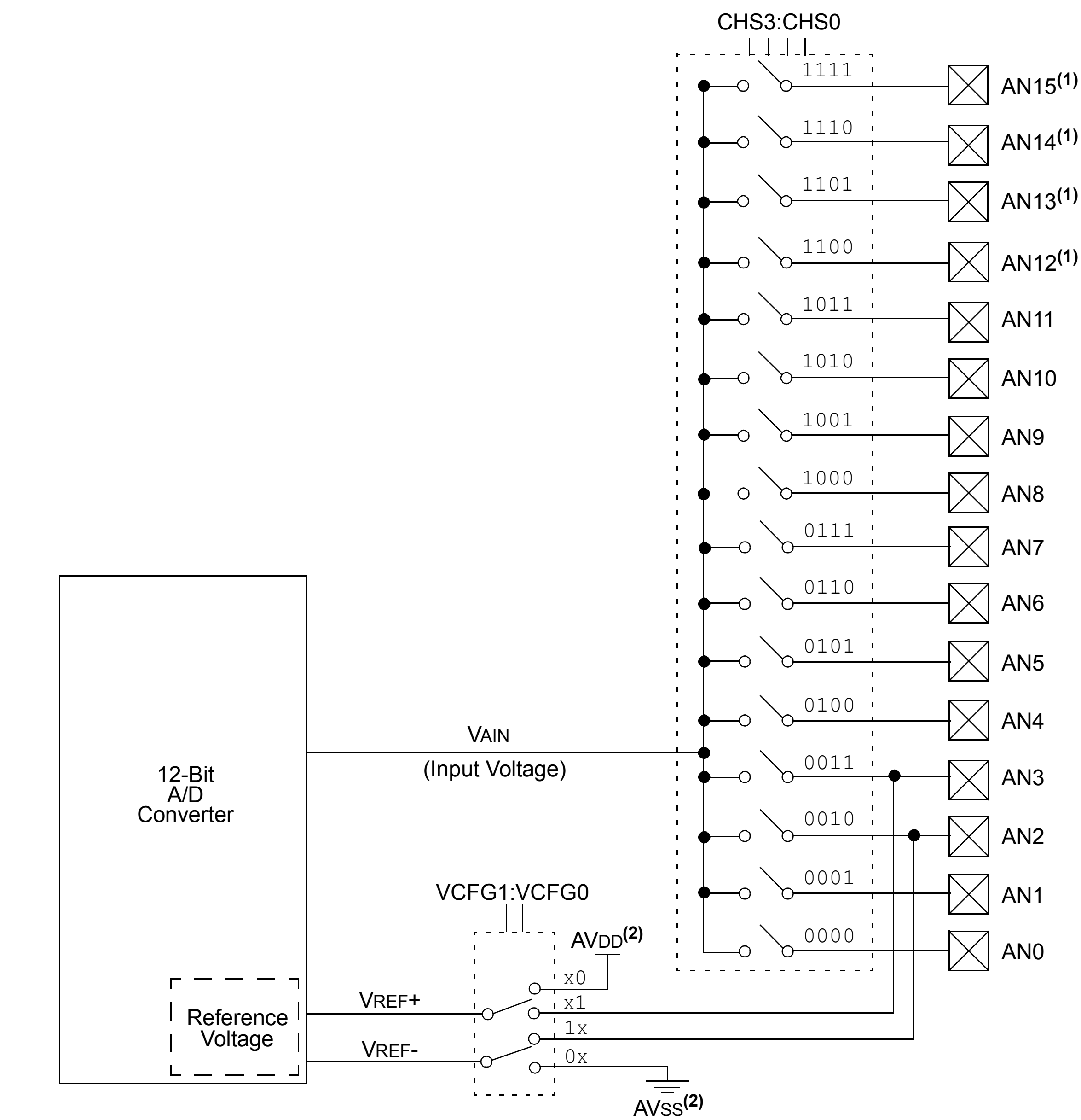
The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D Converter can be configured as an analog input or a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/$\overline{DONE}$ bit (ADCON0<1>) is cleared and the A/D Interrupt Flag bit, ADIF, is set. The block diagram of the A/D module is shown in Figure 2-1.

**FIGURE 2-1: A/D BLOCK DIAGRAM**




**Note 1:** Channels AN12 through AN15 are not available on PIC18F6628/6723 devices.

**2:** I/O pins have diode protection to $V_{DD}$ and $V_{SS}$.

## 2.1 A/D Acquisition Requirements

For the A/D Converter to meet its specified accuracy, the charge holding capacitor ($C_{HOLD}$) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 2-3. The source impedance ($R_S$) and the internal sampling switch ($R_{SS}$) impedance directly affect the time required to charge the capacitor, $C_{HOLD}$. The sampling switch ($R_{SS}$) impedance varies over the device voltage ($V_{DD}$). The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 2.5 kΩ**. After the analog input channel is selected (changed), the channel must be sampled for at least the minimum acquisition time before starting a conversion.

| **Note:** | When the conversion is started, the holding capacitor is disconnected from the input pin. |
|---|---|

To calculate the minimum acquisition time, Equation 2-1 may be used. This equation assumes that 1/2 LSb error is used (4096 steps for the 12-bit A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

Example 2-3 shows the calculation of the minimum required acquisition time, $T_{ACQ}$. This calculation is based on the following application system assumptions:

| | | |
|---|---|---|
| $C_{HOLD}$ | = | 25 pF |
| Rs | = | 2.5 kΩ |
| Conversion Error | ≤ | 1/2 LSb |
| $V_{DD}$ | = | 3V → Rss = 4 kΩ |
| Temperature | = | 85°C (system max.) |

### EQUATION 2-1: ACQUISITION TIME

$$T_{ACQ} = \text{Amplifier Settling Time} + \text{Holding Capacitor Charging Time} + \text{Temperature Coefficient}$$
$$= T_{AMP} + T_C + T_{COFF}$$

### EQUATION 2-2: A/D MINIMUM CHARGING TIME

$$V_{HOLD} = (V_{REF} - (V_{REF}/4096)) \cdot (1 - e^{(-T_C/C_{HOLD}(R_{IC} + R_{SS} + R_S))})$$
or
$$T_C = -(C_{HOLD})(R_{IC} + R_{SS} + R_S)\ \ln(1/4096)$$

### EQUATION 2-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

$$T_{ACQ} = T_{AMP} + T_C + T_{COFF}$$

$$T_{AMP} = 0.2\ \mu s$$

$$T_{COFF} = (\text{Temp} - 25°C)(0.02\ \mu s/°C)$$
$$(85°C - 25°C)(0.02\ \mu s/°C)$$
$$1.2\ \mu s$$

Temperature coefficient is only required for temperatures > 25°C. Below 25°C, $T_{COFF}$ = 0 µs.

$$T_C = -(C_{HOLD})(R_{IC} + R_{SS} + R_S)\ \ln(1/4096)\ \mu s$$
$$-(25\ pF)\ (1\ k\Omega + 4\ k\Omega + 2.5\ k\Omega)\ \ln(0.0002441)\ \mu s$$
$$1.56\ \mu s$$

$$T_{ACQ} = 0.2\ \mu s + 1.56\ \mu s + 1.2\ \mu s$$
$$2.96\ \mu s$$

## 2.4 Operation in Power-Managed Modes

The selection of the automatic acquisition time and A/D conversion clock is determined in part by the clock source and frequency while in a power-managed mode.

If the A/D is expected to operate while the device is in a power-managed mode, the ADCS2:ADCS0 bits in ADCON2 should be updated in accordance with the clock source to be used. The ACQT2:ACQT0 bits do not need to be adjusted as the ADCS2:ADCS0 bits adjust the $T_{AD}$ time for the new clock speed. After entering the mode, an A/D acquisition or conversion may be started. Once started, the device should continue to be clocked by the same clock source until the conversion has been completed.

If desired, the device may be placed into the corresponding Idle mode during the conversion. If the device clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

Operation in Sleep mode requires the A/D $F_{RC}$ clock to be selected. If the ACQT2:ACQT0 bits are set to '`000`' and a conversion is started, the conversion will be delayed one instruction cycle to allow execution of the `SLEEP` instruction and entry to Sleep mode. The IDLEN bit (OSCCON<7>) must have already been cleared prior to starting the conversion.

## 2.5 Configuring Analog Port Pins

The ADCON1, TRISA, TRISF and TRISH registers all configure the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level ($V_{OH}$ or $V_{OL}$) will be converted.

The A/D operation is independent of the state of the CHS3:CHS0 bits and the TRIS bits.

> **Note 1:** When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Analog conversion on pins configured as digital pins can be performed. The voltage on the pin will be accurately converted.
>
> **2:** Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.

## 2.6 A/D Conversions

Figure 2-4 shows the operation of the A/D Converter after the GO/DONE bit has been set and the ACQT2:ACQT0 bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

Figure 2-5 shows the operation of the A/D Converter after the GO/DONE bit has been set, the ACQT2:ACQT0 bits are set to '010' and a 4 TAD acquisition time has been selected before the conversion starts.

Clearing the GO/DONE bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. This means the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers).

After the A/D conversion is completed or aborted, a 2 TCY wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

| Note: | The GO/DONE bit should **NOT** be set in the same instruction that turns on the A/D. Code should wait at least 2 μs after enabling the A/D before beginning an acquisition and conversion cycle. |
|---|---|

## 2.7 Discharge

The discharge phase is used to initialize the value of the holding capacitor. The array is discharged before every sample. This feature helps to optimize the unity gain amplifier, as the circuit always needs to charge the capacitor array, rather than charge/discharge based on previous measure values.

**FIGURE 2-4: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 000, TACQ = 0)**

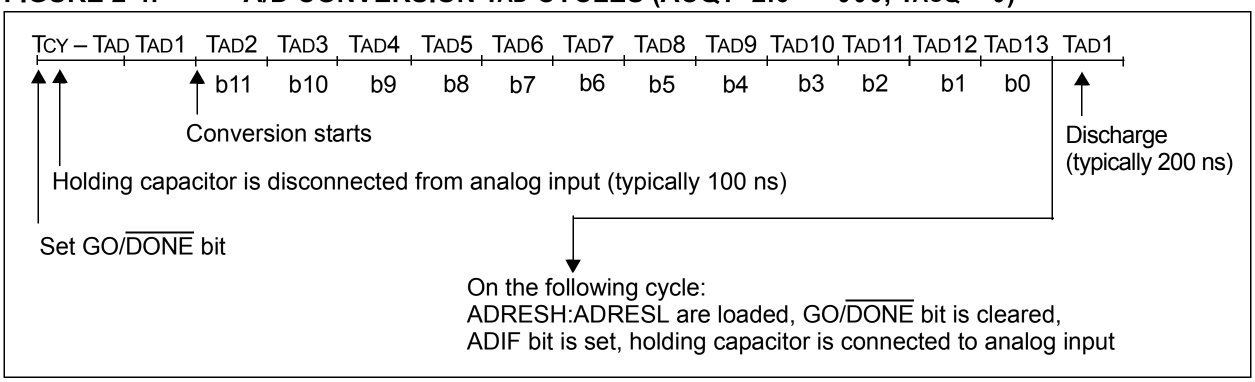
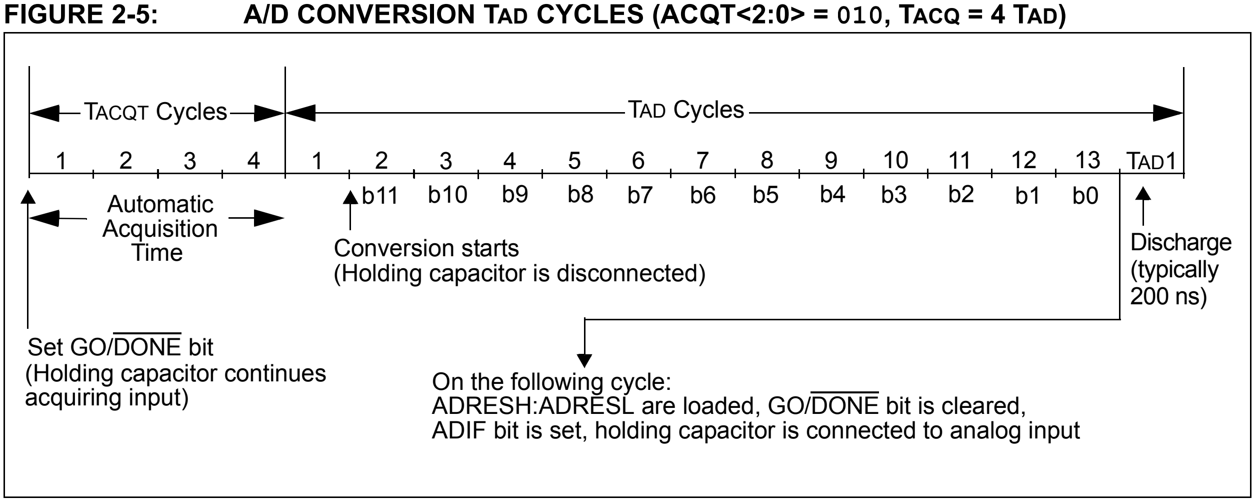



**FIGURE 2-5: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 010, TACQ = 4 TAD)**



## 5.0 PACKAGING INFORMATION

For packaging information, see the *"PIC18F8722 Family Data Sheet"* (DS39646).

## APPENDIX A: REVISION HISTORY

### Revision A (August 2007)

Original data sheet for the PIC18F8723 family of devices.

### Revision B (October 2009)

Updated to remove Preliminary status.

## APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

**TABLE B-1: PIC18F8723 FAMILY DEVICE DIFFERENCES**

| Features | PIC18F6628 | PIC18F6723 | PIC18F8628 | PIC18F8723 |
|---|---|---|---|---|
| Program Memory (Bytes) | 96K | 128K | 96K | 128K |
| Program Memory (Instructions) | 49152 | 65536 | 49152 | 65536 |
| Interrupt Sources | 28 | 28 | 29 | 29 |
| I/O Ports | Ports A, B, C, D, E, F, G | Ports A, B, C, D, E, F, G | Ports A, B, C, D, E, F, G, H, J | Ports A, B, C, D, E, F, G, H, J |
| Capture/Compare/PWM Modules | 2 | 2 | 2 | 2 |
| Enhanced Capture/Compare/PWM Modules | 3 | 3 | 3 | 3 |
| Parallel Communications (PSP) | Yes | Yes | Yes | Yes |
| External Memory Bus | No | No | Yes | Yes |
| 12-Bit Analog-to-Digital Module | 12 Input Channels | 12 Input Channels | 16 Input Channels | 16 Input Channels |
| Packages | 64-Pin TQFP | 64-Pin TQFP | 80-Pin TQFP | 80-Pin TQFP |

## APPENDIX E: MIGRATION FROM MID-RANGE TO ENHANCED DEVICES

A detailed discussion of the differences between the mid-range MCU devices (i.e., PIC16CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in *AN716, "Migrating Designs from PIC16C74A/74B to PIC18C442*". The changes discussed, while device specific, are generally applicable to all mid-range to enhanced device migrations.

This Application Note is available on our web site, www.microchip.com, as Literature Number DS00716.

## APPENDIX F: MIGRATION FROM HIGH-END TO ENHANCED DEVICES

A detailed discussion of the migration pathway and differences between the high-end MCU devices (i.e., PIC17CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in *AN726, "PIC17CXXX to PIC18CXXX Migration*".

This Application Note is available on our web site, www.microchip.com, as Literature Number DS00726.

**NOTES:**

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