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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 40MHz |
| Connectivity | EBI/EMI, I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, HLVD, POR, PWM, WDT |
| Number of I/O | 70 |
| Program Memory Size | 96KB (48K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 3.8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.2V ~ 5.5V |
| Data Converters | A/D 16x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-TQFP |
| Supplier Device Package | 80-TQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic18f8628-i-pt |

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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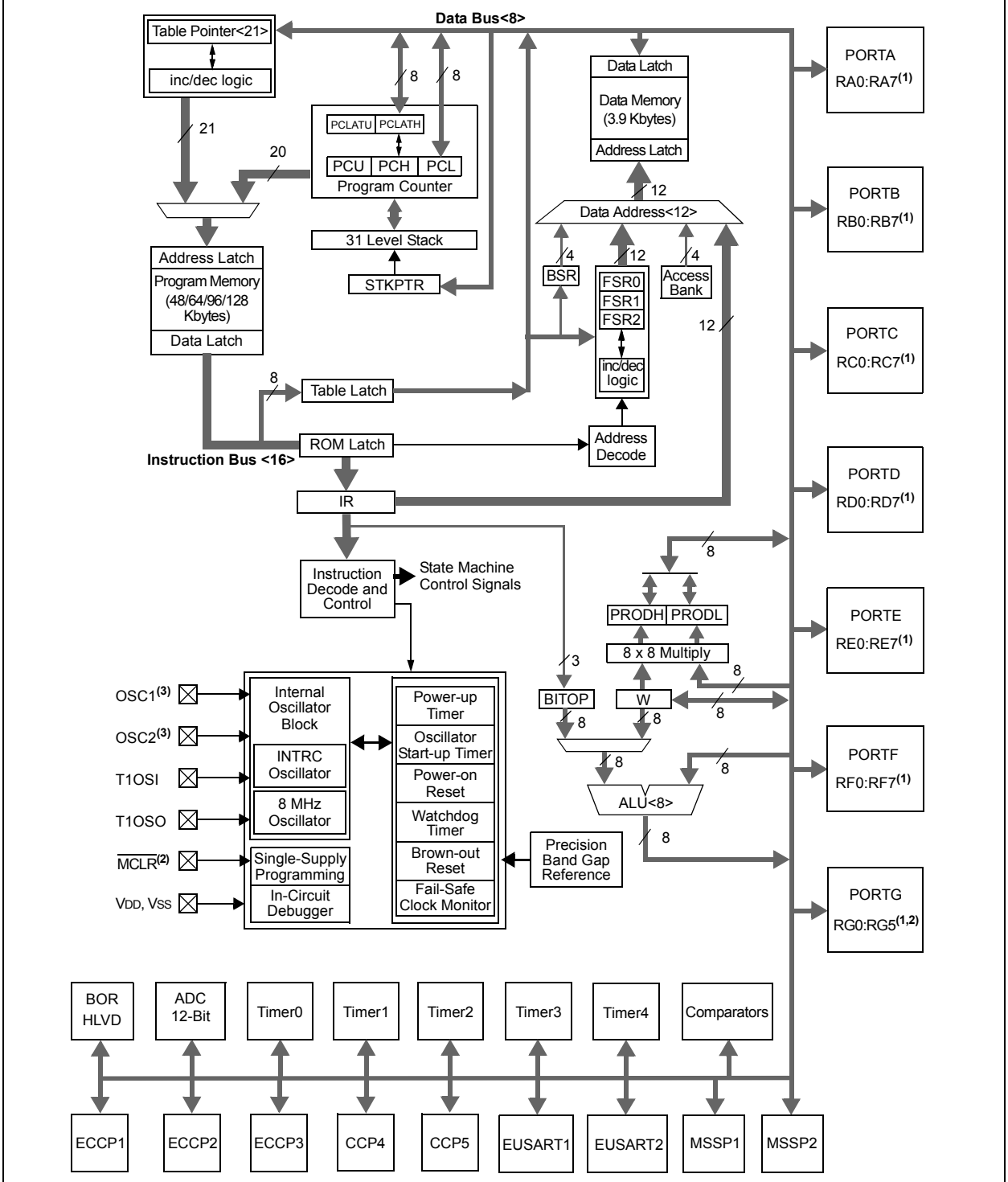
## Table of Contents

**TABLE 1-1: DEVICE FEATURES**

| Features | PIC18F6628 | PIC18F6723 | PIC18F8628 | PIC18F8723 |
|---|---|---|---|---|
| Operating Frequency | DC – 40 MHz | DC – 40 MHz | DC – 40 MHz | DC – 40 MHz |
| Program Memory (Bytes) | 96K | 128K | 96K | 128K |
| Program Memory (Instructions) | 49152 | 65536 | 49152 | 65536 |
| Data Memory (Bytes) | 3936 | 3936 | 3936 | 3936 |
| Data EEPROM Memory (Bytes) | 1024 | 1024 | 1024 | 1024 |
| Interrupt Sources | 28 | 28 | 29 | 29 |
| I/O Ports | Ports A, B, C, D, E, F, G | Ports A, B, C, D, E, F, G | Ports A, B, C, D, E, F, G, H, J | Ports A, B, C, D, E, F, G, H, J |
| Timers | 5 | 5 | 5 | 5 |
| Capture/Compare/PWM Modules | 2 | 2 | 2 | 2 |
| Enhanced Capture/Compare/ PWM Modules | 3 | 3 | 3 | 3 |
| Enhanced USART | 2 | 2 | 2 | 2 |
| Serial Communications | MSSP, Enhanced USART | MSSP, Enhanced USART | MSSP, Enhanced USART | MSSP, Enhanced USART |
| Parallel Communications (PSP) | Yes | Yes | Yes | Yes |
| 12-Bit Analog-to-Digital Module | 12 Input Channels | 12 Input Channels | 16 Input Channels | 16 Input Channels |
| Resets (and Delays) | POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT | POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT | POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT | POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT |
| Programmable High/Low-Voltage Detect | Yes | Yes | Yes | Yes |
| Programmable Brown-out Reset | Yes | Yes | Yes | Yes |
| Instruction Set | 75 Instructions; 83 with Extended Instruction Set Enabled | 75 Instructions; 83 with Extended Instruction Set Enabled | 75 Instructions; 83 with Extended Instruction Set Enabled | 75 Instructions; 83 with Extended Instruction Set Enabled |
| Packages | 64-Pin TQFP | 64-Pin TQFP | 80-Pin TQFP | 80-Pin TQFP |

**FIGURE 1-1: PIC18F6628/6723 (64-PIN) BLOCK DIAGRAM**




**Note 1:** See Table 1-2 for I/O port pin descriptions.

**2:** RG5 is only available when $\overline{\text{MCLR}}$ functionality is disabled.

**3:** OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, refer to **Section 2.0 "Oscillator Configurations"** of the *"PIC18F8722 Family Data Sheet"* (DS39646).

**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTA is a bidirectional I/O port. |
| RA0/AN0 | 24 | | | |
| RA0 | | I/O | TTL | Digital I/O. |
| AN0 | | I | Analog | Analog input 0. |
| RA1/AN1 | 23 | | | |
| RA1 | | I/O | TTL | Digital I/O. |
| AN1 | | I | Analog | Analog input 1. |
| RA2/AN2/VREF- | 22 | | | |
| RA2 | | I/O | TTL | Digital I/O. |
| AN2 | | I | Analog | Analog input 2. |
| VREF- | | I | Analog | A/D reference voltage (low) input. |
| RA3/AN3/VREF+ | 21 | | | |
| RA3 | | I/O | TTL | Digital I/O. |
| AN3 | | I | Analog | Analog input 3. |
| VREF+ | | I | Analog | A/D reference voltage (high) input. |
| RA4/T0CKI | 28 | | | |
| RA4 | | I/O | ST | Digital I/O. |
| T0CKI | | I | ST | Timer0 external clock input. |
| RA5/AN4/HLVDIN | 27 | | | |
| RA5 | | I/O | TTL | Digital I/O. |
| AN4 | | I | Analog | Analog input 4. |
| HLVDIN | | I | Analog | High/Low-Voltage Detect input. |
| RA6 | | | | See the OSC2/CLKO/RA6 pin. |
| RA7 | | | | See the OSC1/CLKI/RA7 pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™ = $I^2C$/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTC is a bidirectional I/O port. |
| RC0/T1OSO/T13CKI | 30 | | | |
| RC0 | | I/O | ST | Digital I/O. |
| T1OSO | | O | — | Timer1 oscillator output. |
| T13CKI | | I | ST | Timer1/Timer3 external clock input. |
| RC1/T1OSI/ECCP2/ P2A | 29 | | | |
| RC1 | | I/O | ST | Digital I/O. |
| T1OSI | | I | CMOS | Timer1 oscillator input. |
| ECCP2(1) | | I/O | ST | Enhanced Capture 2 input/Compare 2 output/ PWM2 output. |
| P2A(1) | | O | — | ECCP2 PWM output A. |
| RC2/ECCP1/P1A | 33 | | | |
| RC2 | | I/O | ST | Digital I/O. |
| ECCP1 | | I/O | ST | Enhanced Capture 1 input/Compare 1 output/ PWM1 output. |
| P1A | | O | — | ECCP1 PWM output A. |
| RC3/SCK1/SCL1 | 34 | | | |
| RC3 | | I/O | ST | Digital I/O. |
| SCK1 | | I/O | ST | Synchronous serial clock input/output for SPI mode. |
| SCL1 | | I/O | ST | Synchronous serial clock input/output for $I^2C$™ mode. |
| RC4/SDI1/SDA1 | 35 | | | |
| RC4 | | I/O | ST | Digital I/O. |
| SDI1 | | I | ST | SPI data in. |
| SDA1 | | I/O | ST | $I^2C$ data I/O. |
| RC5/SDO1 | 36 | | | |
| RC5 | | I/O | ST | Digital I/O. |
| SDO1 | | O | — | SPI data out. |
| RC6/TX1/CK1 | 31 | | | |
| RC6 | | I/O | ST | Digital I/O. |
| TX1 | | O | — | EUSART1 asynchronous transmit. |
| CK1 | | I/O | ST | EUSART1 synchronous clock (see related RX1/DT1). |
| RC7/RX1/DT1 | 32 | | | |
| RC7 | | I/O | ST | Digital I/O. |
| RX1 | | I | ST | EUSART1 asynchronous receive. |
| DT1 | | I/O | ST | EUSART1 synchronous data (see related TX1/CK1). |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™ = $I^2C$/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTD is a bidirectional I/O port. |
| RD0/PSP0 | 58 | | | |
| RD0 | | I/O | ST | Digital I/O. |
| PSP0 | | I/O | TTL | Parallel Slave Port data. |
| RD1/PSP1 | 55 | | | |
| RD1 | | I/O | ST | Digital I/O. |
| PSP1 | | I/O | TTL | Parallel Slave Port data. |
| RD2/PSP2 | 54 | | | |
| RD2 | | I/O | ST | Digital I/O. |
| PSP2 | | I/O | TTL | Parallel Slave Port data. |
| RD3/PSP3 | 53 | | | |
| RD3 | | I/O | ST | Digital I/O. |
| PSP3 | | I/O | TTL | Parallel Slave Port data. |
| RD4/PSP4/SDO2 | 52 | | | |
| RD4 | | I/O | ST | Digital I/O. |
| PSP4 | | I/O | TTL | Parallel Slave Port data. |
| SDO2 | | O | — | SPI data out. |
| RD5/PSP5/SDI2/ SDA2 | 51 | | | |
| RD5 | | I/O | ST | Digital I/O. |
| PSP5 | | I/O | TTL | Parallel Slave Port data. |
| SDI2 | | I | ST | SPI data in. |
| SDA2 | | I/O | $I^2C$/SMB | $I^2C$™ data I/O. |
| RD6/PSP6/SCK2/ SCL2 | 50 | | | |
| RD6 | | I/O | ST | Digital I/O. |
| PSP6 | | I/O | TTL | Parallel Slave Port data. |
| SCK2 | | I/O | ST | Synchronous serial clock input/output for SPI mode. |
| SCL2 | | I/O | $I^2C$/SMB | Synchronous serial clock input/output for $I^2C$ mode. |
| RD7/PSP7/$\overline{SS2}$ | 49 | | | |
| RD7 | | I/O | ST | Digital I/O. |
| PSP7 | | I/O | TTL | Parallel Slave Port data. |
| $\overline{SS2}$ | | I | TTL | SPI slave select input. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™ = $I^2C$/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTE is a bidirectional I/O port. |
| RE0/$\overline{RD}$/P2D | 2 | | | |
| RE0 | | I/O | ST | Digital I/O. |
| $\overline{RD}$ | | I | TTL | Read control for Parallel Slave Port. |
| P2D | | O | — | ECCP2 PWM output D. |
| RE1/$\overline{WR}$/P2C | 1 | | | |
| RE1 | | I/O | ST | Digital I/O. |
| $\overline{WR}$ | | I | TTL | Write control for Parallel Slave Port. |
| P2C | | O | — | ECCP2 PWM output C. |
| RE2/$\overline{CS}$/P2B | 64 | | | |
| RE2 | | I/O | ST | Digital I/O. |
| $\overline{CS}$ | | I | TTL | Chip select control for Parallel Slave Port. |
| P2B | | O | — | ECCP2 PWM output B. |
| RE3/P3C | 63 | | | |
| RE3 | | I/O | ST | Digital I/O. |
| P3C | | O | — | ECCP3 PWM output C. |
| RE4/P3B | 62 | | | |
| RE4 | | I/O | ST | Digital I/O. |
| P3B | | O | — | ECCP3 PWM output B. |
| RE5/P1C | 61 | | | |
| RE5 | | I/O | ST | Digital I/O. |
| P1C | | O | — | ECCP1 PWM output C. |
| RE6/P1B | 60 | | | |
| RE6 | | I/O | ST | Digital I/O. |
| P1B | | O | — | ECCP1 PWM output B. |
| RE7/ECCP2/P2A | 59 | | | |
| RE7 | | I/O | ST | Digital I/O. |
| ECCP2**(2)** | | I/O | ST | Enhanced Capture 2 input/Compare 2 output/ PWM2 output. |
| P2A**(2)** | | O | — | ECCP2 PWM output A. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™ = $I^2C$/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTF is a bidirectional I/O port. |
| RF0/AN5 | 18 | | | |
| RF0 | | I/O | ST | Digital I/O. |
| AN5 | | I | Analog | Analog input 5. |
| RF1/AN6/C2OUT | 17 | | | |
| RF1 | | I/O | ST | Digital I/O. |
| AN6 | | I | Analog | Analog input 6. |
| C2OUT | | O | — | Comparator 2 output. |
| RF2/AN7/C1OUT | 16 | | | |
| RF2 | | I/O | ST | Digital I/O. |
| AN7 | | I | Analog | Analog input 7. |
| C1OUT | | O | — | Comparator 1 output. |
| RF3/AN8 | 15 | | | |
| RF3 | | I/O | ST | Digital I/O. |
| AN8 | | I | Analog | Analog input 8. |
| RF4/AN9 | 14 | | | |
| RF4 | | I/O | ST | Digital I/O. |
| AN9 | | I | Analog | Analog input 9. |
| RF5/AN10/CVREF | 13 | | | |
| RF5 | | I/O | ST | Digital I/O. |
| AN10 | | I | Analog | Analog input 10. |
| CVREF | | O | Analog | Comparator reference voltage output. |
| RF6/AN11 | 12 | | | |
| RF6 | | I/O | ST | Digital I/O. |
| AN11 | | I | Analog | Analog input 11. |
| RF7/$\overline{SS1}$ | 11 | | | |
| RF7 | | I/O | ST | Digital I/O. |
| $\overline{SS1}$ | | I | TTL | SPI slave select input. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™ = $I^2C$/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTG is a bidirectional I/O port. |
| RG0/ECCP3/P3A | 3 | | | |
| RG0 | | I/O | ST | Digital I/O. |
| ECCP3 | | I/O | ST | Enhanced Capture 3 input/Compare 3 output/ PWM3 output. |
| P3A | | O | — | ECCP3 PWM output A. |
| RG1/TX2/CK2 | 4 | | | |
| RG1 | | I/O | ST | Digital I/O. |
| TX2 | | O | — | EUSART2 asynchronous transmit. |
| CK2 | | I/O | ST | EUSART2 synchronous clock (see related RX2/DT2). |
| RG2/RX2/DT2 | 5 | | | |
| RG2 | | I/O | ST | Digital I/O. |
| RX2 | | I | ST | EUSART2 asynchronous receive. |
| DT2 | | I/O | ST | EUSART2 synchronous data (see related TX2/CK2). |
| RG3/CCP4/P3D | 6 | | | |
| RG3 | | I/O | ST | Digital I/O. |
| CCP4 | | I/O | ST | Capture 4 input/Compare 4 output/PWM4 output. |
| P3D | | O | — | ECCP3 PWM output D. |
| RG4/CCP5/P1D | 8 | | | |
| RG4 | | I/O | ST | Digital I/O. |
| CCP5 | | I/O | ST | Capture 5 input/Compare 5 output/PWM5 output. |
| P1D | | O | — | ECCP1 PWM output D. |
| RG5 | | | | See RG5/$\overline{\text{MCLR}}$/VPP pin. |
| VSS | 9, 25, 41, 56 | P | — | Ground reference for logic and I/O pins. |
| VDD | 10, 26, 38, 57 | P | — | Positive supply for logic and I/O pins. |
| AVSS | 20 | P | — | Ground reference for analog modules. |
| AVDD | 19 | P | — | Positive supply for analog modules. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™ = $I^2C$/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| RG5/$\overline{MCLR}$/VPP | 9 | | | Master Clear (input) or programming voltage (input). |
| RG5 | | I | ST | Digital input. |
| $\overline{MCLR}$ | | I | ST | Master Clear (Reset) input. This pin is an active-low Reset to the device. |
| VPP | | P | | Programming voltage input. |
| OSC1/CLKI/RA7 | 49 | | | Oscillator crystal or external clock input. |
| OSC1 | | I | ST | Oscillator crystal input or external clock source input. ST buffer when configured in RC mode, CMOS otherwise. |
| CLKI | | I | CMOS | External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) |
| RA7 | | I/O | TTL | General purpose I/O pin. |
| OSC2/CLKO/RA6 | 50 | | | Oscillator crystal or clock output. |
| OSC2 | | O | — | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. |
| CLKO | | O | — | In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. |
| RA6 | | I/O | TTL | General purpose I/O pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™/SMB = $I^2C$/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).

**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).

**3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

**4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

**5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTA is a bidirectional I/O port. |
| RA0/AN0 | 30 | | | |
| RA0 | | I/O | TTL | Digital I/O. |
| AN0 | | I | Analog | Analog input 0. |
| RA1/AN1 | 29 | | | |
| RA1 | | I/O | TTL | Digital I/O. |
| AN1 | | I | Analog | Analog input 1. |
| RA2/AN2/VREF- | 28 | | | |
| RA2 | | I/O | TTL | Digital I/O. |
| AN2 | | I | Analog | Analog input 2. |
| VREF- | | I | Analog | A/D reference voltage (low) input. |
| RA3/AN3/VREF+ | 27 | | | |
| RA3 | | I/O | TTL | Digital I/O. |
| AN3 | | I | Analog | Analog input 3. |
| VREF+ | | I | Analog | A/D reference voltage (high) input. |
| RA4/T0CKI | 34 | | | |
| RA4 | | I/O | ST | Digital I/O. |
| T0CKI | | I | ST | Timer0 external clock input. |
| RA5/AN4/HLVDIN | 33 | | | |
| RA5 | | I/O | TTL | Digital I/O. |
| AN4 | | I | Analog | Analog input 4. |
| HLVDIN | | I | Analog | High/Low-Voltage Detect input. |
| RA6 | | | | See the OSC2/CLKO/RA6 pin. |
| RA7 | | | | See the OSC1/CLKI/RA7 pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™/SMB = $I^2C$/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).

**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).

**3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

**4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

**5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTC is a bidirectional I/O port. |
| RC0/T1OSO/T13CKI | 36 | | | |
| RC0 | | I/O | ST | Digital I/O. |
| T1OSO | | O | — | Timer1 oscillator output. |
| T13CKI | | I | ST | Timer1/Timer3 external clock input. |
| RC1/T1OSI/ECCP2/ P2A | 35 | | | |
| RC1 | | I/O | ST | Digital I/O. |
| T1OSI | | I | CMOS | Timer1 oscillator input. |
| ECCP2(2) | | I/O | ST | Enhanced Capture 2 input/Compare 2 output/ PWM2 output. |
| P2A(2) | | O | — | ECCP2 PWM output A. |
| RC2/ECCP1/P1A | 43 | | | |
| RC2 | | I/O | ST | Digital I/O. |
| ECCP1 | | I/O | ST | Enhanced Capture 1 input/Compare 1 output/ PWM1 output. |
| P1A | | O | — | ECCP1 PWM output A. |
| RC3/SCK1/SCL1 | 44 | | | |
| RC3 | | I/O | ST | Digital I/O. |
| SCK1 | | I/O | ST | Synchronous serial clock input/output for SPI mode. |
| SCL1 | | I/O | ST | Synchronous serial clock input/output for $I^2C$™ mode. |
| RC4/SDI1/SDA1 | 45 | | | |
| RC4 | | I/O | ST | Digital I/O. |
| SDI1 | | I | ST | SPI data in. |
| SDA1 | | I/O | ST | $I^2C$ data I/O. |
| RC5/SDO1 | 46 | | | |
| RC5 | | I/O | ST | Digital I/O. |
| SDO1 | | O | — | SPI data out. |
| RC6/TX1/CK1 | 37 | | | |
| RC6 | | I/O | ST | Digital I/O. |
| TX1 | | O | — | EUSART1 asynchronous transmit. |
| CK1 | | I/O | ST | EUSART1 synchronous clock (see related RX1/DT1). |
| RC7/RX1/DT1 | 38 | | | |
| RC7 | | I/O | ST | Digital I/O. |
| RX1 | | I | ST | EUSART1 asynchronous receive. |
| DT1 | | I/O | ST | EUSART1 synchronous data (see related TX1/CK1). |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™/SMB = $I^2C$/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).

**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).

**3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

**4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

**5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTH is a bidirectional I/O port. |
| RH0/A16 | 79 | | | |
| RH0 | | I/O | ST | Digital I/O. |
| A16 | | I/O | TTL | External memory address/data 16. |
| RH1/A17 | 80 | | | |
| RH1 | | I/O | ST | Digital I/O. |
| A17 | | I/O | TTL | External memory address/data 17. |
| RH2/A18 | 1 | | | |
| RH2 | | I/O | ST | Digital I/O. |
| A18 | | I/O | TTL | External memory address/data 18. |
| RH3/A19 | 2 | | | |
| RH3 | | I/O | ST | Digital I/O. |
| A19 | | I/O | TTL | External memory address/data 19. |
| RH4/AN12/P3C | 22 | | | |
| RH4 | | I/O | ST | Digital I/O. |
| AN12 | | I | Analog | Analog input 12. |
| P3C(5) | | O | — | ECCP3 PWM output C. |
| RH5/AN13/P3B | 21 | | | |
| RH5 | | I/O | ST | Digital I/O. |
| AN13 | | I | Analog | Analog input 13. |
| P3B(5) | | O | — | ECCP3 PWM output B. |
| RH6/AN14/P1C | 20 | | | |
| RH6 | | I/O | ST | Digital I/O. |
| AN14 | | I | Analog | Analog input 14. |
| P1C(5) | | O | — | ECCP1 PWM output C. |
| RH7/AN15/P1B | 19 | | | |
| RH7 | | I/O | ST | Digital I/O. |
| AN15 | | I | Analog | Analog input 15. |
| P1B(5) | | O | — | ECCP1 PWM output B. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™/SMB = $I^2C$/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).

**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).

**3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

**4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

**5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

**REGISTER 2-3: ADCON2: A/D CONTROL REGISTER 2**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADFM | — | ACQT2 | ACQT1 | ACQT0 | ADCS2 | ADCS1 | ADCS0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified
0 = Left justified

bit 6 **Unimplemented:** Read as '0'

bit 5-3 **ACQT2:ACQT0:** A/D Acquisition Time Select bits
111 = 20 TAD
110 = 16 TAD
101 = 12 TAD
100 = 8 TAD
011 = 6 TAD
010 = 4 TAD
001 = 2 TAD
000 = 0 TAD(1)

bit 2-0 **ADCS2:ADCS0:** A/D Conversion Clock Select bits
111 = FRC (clock derived from A/D RC oscillator)(1)
110 = FOSC/64
101 = FOSC/16
100 = FOSC/4
011 = FRC (clock derived from A/D RC oscillator)(1)
010 = FOSC/32
001 = FOSC/8
000 = FOSC/2

**Note 1:** If the A/D FRC clock source is selected, a delay of one TCY (instruction cycle) is added before the A/D clock starts. This allows the SLEEP instruction to be executed before starting a conversion.

The analog reference voltage is software selectable to either the device's positive and negative supply voltage ($V_{DD}$ and $V_{SS}$), or the voltage level on the RA3/AN3/$V_{REF+}$ and RA2/AN2/$V_{REF-}$/$CV_{REF}$ pins.

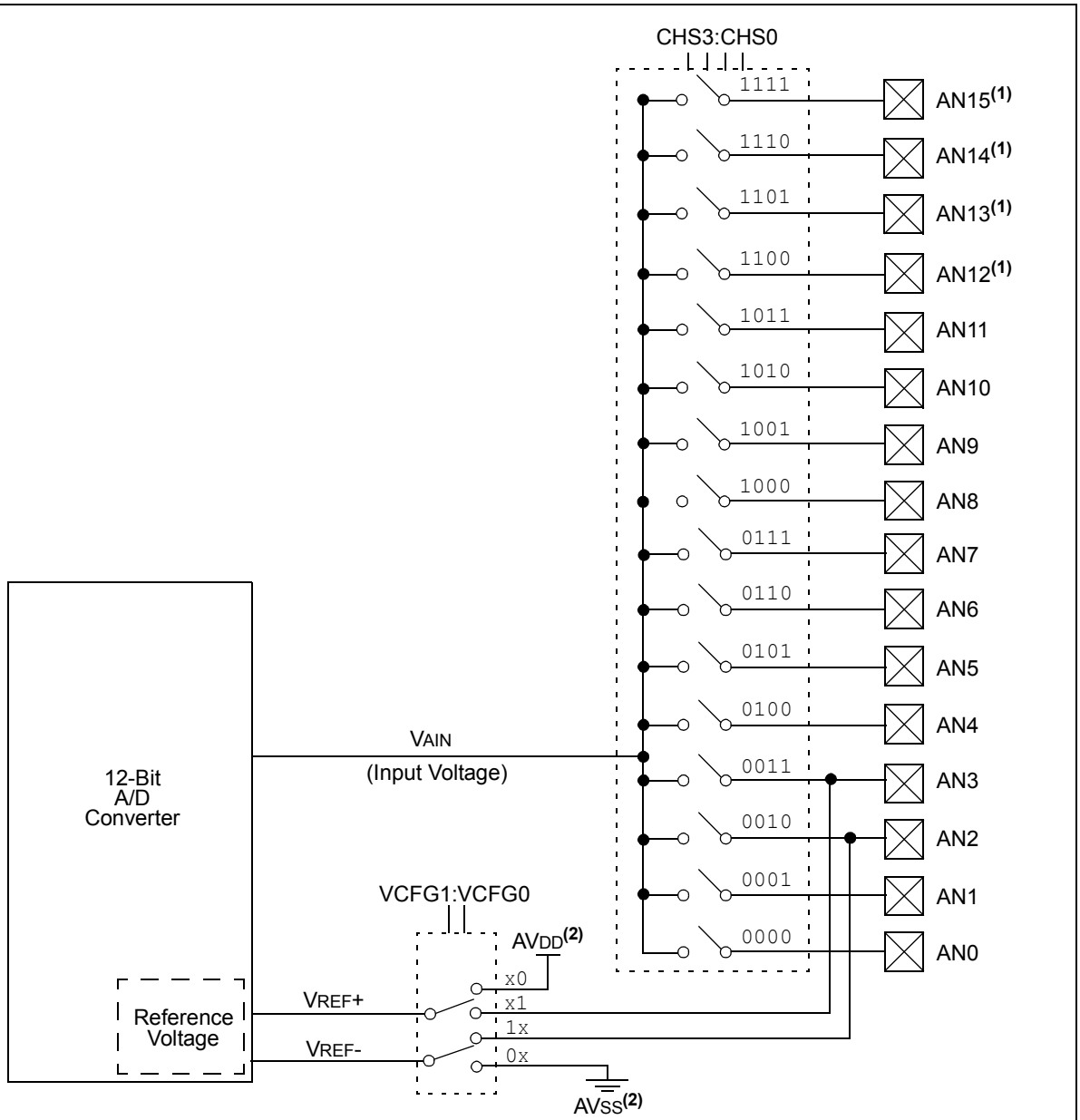
The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D Converter can be configured as an analog input or a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/$\overline{DONE}$ bit (ADCON0<1>) is cleared and the A/D Interrupt Flag bit, ADIF, is set. The block diagram of the A/D module is shown in Figure 2-1.

**FIGURE 2-1: A/D BLOCK DIAGRAM**




**Note 1:** Channels AN12 through AN15 are not available on PIC18F6628/6723 devices.

**2:** I/O pins have diode protection to $V_{DD}$ and $V_{SS}$.

## 2.1 A/D Acquisition Requirements

For the A/D Converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 2-3. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor, CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 2.5 kΩ**. After the analog input channel is selected (changed), the channel must be sampled for at least the minimum acquisition time before starting a conversion.

| **Note:** | When the conversion is started, the holding capacitor is disconnected from the input pin. |
|---|---|

To calculate the minimum acquisition time, Equation 2-1 may be used. This equation assumes that 1/2 LSb error is used (4096 steps for the 12-bit A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

Example 2-3 shows the calculation of the minimum required acquisition time, TACQ. This calculation is based on the following application system assumptions:

| | | |
|---|---|---|
| CHOLD | = | 25 pF |
| Rs | = | 2.5 kΩ |
| Conversion Error | ≤ | 1/2 LSb |
| VDD | = | 3V → Rss = 4 kΩ |
| Temperature | = | 85°C (system max.) |

**EQUATION 2-1: ACQUISITION TIME**

$$T_{ACQ} = \text{Amplifier Settling Time} + \text{Holding Capacitor Charging Time} + \text{Temperature Coefficient}$$
$$= T_{AMP} + T_C + T_{COFF}$$

**EQUATION 2-2: A/D MINIMUM CHARGING TIME**

$$V_{HOLD} = (V_{REF} - (V_{REF}/4096)) \cdot (1 - e^{(-T_C/C_{HOLD}(R_{IC} + R_{SS} + R_S))})$$
or
$$T_C = -(C_{HOLD})(R_{IC} + R_{SS} + R_S) \ln(1/4096)$$

**EQUATION 2-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME**

$$T_{ACQ} = T_{AMP} + T_C + T_{COFF}$$
$$T_{AMP} = 0.2\ \mu s$$
$$T_{COFF} = (\text{Temp} - 25°C)(0.02\ \mu s/°C)$$
$$(85°C - 25°C)(0.02\ \mu s/°C)$$
$$1.2\ \mu s$$

Temperature coefficient is only required for temperatures > 25°C. Below 25°C, $T_{COFF} = 0\ \mu s$.

$$T_C = -(C_{HOLD})(R_{IC} + R_{SS} + R_S) \ln(1/4096)\ \mu s$$
$$-(25\ pF)\ (1\ k\Omega + 4\ k\Omega + 2.5\ k\Omega) \ln(0.0002441)\ \mu s$$
$$1.56\ \mu s$$

$$T_{ACQ} = 0.2\ \mu s + 1.56\ \mu s + 1.2\ \mu s$$
$$2.96\ \mu s$$

## 2.6 A/D Conversions

Figure 2-4 shows the operation of the A/D Converter after the GO/$\overline{\text{DONE}}$ bit has been set and the ACQT2:ACQT0 bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

Figure 2-5 shows the operation of the A/D Converter after the GO/$\overline{\text{DONE}}$ bit has been set, the ACQT2:ACQT0 bits are set to '010' and a 4 TAD acquisition time has been selected before the conversion starts.

Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. This means the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers).

After the A/D conversion is completed or aborted, a 2 TCY wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

**Note:** The GO/$\overline{\text{DONE}}$ bit should **NOT** be set in the same instruction that turns on the A/D. Code should wait at least 2 μs after enabling the A/D before beginning an acquisition and conversion cycle.

## 2.7 Discharge

The discharge phase is used to initialize the value of the holding capacitor. The array is discharged before every sample. This feature helps to optimize the unity gain amplifier, as the circuit always needs to charge the capacitor array, rather than charge/discharge based on previous measure values.

**FIGURE 2-4: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 000, TACQ = 0)**

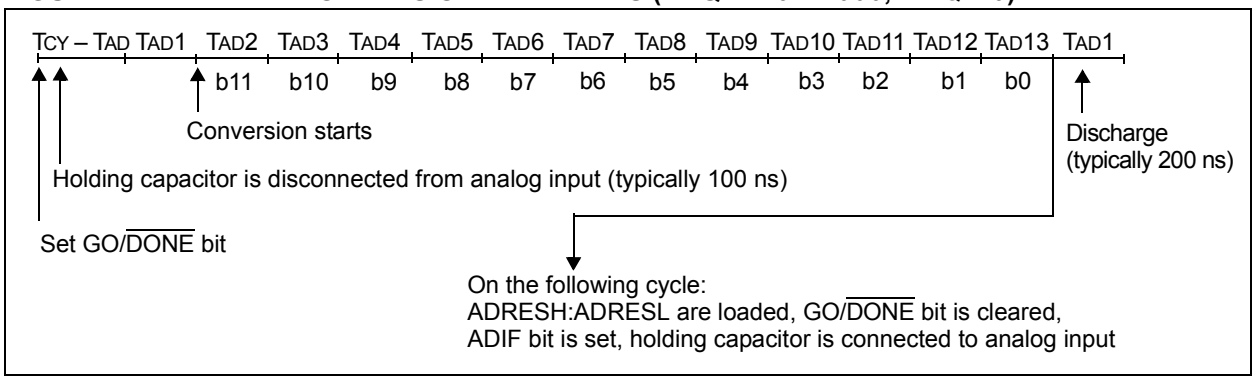
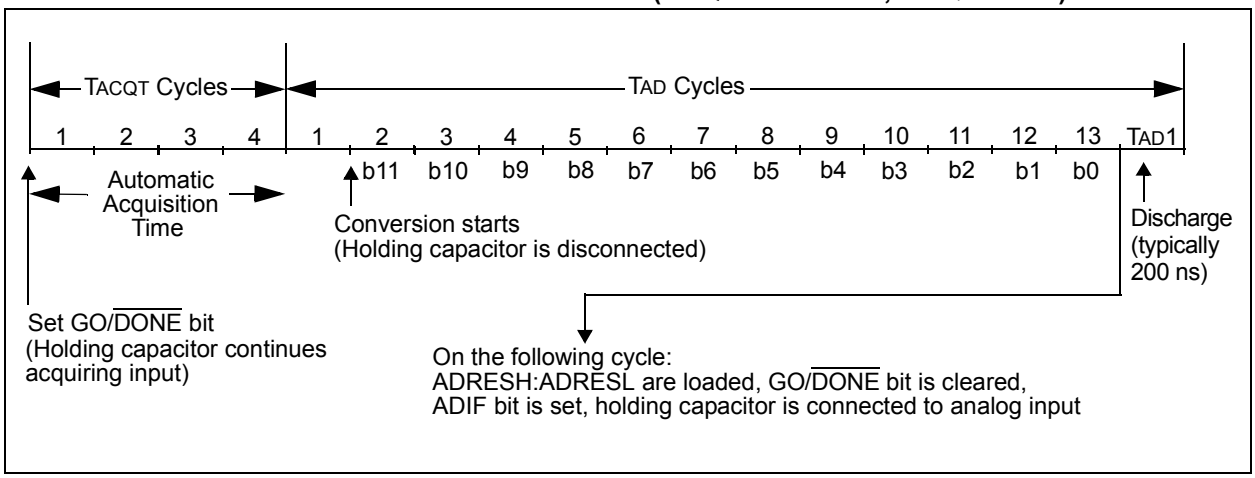



**FIGURE 2-5: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 010, TACQ = 4 TAD)**



## APPENDIX A: REVISION HISTORY

### Revision A (August 2007)

Original data sheet for the PIC18F8723 family of devices.

### Revision B (October 2009)

Updated to remove Preliminary status.

## APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

**TABLE B-1: PIC18F8723 FAMILY DEVICE DIFFERENCES**

| Features | PIC18F6628 | PIC18F6723 | PIC18F8628 | PIC18F8723 |
|---|---|---|---|---|
| Program Memory (Bytes) | 96K | 128K | 96K | 128K |
| Program Memory (Instructions) | 49152 | 65536 | 49152 | 65536 |
| Interrupt Sources | 28 | 28 | 29 | 29 |
| I/O Ports | Ports A, B, C, D, E, F, G | Ports A, B, C, D, E, F, G | Ports A, B, C, D, E, F, G, H, J | Ports A, B, C, D, E, F, G, H, J |
| Capture/Compare/PWM Modules | 2 | 2 | 2 | 2 |
| Enhanced Capture/Compare/PWM Modules | 3 | 3 | 3 | 3 |
| Parallel Communications (PSP) | Yes | Yes | Yes | Yes |
| External Memory Bus | No | No | Yes | Yes |
| 12-Bit Analog-to-Digital Module | 12 Input Channels | 12 Input Channels | 16 Input Channels | 16 Input Channels |
| Packages | 64-Pin TQFP | 64-Pin TQFP | 80-Pin TQFP | 80-Pin TQFP |

**NOTES:**