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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	70
Program Memory Size	96KB (48K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f8628t-i-pt

PIC18F8723 FAMILY

64/80-Pin, 1-Mbit, Enhanced Flash Microcontrollers with 12-Bit A/D and nanoWatt Technology

Peripheral Highlights:

- 12-Bit, Up to 16-Channel Analog-to-Digital Converter module (A/D):
  - Auto-acquisition capability
  - Conversion available during Sleep
- Two Master Synchronous Serial Port (MSSP) modules supporting 2/3/4-Wire SPI (all four modes) and I^2C™ Master and Slave modes
- Two Capture/Compare/PWM (CCP) modules
- Three Enhanced Capture/Compare/PWM (ECCP) modules:
  - One, two or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart
- Two Enhanced Addressable USART modules:
  - Supports RS-485, RS-232 and LIN 1.2
  - Auto-wake-up on Start bit
  - Auto-Baud Detect
- Dual Analog Comparators with Input Multiplexing
- High-Current Sink/Source 25 mA/25 mA
- Four Programmable External Interrupts
- Four Input Change Interrupts

External Memory Interface:

- Address Capability of Up to 2 Mbytes
- 8-Bit or 16-Bit Interface
- 8, 12, 16 and 20-Bit Address modes

Power-Managed Modes:

- Run: CPU on, Peripherals on
- Idle: CPU off, Peripherals on
- Sleep: CPU off, Peripherals off
- Idle mode Currents Down to 15 μA Typical
- Sleep Current Down to 0.2 μA Typical
- Timer1 Oscillator: 1.8 μA, 32 kHz, 2V
- Watchdog Timer: 2.1 μA

Special Microcontroller Features:

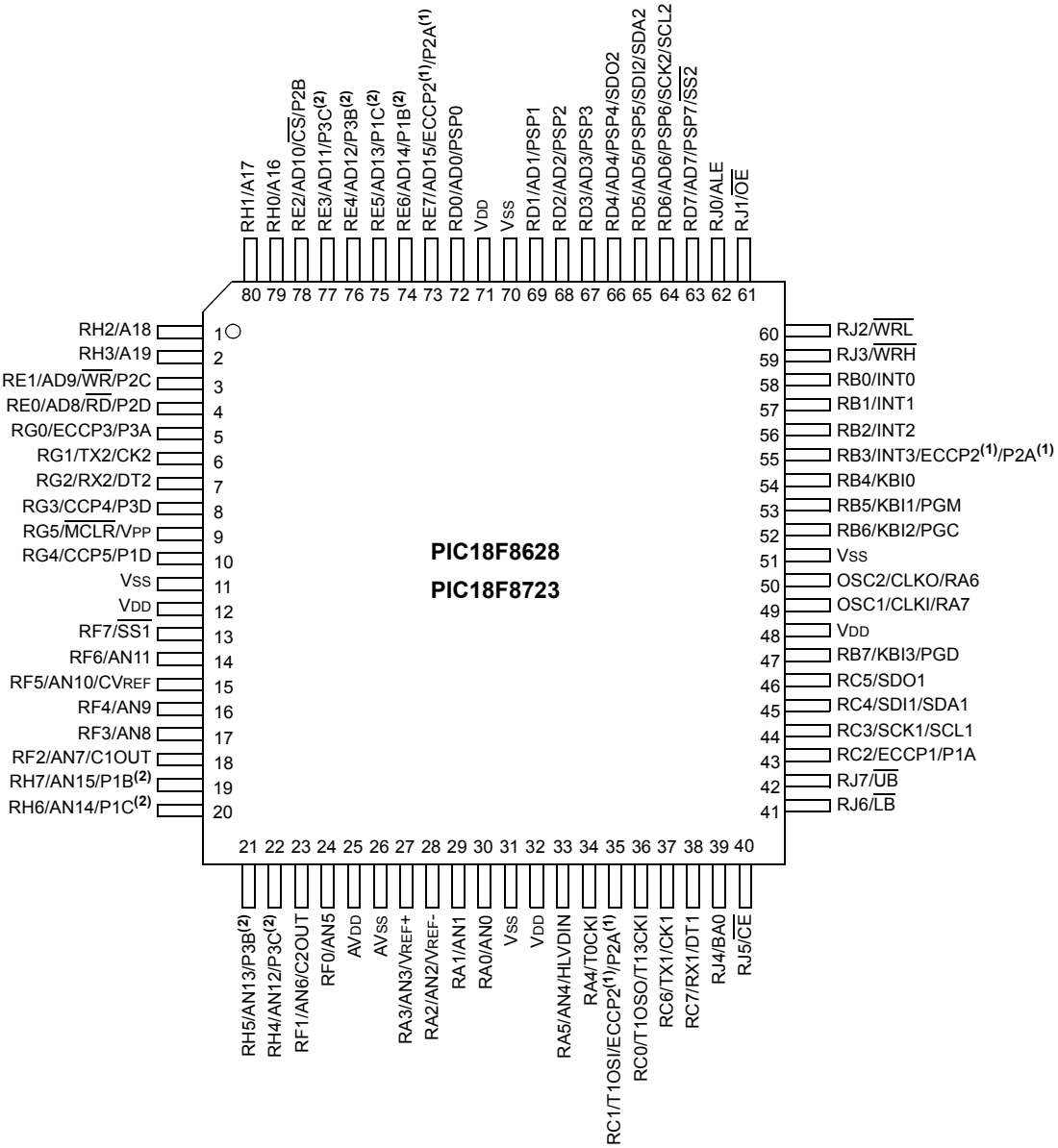
- C Compiler Optimized Architecture:
  - Optional extended instruction set designed to optimize re-entrant code
- 100,000 Erase/Write Cycle Enhanced Flash Program Memory Typical
- 1,000,000 Erase/Write Cycle Data EEPROM Memory Typical
- Flash/Data EEPROM Retention: 100 Years Typical
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 131s
- Single-Supply In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Wide Operating Voltage Range: 2.0V to 5.5V
- Fail-Safe Clock Monitor
- Two-Speed Oscillator Start-up
- nanoWatt Technology

Note: This document is supplemented by the *"PIC18F8722 Family Data Sheet"* (DS39646). See **Section 1.0 "Device Overview"**.

Device	Program Memory		Data Memory		I/O	12-Bit A/D (ch)	CCP/ ECCP (PWM)	MSSP			EUSART	Comparators	Timers 8/16-Bit	External Bus
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)					SPI	Master I^2C™				
PIC18F6628	96K	49152	3936	1024	54	12	2/3	2	Y	Y	2	2	2/3	N
PIC18F6723	128K	65536	3936	1024	54	12	2/3	2	Y	Y	2	2	2/3	N
PIC18F8628	96K	49152	3936	1024	70	16	2/3	2	Y	Y	2	2	2/3	Y
PIC18F8723	128K	65536	3936	1024	70	16	2/3	2	Y	Y	2	2	2/3	Y

Pin Diagrams (Continued)

80-Pin TQFP



Note 1: The ECCP2/P2A pin placement is determined by the CCP2MX Configuration bit and Processor mode settings.
2: P1B, P1C, P3B and P3C pin placement is determined by the ECCPMX Configuration bit.

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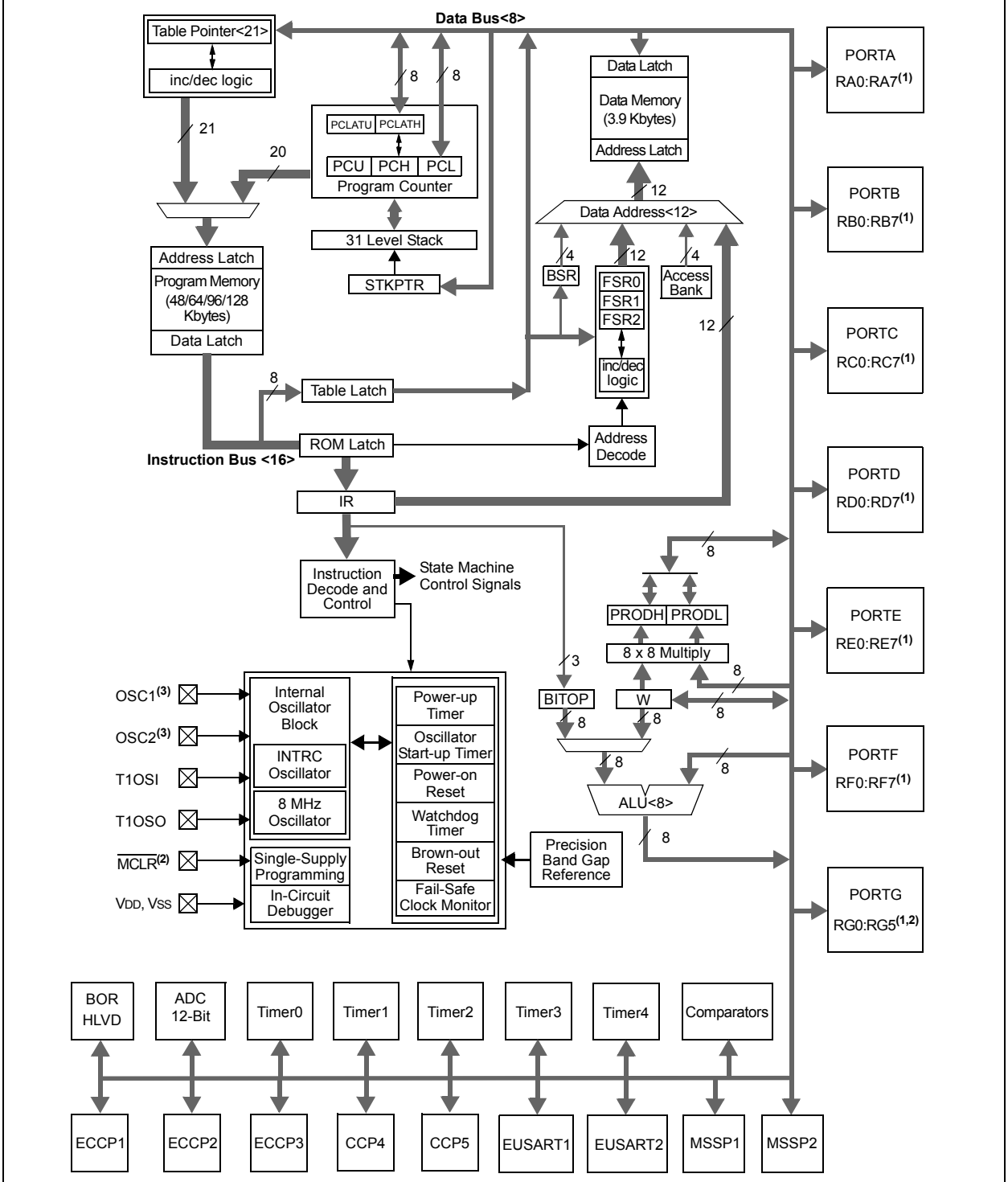
NOTES:

FIGURE 1-1: PIC18F6628/6723 (64-PIN) BLOCK DIAGRAM



Note 1: See Table 1-2 for I/O port pin descriptions.

2: RG5 is only available when $\overline{\text{MCLR}}$ functionality is disabled.

3: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, refer to **Section 2.0 "Oscillator Configurations"** of the *"PIC18F8722 Family Data Sheet"* (DS39646).

TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RG5/$\overline{MCLR}$/V_{PP}	7			Master Clear (input) or programming voltage (input).
RG5		I	ST	Digital input.
$\overline{MCLR}$		I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
V_{PP}		P		Programming voltage input.
OSC1/CLKI/RA7	39			Oscillator crystal or external clock input.
OSC1		I	ST	Oscillator crystal input or external clock source input. ST buffer when configured in RC mode, CMOS otherwise.
CLKI		I	CMOS	External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.)
RA7		I/O	TTL	General purpose I/O pin.
OSC2/CLKO/RA6	40			Oscillator crystal or clock output.
OSC2		O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO		O	—	In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6		I/O	TTL	General purpose I/O pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; I^2C™ = I^2C/SMBus input buffer

Note 1: Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTD is a bidirectional I/O port.
RD0/PSP0	58			
RD0		I/O	ST	Digital I/O.
PSP0		I/O	TTL	Parallel Slave Port data.
RD1/PSP1	55			
RD1		I/O	ST	Digital I/O.
PSP1		I/O	TTL	Parallel Slave Port data.
RD2/PSP2	54			
RD2		I/O	ST	Digital I/O.
PSP2		I/O	TTL	Parallel Slave Port data.
RD3/PSP3	53			
RD3		I/O	ST	Digital I/O.
PSP3		I/O	TTL	Parallel Slave Port data.
RD4/PSP4/SDO2	52			
RD4		I/O	ST	Digital I/O.
PSP4		I/O	TTL	Parallel Slave Port data.
SDO2		O	—	SPI data out.
RD5/PSP5/SDI2/ SDA2	51			
RD5		I/O	ST	Digital I/O.
PSP5		I/O	TTL	Parallel Slave Port data.
SDI2		I	ST	SPI data in.
SDA2		I/O	I^2C/SMB	I^2C™ data I/O.
RD6/PSP6/SCK2/ SCL2	50			
RD6		I/O	ST	Digital I/O.
PSP6		I/O	TTL	Parallel Slave Port data.
SCK2		I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL2		I/O	I^2C/SMB	Synchronous serial clock input/output for I^2C mode.
RD7/PSP7/$\overline{SS2}$	49			
RD7		I/O	ST	Digital I/O.
PSP7		I/O	TTL	Parallel Slave Port data.
$\overline{SS2}$		I	TTL	SPI slave select input.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; I^2C™ = I^2C/SMBus input buffer

Note 1: Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTF is a bidirectional I/O port.
RF0/AN5	18			
RF0		I/O	ST	Digital I/O.
AN5		I	Analog	Analog input 5.
RF1/AN6/C2OUT	17			
RF1		I/O	ST	Digital I/O.
AN6		I	Analog	Analog input 6.
C2OUT		O	—	Comparator 2 output.
RF2/AN7/C1OUT	16			
RF2		I/O	ST	Digital I/O.
AN7		I	Analog	Analog input 7.
C1OUT		O	—	Comparator 1 output.
RF3/AN8	15			
RF3		I/O	ST	Digital I/O.
AN8		I	Analog	Analog input 8.
RF4/AN9	14			
RF4		I/O	ST	Digital I/O.
AN9		I	Analog	Analog input 9.
RF5/AN10/CVREF	13			
RF5		I/O	ST	Digital I/O.
AN10		I	Analog	Analog input 10.
CVREF		O	Analog	Comparator reference voltage output.
RF6/AN11	12			
RF6		I/O	ST	Digital I/O.
AN11		I	Analog	Analog input 11.
RF7/$\overline{SS1}$	11			
RF7		I/O	ST	Digital I/O.
$\overline{SS1}$		I	TTL	SPI slave select input.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; I^2C™ = I^2C/SMBus input buffer

Note 1: Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/INT0/FLT0	58			
RB0		I/O	TTL	Digital I/O.
INT0		I	ST	External interrupt 0.
FLT0		I	ST	PWM Fault input for ECCPx.
RB1/INT1	57			
RB1		I/O	TTL	Digital I/O.
INT1		I	ST	External interrupt 1.
RB2/INT2	56			
RB2		I/O	TTL	Digital I/O.
INT2		I	ST	External interrupt 2.
RB3/INT3/ECCP2/P2A	55			
RB3		I/O	TTL	Digital I/O.
INT3		I	ST	External interrupt 3.
ECCP2(1)		O	—	Enhanced Capture 2 input/Compare 2 output/ PWM2 output.
P2A(1)		O	—	ECCP2 PWM output A.
RB4/KBI0	54			
RB4		I/O	TTL	Digital I/O.
KBI0		I	TTL	Interrupt-on-change pin.
RB5/KBI1/PGM	53			
RB5		I/O	TTL	Digital I/O.
KBI1		I	TTL	Interrupt-on-change pin.
PGM		I/O	ST	Low-Voltage ICSP™ Programming enable pin.
RB6/KBI2/PGC	52			
RB6		I/O	TTL	Digital I/O.
KBI2		I	TTL	Interrupt-on-change pin.
PGC		I/O	ST	In-Circuit Debugger and ICSP™ programming clock pin.
RB7/KBI3/PGD	47			
RB7		I/O	TTL	Digital I/O.
KBI3		I	TTL	Interrupt-on-change pin.
PGD		I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; I^2C™/SMB = I^2C/SMBus input buffer

Note 1: Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).

2: Default assignment for ECCP2 in all operating modes (CCP2MX is set).

3: Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

4: Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

5: Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTD is a bidirectional I/O port.
RD0/AD0/PSP0	72			
RD0		I/O	ST	Digital I/O.
AD0		I/O	TTL	External memory address/data 0.
PSP0		I/O	TTL	Parallel Slave Port data.
RD1/AD1/PSP1	69			
RD1		I/O	ST	Digital I/O.
AD1		I/O	TTL	External memory address/data 1.
PSP1		I/O	TTL	Parallel Slave Port data.
RD2/AD2/PSP2	68			
RD2		I/O	ST	Digital I/O.
AD2		I/O	TTL	External memory address/data 2.
PSP2		I/O	TTL	Parallel Slave Port data.
RD3/AD3/PSP3	67			
RD3		I/O	ST	Digital I/O.
AD3		I/O	TTL	External memory address/data 3.
PSP3		I/O	TTL	Parallel Slave Port data.
RD4/AD4/PSP4/SDO2	66			
RD4		I/O	ST	Digital I/O.
AD4		I/O	TTL	External memory address/data 4.
PSP4		I/O	TTL	Parallel Slave Port data.
SDO2		O	—	SPI data out.
RD5/AD5/PSP5/ SDI2/SDA2	65			
RD5		I/O	ST	Digital I/O.
AD5		I/O	TTL	External memory address/data 5.
PSP5		I/O	TTL	Parallel Slave Port data.
SDI2		I	ST	SPI data in.
SDA2		I/O	I^2C/SMB	I^2C™ data I/O.
RD6/AD6/PSP6/ SCK2/SCL2	64			
RD6		I/O	ST	Digital I/O.
AD6		I/O	TTL	External memory address/data 6.
PSP6		I/O	TTL	Parallel Slave Port data.
SCK2		I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL2		I/O	I^2C/SMB	Synchronous serial clock input/output for I^2C mode.
RD7/AD7/PSP7/$\overline{SS2}$	63			
RD7		I/O	ST	Digital I/O.
AD7		I/O	TTL	External memory address/data 7.
PSP7		I/O	TTL	Parallel Slave Port data.
$\overline{SS2}$		I	TTL	SPI slave select input.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; I^2C™/SMB = I^2C/SMBus input buffer

Note 1: Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).

2: Default assignment for ECCP2 in all operating modes (CCP2MX is set).

3: Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

4: Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

5: Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

2.1 A/D Acquisition Requirements

For the A/D Converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 2-3. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor, CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 2.5 kΩ**. After the analog input channel is selected (changed), the channel must be sampled for at least the minimum acquisition time before starting a conversion.

Note:	When the conversion is started, the holding capacitor is disconnected from the input pin.

To calculate the minimum acquisition time, Equation 2-1 may be used. This equation assumes that 1/2 LSb error is used (4096 steps for the 12-bit A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

Example 2-3 shows the calculation of the minimum required acquisition time, TACQ. This calculation is based on the following application system assumptions:

CHOLD	=	25 pF
Rs	=	2.5 kΩ
Conversion Error	≤	1/2 LSb
VDD	=	3V → Rss = 4 kΩ
Temperature	=	85°C (system max.)

EQUATION 2-1: ACQUISITION TIME

$$T_{ACQ} = \text{Amplifier Settling Time} + \text{Holding Capacitor Charging Time} + \text{Temperature Coefficient}$$
$$= T_{AMP} + T_C + T_{COFF}$$

EQUATION 2-2: A/D MINIMUM CHARGING TIME

$$V_{HOLD} = (V_{REF} - (V_{REF}/4096)) \cdot (1 - e^{(-T_C/C_{HOLD}(R_{IC} + R_{SS} + R_S))})$$
or
$$T_C = -(C_{HOLD})(R_{IC} + R_{SS} + R_S) \ln(1/4096)$$

EQUATION 2-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

$$T_{ACQ} = T_{AMP} + T_C + T_{COFF}$$
$$T_{AMP} = 0.2\ \mu s$$
$$T_{COFF} = (\text{Temp} - 25°C)(0.02\ \mu s/°C)$$
$$(85°C - 25°C)(0.02\ \mu s/°C)$$
$$1.2\ \mu s$$

Temperature coefficient is only required for temperatures > 25°C. Below 25°C, $T_{COFF} = 0\ \mu s$.

$$T_C = -(C_{HOLD})(R_{IC} + R_{SS} + R_S) \ln(1/4096)\ \mu s$$
$$-(25\ pF)\ (1\ k\Omega + 4\ k\Omega + 2.5\ k\Omega) \ln(0.0002441)\ \mu s$$
$$1.56\ \mu s$$

$$T_{ACQ} = 0.2\ \mu s + 1.56\ \mu s + 1.2\ \mu s$$
$$2.96\ \mu s$$

3.0 SPECIAL FEATURES OF THE CPU

Note: For additional details on the Configuration bits, refer to **Section 25.1 "Configuration Bits" in** the *"PIC18F8722 Family Data Sheet"* (DS39646). Device ID information presented in this section is for the PIC18F8723 family only.

PIC18F8723 family devices include several features intended to maximize reliability and minimize cost through elimination of external components. These include:

- Device ID Registers

3.1 Device ID Registers

The Device ID registers are "read-only" registers. They identify the device type and revision to device programmers and can be read by firmware using table reads.

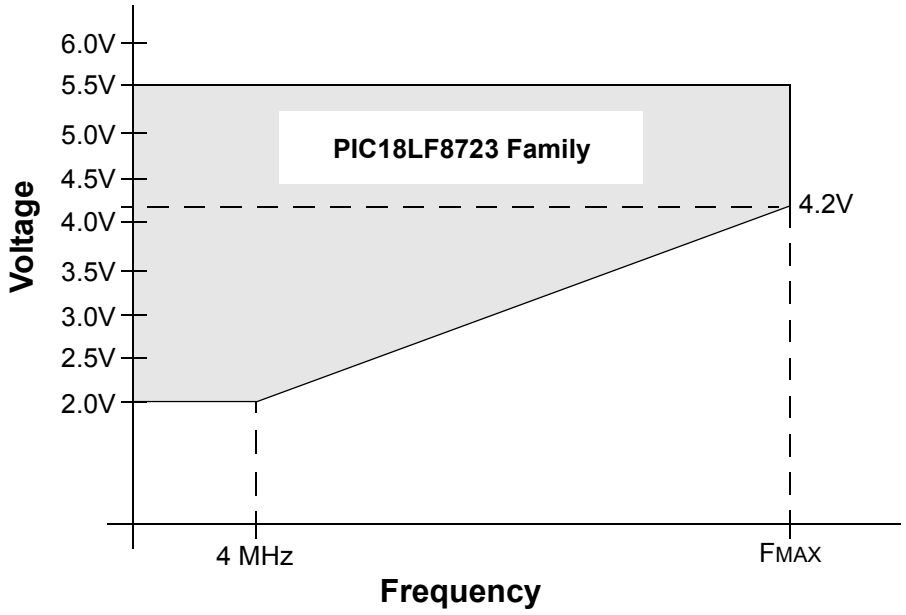
TABLE 3-1: DEVICE IDs

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
3FFFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx(1)
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	xxxx xxxx(1)

Legend: x = unknown

Note 1: See Register 3-1 and Register 3-2 for DEVID values. DEVID registers are read-only and cannot be programmed by the user.

FIGURE 4-3: PIC18LF8723 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



In 8-Bit External Memory mode:
F_{MAX} = (9.55 MHz/V) ($V_{DDAPPMIN}$ – 2.0V) + 4 MHz, if $V_{DDAPPMIN} \leq$ 4.2V;
F_{MAX} = 25 MHz, if $V_{DDAPPMIN}$ > 4.2V.

In all other modes:
F_{MAX} = (16.36 MHz/V) ($V_{DDAPPMIN}$ – 2.0V) + 4 MHz;
F_{MAX} = 40 MHz, if $V_{DDAPPMIN}$ > 4.2V.

Note: $V_{DDAPPMIN}$ is the minimum voltage of the PIC® device in the application.

TABLE 4-1: A/D CONVERTER CHARACTERISTICS: PIC18F8723 FAMILY (INDUSTRIAL)

Param No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions	
A01	NR	Resolution	—	—	12	bit		ΔVREF ≥ 3.0V
A03	EIL	Integral Linearity Error	—	<±1	±2.0	LSB	VDD = 3.0V	ΔVREF ≥ 3.0V
			—	—	±2.0	LSB	VDD = 5.0V	
A04	EDL	Differential Linearity Error	—	<±1	+1.5/-1.0	LSB	VDD = 3.0V	ΔVREF ≥ 3.0V
			—	—	+1.5/-1.0	LSB	VDD = 5.0V	
A06	EOFF	Offset Error	—	<±1	±5	LSB	VDD = 3.0V	ΔVREF ≥ 3.0V
			—	—	±3	LSB	VDD = 5.0V	
A07	EGN	Gain Error	—	<±1	±1.25	LSB	VDD = 3.0V	ΔVREF ≥ 3.0V
			—	—	±2.00	LSB	VDD = 5.0V	
A10	—	Monotonicity	Guaranteed(1)			—		VSS ≤ VAIN ≤ VREF
A20	ΔVREF	Reference Voltage Range (VREFH – VREFL)	3	—	VDD – VSS	V		For 12-bit resolution
A21	VREFH	Reference Voltage High	VSS + 3.0V	—	VDD + 0.3V	V		For 12-bit resolution
A22	VREFL	Reference Voltage Low	VSS – 0.3V	—	VDD – 3.0V	V		For 12-bit resolution
A25	VAIN	Analog Input Voltage	VREFL	—	VREFH	V		
A30	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	2.5	kΩ		
A50	IREF	VREF Input Current(2)	— —	— —	5 150	μA μA		During VAIN acquisition. During A/D conversion cycle.

Note 1: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

2: VREFH current is from the RA3/AN3/VREF+ pin or VDD, whichever is selected as the VREFH source. VREFL current is from the RA2/AN2/VREF-/CVREF pin or VSS, whichever is selected as the VREFL source.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (August 2007)

Original data sheet for the PIC18F8723 family of devices.

Revision B (October 2009)

Updated to remove Preliminary status.

APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

TABLE B-1: PIC18F8723 FAMILY DEVICE DIFFERENCES

Features	PIC18F6628	PIC18F6723	PIC18F8628	PIC18F8723
Program Memory (Bytes)	96K	128K	96K	128K
Program Memory (Instructions)	49152	65536	49152	65536
Interrupt Sources	28	28	29	29
I/O Ports	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G, H, J	Ports A, B, C, D, E, F, G, H, J
Capture/Compare/PWM Modules	2	2	2	2
Enhanced Capture/Compare/PWM Modules	3	3	3	3
Parallel Communications (PSP)	Yes	Yes	Yes	Yes
External Memory Bus	No	No	Yes	Yes
12-Bit Analog-to-Digital Module	12 Input Channels	12 Input Channels	16 Input Channels	16 Input Channels
Packages	64-Pin TQFP	64-Pin TQFP	80-Pin TQFP	80-Pin TQFP

APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

Not Applicable

APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

Not Currently Available

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Device: PIC18F8723 Family Literature Number: DS39894B

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

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4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

PIC18F8723 FAMILY PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device[1) (2)]	PIC18F6628/6723, PIC18F8628/8723, VDD range 4.2V to 5.5V PIC18LF6628/6723, PIC18LF6628/6723(VDD range 2.0V to 5.5V
Temperature Range	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)
Package	PT = TQFP (Thin Quad Flatpack)
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)

Examples:

a) PIC18LF6723-I/PT 301 = Industrial temp., TQFP package, Extended VDD limits, QTP pattern #301.

b) PIC18F6723-E/PT = Extended temp., TQFP package, standard VDD limits.

Note 1: F = Standard Voltage Range
LF = Wide Voltage Range
2: T = in tape and reel TQFP packages only.