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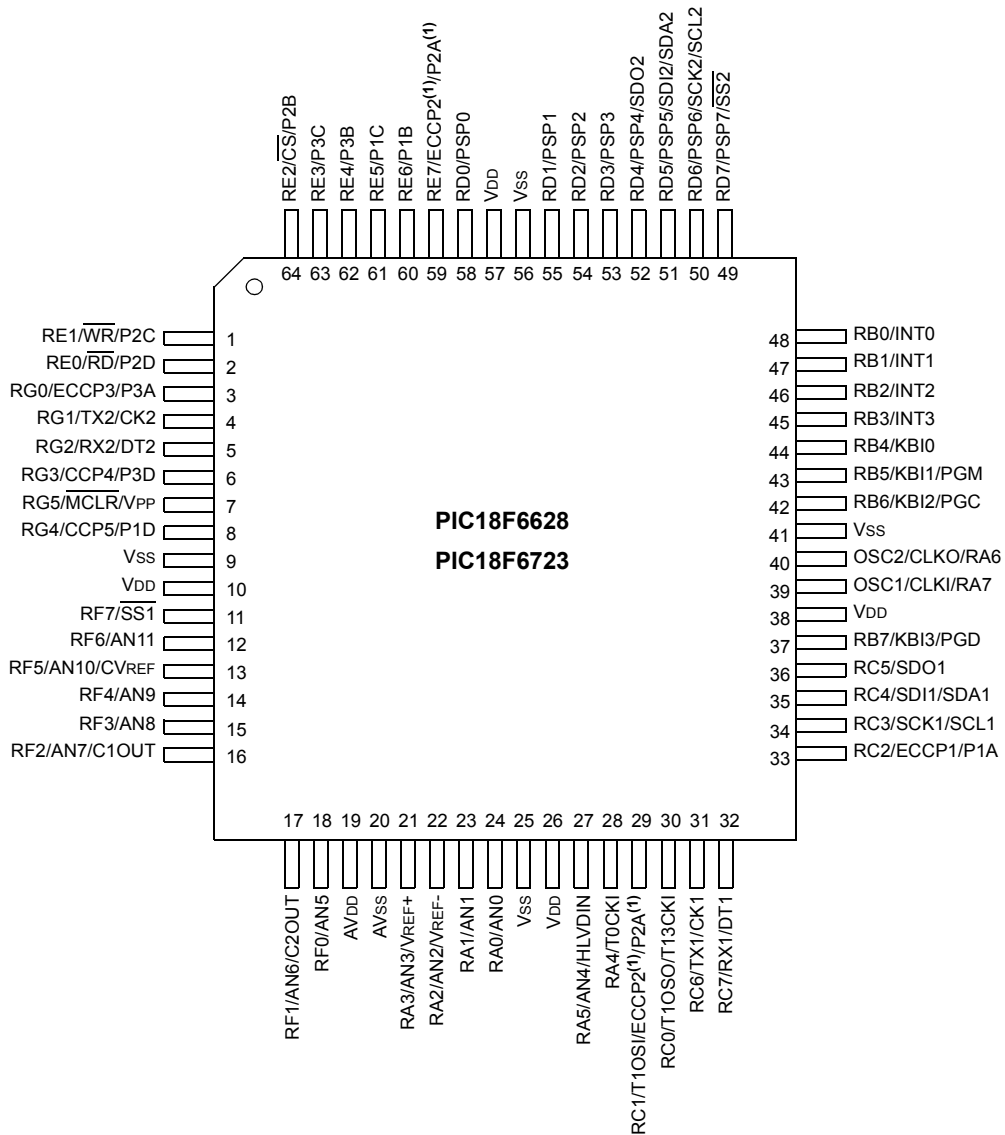
Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf6723t-i-pt

PIC18F8723

Pin Diagrams

64-Pin TQFP



Note 1: The ECCP2/P2A pin placement is determined by the CCP2MX Configuration bit.

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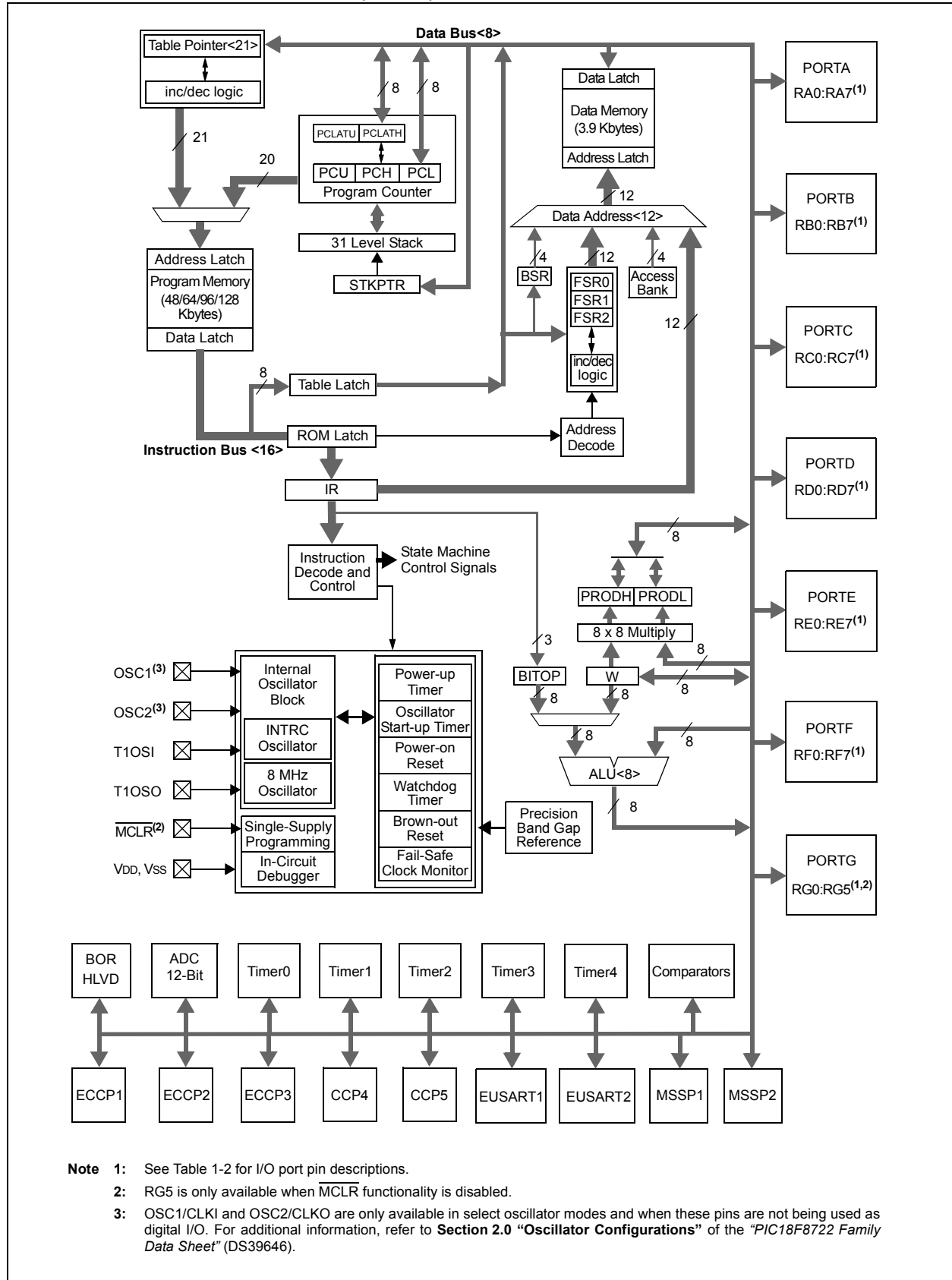
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PIC18F8723

NOTES:

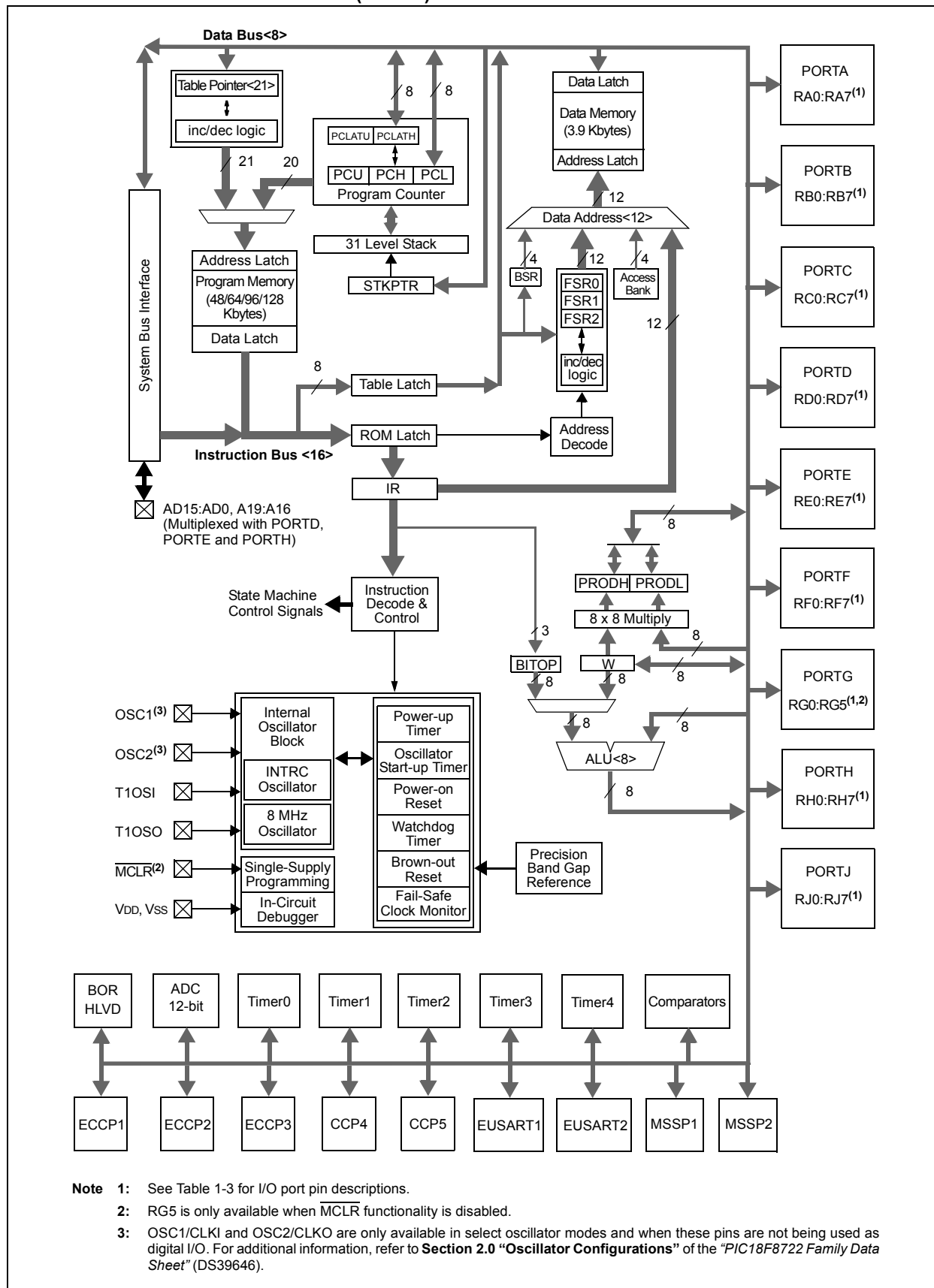
PIC18F8723 FAMILY

FIGURE 1-1: PIC18F6628/6723 (64-PIN) BLOCK DIAGRAM



PIC18F8723 FAMILY

FIGURE 1-2: PIC18F8628/8723 (80-PIN) BLOCK DIAGRAM



PIC18F8723 FAMILY

TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RG5/ <u>MCLR</u> /VPP RG5 <u>MCLR</u> VPP	7	I I P	ST ST 	Master Clear (input) or programming voltage (input). Digital input. Master Clear (Reset) input. This pin is an active-low Reset to the device. Programming voltage input.
OSC1/CLKI/RA7 OSC1 CLKI RA7	39	I I I/O	ST CMOS TTL	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode, CMOS otherwise. External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) General purpose I/O pin.
OSC2/CLKO/RA6 OSC2 CLKO RA6	40	O O I/O	— — TTL	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. General purpose I/O pin.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C™ = I²C/SMBus input buffer

Note 1: Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

PIC18F8723 FAMILY

TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RC0/T1OSO/T13CKI	30	I/O	ST	PORTC is a bidirectional I/O port. Digital I/O. Timer1 oscillator output. Timer1/Timer3 external clock input.
RC0		O	—	
T1OSO		I	ST	
RC1/T1OSI/ECCP2/P2A	29	I/O	ST	Digital I/O. Timer1 oscillator input. Enhanced Capture 2 input/Compare 2 output/ PWM2 output. ECCP2 PWM output A.
RC1		I	CMOS	
T1OSI		I/O	ST	
ECCP2 ⁽¹⁾		O	—	
P2A ⁽¹⁾		O	—	
RC2/ECCP1/P1A	33	I/O	ST	Digital I/O. Enhanced Capture 1 input/Compare 1 output/ PWM1 output. ECCP1 PWM output A.
RC2		I/O	ST	
ECCP1		O	—	
P1A		O	—	
RC3/SCK1/SCL1	34	I/O	ST	Digital I/O. Synchronous serial clock input/output for SPI mode. Synchronous serial clock input/output for I ² C™ mode.
RC3		I/O	ST	
SCK1		I/O	ST	
SCL1		I/O	ST	
RC4/SDI1/SDA1	35	I/O	ST	Digital I/O. SPI data in. I ² C data I/O.
RC4		I	ST	
SDI1		I/O	ST	
SDA1		I/O	ST	
RC5/SDO1	36	I/O	ST	Digital I/O. SPI data out.
RC5		O	—	
SDO1		O	—	
RC6/TX1/CK1	31	I/O	ST	Digital I/O. EUSART1 asynchronous transmit. EUSART1 synchronous clock (see related RX1/DT1).
RC6		O	—	
TX1		I/O	ST	
CK1		I/O	ST	
RC7/RX1/DT1	32	I/O	ST	Digital I/O. EUSART1 asynchronous receive. EUSART1 synchronous data (see related TX1/CK1).
RC7		I	ST	
RX1		I/O	ST	
DT1		I/O	ST	

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C™ = I²C/SMBus input buffer

Note 1: Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

PIC18F8723 FAMILY

TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RG5/MCLR/VPP RG5 MCLR VPP	9	I I P	ST ST 	Master Clear (input) or programming voltage (input). Digital input. Master Clear (Reset) input. This pin is an active-low Reset to the device. Programming voltage input.
OSC1/CLKI/RA7 OSC1 CLKI RA7	49	I I I/O	ST CMOS TTL	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode, CMOS otherwise. External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) General purpose I/O pin.
OSC2/CLKO/RA6 OSC2 CLKO RA6	50	O O I/O	— — TTL	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. General purpose I/O pin.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C™/SMB = I²C/SMBus input buffer

- Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).
- 2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).
- 3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).
- 4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).
- 5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

PIC18F8723 FAMILY

TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RJ0/ALE RJ0 ALE	62	I/O O	ST —	PORTJ is a bidirectional I/O port. Digital I/O. External memory address latch enable.
RJ1/ $\overline{\text{OE}}$ RJ1 $\overline{\text{OE}}$	61	I/O O	ST —	Digital I/O. External memory output enable.
RJ2/ $\overline{\text{WRL}}$ RJ2 $\overline{\text{WRL}}$	60	I/O O	ST —	Digital I/O. External memory write low control.
RJ3/ $\overline{\text{WRH}}$ RJ3 $\overline{\text{WRH}}$	59	I/O O	ST —	Digital I/O. External memory write high control.
RJ4/BA0 RJ4 BA0	39	I/O O	ST —	Digital I/O. External memory byte address 0 control.
RJ5/ $\overline{\text{CE}}$ RJ4 $\overline{\text{CE}}$	40	I/O O	ST —	Digital I/O External memory chip enable control.
RJ6/ $\overline{\text{LB}}$ RJ6 $\overline{\text{LB}}$	41	I/O O	ST —	Digital I/O. External memory low byte control.
RJ7/ $\overline{\text{UB}}$ RJ7 $\overline{\text{UB}}$	42	I/O O	ST —	Digital I/O. External memory high byte control.
Vss	11, 31, 51, 70	P	—	Ground reference for logic and I/O pins.
VDD	12, 32, 48, 71	P	—	Positive supply for logic and I/O pins.
AVss	26	P	—	Ground reference for analog modules.
AVDD	25	P	—	Positive supply for analog modules.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I²C™/SMB = I²C/SMBus input buffer

- Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).
2: Default assignment for ECCP2 in all operating modes (CCP2MX is set).
3: Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).
4: Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).
5: Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

2.0 12-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module has 12 inputs for the 64-pin devices (PIC18F6628/6723) and 16 for the 80-pin devices (PIC18F8628/8723). This module allows conversion of an analog input signal to a corresponding 12-bit digital number.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

The ADCON0 register, shown in Register 2-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 2-2, configures the functions of the port pins. The ADCON2 register, shown in Register 2-3, configures the A/D clock source, programmed acquisition time and justification.

REGISTER 2-1: ADCON0: A/D CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHS3:CHS0:** Analog Channel Select bits

0000 = Channel 0 (AN0)
 0001 = Channel 1 (AN1)
 0010 = Channel 2 (AN2)
 0011 = Channel 3 (AN3)
 0100 = Channel 4 (AN4)
 0101 = Channel 5 (AN5)
 0110 = Channel 6 (AN6)
 0111 = Channel 7 (AN7)
 1000 = Channel 8 (AN8)
 1001 = Channel 9 (AN9)
 1010 = Channel 10 (AN10)
 1011 = Channel 11 (AN11)
 1100 = Channel 12 (AN12)^(1,2)
 1101 = Channel 13 (AN13)^(1,2)
 1110 = Channel 14 (AN14)^(1,2)
 1111 = Channel 15 (AN15)^(1,2)

bit 1 **GO/DONE:** A/D Conversion Status bit

When ADON = 1:

1 = A/D conversion in progress

0 = A/D Idle

bit 0 **ADON:** A/D On bit

1 = A/D Converter module is enabled

0 = A/D Converter module is disabled

Note 1: These channels are not implemented on PIC18F6628/6723 devices.

2: Performing a conversion on unimplemented channels will return a floating input measurement.

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REGISTER 2-3: ADCON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **ADFM:** A/D Result Format Select bit

1 = Right justified

0 = Left justified

bit 6 **Unimplemented:** Read as '0'

bit 5-3 **ACQT2:ACQT0:** A/D Acquisition Time Select bits

111 = 20 TAD

110 = 16 TAD

101 = 12 TAD

100 = 8 TAD

011 = 6 TAD

010 = 4 TAD

001 = 2 TAD

000 = 0 TAD⁽¹⁾

bit 2-0 **ADCS2:ADCS0:** A/D Conversion Clock Select bits

111 = FRC (clock derived from A/D RC oscillator)⁽¹⁾

110 = FOSC/64

101 = FOSC/16

100 = FOSC/4

011 = FRC (clock derived from A/D RC oscillator)⁽¹⁾

010 = FOSC/32

001 = FOSC/8

000 = FOSC/2

Note 1: If the A/D FRC clock source is selected, a delay of one T_{CY} (instruction cycle) is added before the A/D clock starts. This allows the **SLEEP** instruction to be executed before starting a conversion.

PIC18F8723 FAMILY

The analog reference voltage is software selectable to either the device's positive and negative supply voltage (VDD and VSS), or the voltage level on the RA3/AN3/VREF+ and RA2/AN2/VREF-/CVREF pins.

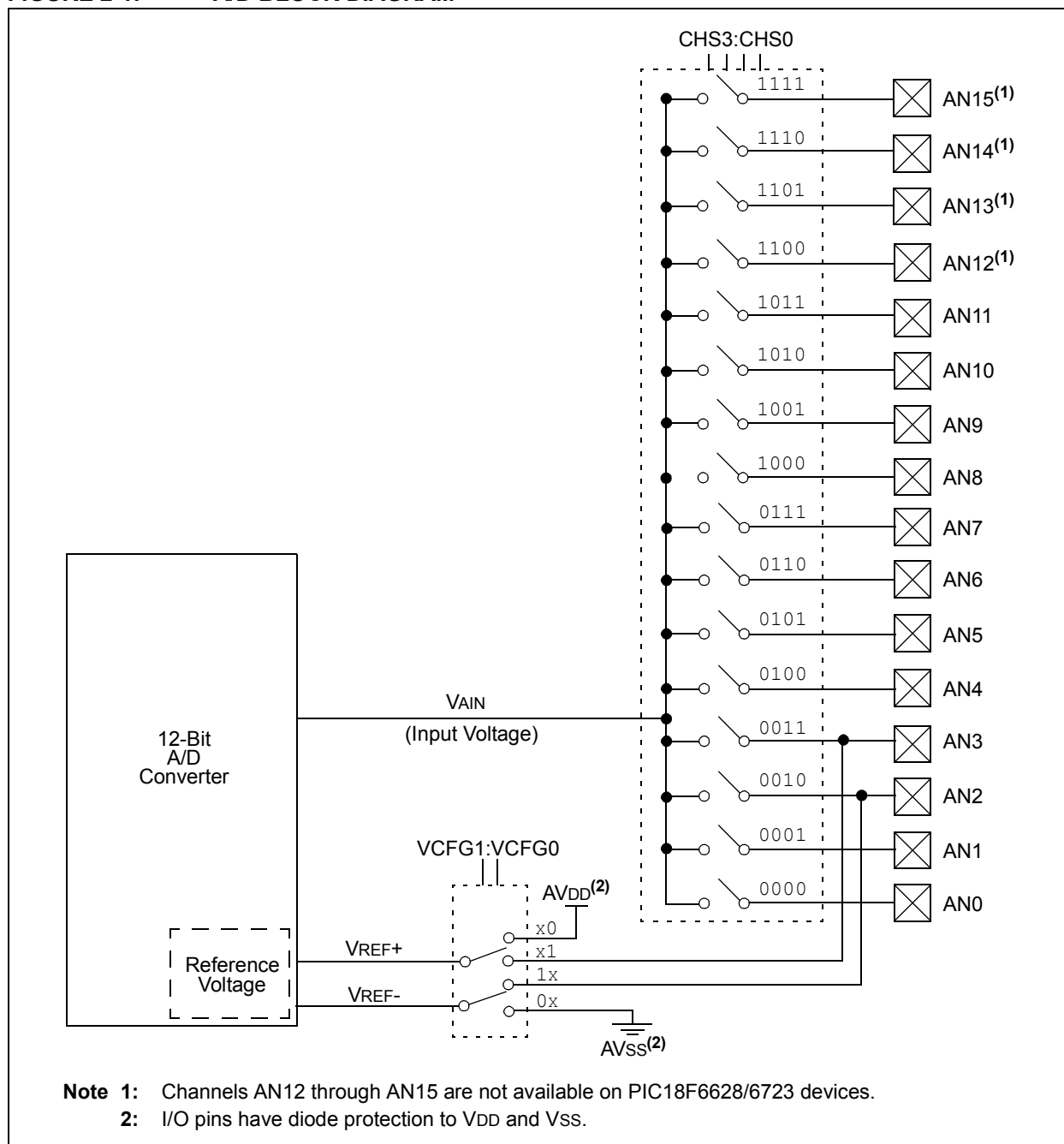
The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D Converter can be configured as an analog input or a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/DONE bit (ADCON0<1>) is cleared and the A/D Interrupt Flag bit, ADIF, is set. The block diagram of the A/D module is shown in Figure 2-1.

FIGURE 2-1: A/D BLOCK DIAGRAM



PIC18F8723 FAMILY

2.1 A/D Acquisition Requirements

For the A/D Converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 2-3. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor, CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 2.5 kΩ.** After the analog input channel is selected (changed), the channel must be sampled for at least the minimum acquisition time before starting a conversion.

Note: When the conversion is started, the holding capacitor is disconnected from the input pin.

To calculate the minimum acquisition time, Equation 2-1 may be used. This equation assumes that 1/2 LSB error is used (4096 steps for the 12-bit A/D). The 1/2 LSB error is the maximum error allowed for the A/D to meet its specified resolution.

Example 2-3 shows the calculation of the minimum required acquisition time, TACQ. This calculation is based on the following application system assumptions:

CHOLD	=	25 pF
Rs	=	2.5 kΩ
Conversion Error	≤	1/2 LSB
VDD	=	3V → Rss = 4 kΩ
Temperature	=	85°C (system max.)

EQUATION 2-1: ACQUISITION TIME

$$\begin{aligned} \text{TACQ} &= \text{Amplifier Settling Time} + \text{Holding Capacitor Charging Time} + \text{Temperature Coefficient} \\ &= \text{TAMP} + \text{TC} + \text{Tcoff} \end{aligned}$$

EQUATION 2-2: A/D MINIMUM CHARGING TIME

$$\begin{aligned} \text{V}_{\text{HOLD}} &= (\text{V}_{\text{REF}} - (\text{V}_{\text{REF}}/4096)) \cdot (1 - e^{-(\text{TC}/\text{CHOLD})(\text{RIC} + \text{RSS} + \text{RS})}) \\ \text{or} \\ \text{TC} &= -(\text{CHOLD})(\text{RIC} + \text{RSS} + \text{RS}) \ln(1/4096) \end{aligned}$$

EQUATION 2-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

$$\begin{aligned} \text{TACQ} &= \text{TAMP} + \text{TC} + \text{Tcoff} \\ \text{TAMP} &= 0.2 \mu\text{s} \\ \text{Tcoff} &= (\text{Temp} - 25^\circ\text{C})(0.02 \mu\text{s}/^\circ\text{C}) \\ &\quad (85^\circ\text{C} - 25^\circ\text{C})(0.02 \mu\text{s}/^\circ\text{C}) \\ &\quad 1.2 \mu\text{s} \end{aligned}$$

Temperature coefficient is only required for temperatures > 25°C. Below 25°C, Tcoff = 0 μs.

$$\begin{aligned} \text{TC} &= -(\text{CHOLD})(\text{RIC} + \text{RSS} + \text{RS}) \ln(1/4096) \mu\text{s} \\ &\quad -(25 \text{ pF})(1 \text{ k}\Omega + 4 \text{ k}\Omega + 2.5 \text{ k}\Omega) \ln(0.0002441) \mu\text{s} \\ &\quad 1.56 \mu\text{s} \\ \text{TACQ} &= 0.2 \mu\text{s} + 1.56 \mu\text{s} + 1.2 \mu\text{s} \\ &\quad 2.96 \mu\text{s} \end{aligned}$$

2.2 Selecting and Configuring Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set. It also gives users the option to use an automatically determined acquisition time.

Acquisition time may be set with the ACQT2:ACQT0 bits (ADCON2<5:3>), which provide a range of 2 to 20 TAD. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

Manual acquisition is selected when ACQT2:ACQT0 = 000. When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This option is also the default Reset state of the ACQT2:ACQT0 bits and is compatible with devices that do not offer programmable acquisition times.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

2.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 13 TAD per 12-bit conversion. The source of the A/D conversion clock is software selectable. There are seven possible options for TAD:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible, but greater than the minimum TAD (see parameter 130 for more information).

Table 2-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

TABLE 2-1: TAD vs. DEVICE OPERATING FREQUENCIES

A/D Clock Source (TAD)		Assumes TAD Min. = 0.8 μ s
Operation	ADCS2:ADCS0	Maximum Fosc
2 TOSC	000	2.50 MHz
4 TOSC	100	5.00 MHz
8 TOSC	001	10.00 MHz
16 TOSC	101	20.00 MHz
32 TOSC	010	40.00 MHz
64 TOSC	110	40.00 MHz
RC ⁽¹⁾	x11	1.00 MHz ⁽²⁾

Note 1: The RC source has a typical TAD time of 2.5 μ s.

2: For device frequencies above 1 MHz, the device must be in Sleep for the entire conversion or a FOSC divider should be used instead; otherwise, the A/D accuracy specification may not be met.

2.6 A/D Conversions

Figure 2-4 shows the operation of the A/D Converter after the $\overline{\text{GO/DONE}}$ bit has been set and the ACQT2:ACQT0 bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

Figure 2-5 shows the operation of the A/D Converter after the $\overline{\text{GO/DONE}}$ bit has been set, the ACQT2:ACQT0 bits are set to '010' and a 4 TAD acquisition time has been selected before the conversion starts.

Clearing the $\overline{\text{GO/DONE}}$ bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. This means the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers).

After the A/D conversion is completed or aborted, a 2 T_{CY} wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

Note: The $\overline{\text{GO/DONE}}$ bit should **NOT** be set in the same instruction that turns on the A/D. Code should wait at least 2 μs after enabling the A/D before beginning an acquisition and conversion cycle.

2.7 Discharge

The discharge phase is used to initialize the value of the holding capacitor. The array is discharged before every sample. This feature helps to optimize the unity gain amplifier, as the circuit always needs to charge the capacitor array, rather than charge/discharge based on previous measure values.

FIGURE 2-4: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 000, TACQ = 0)

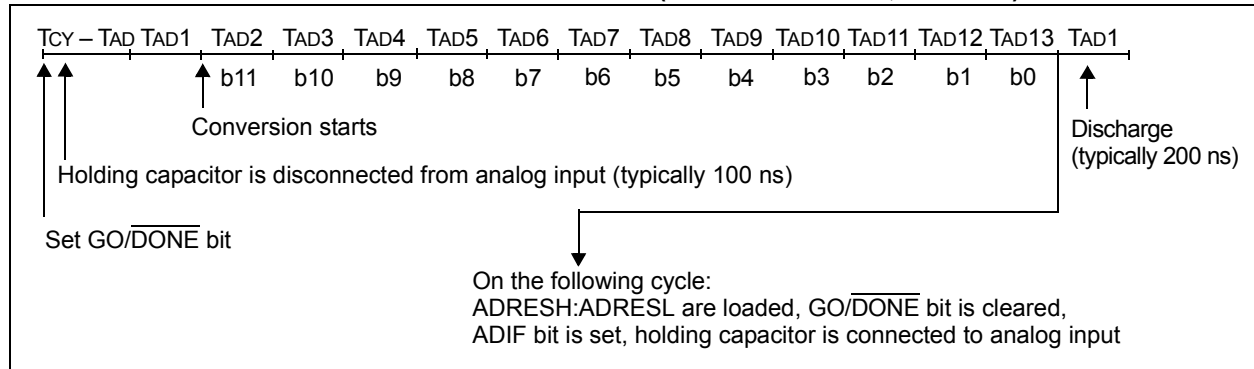
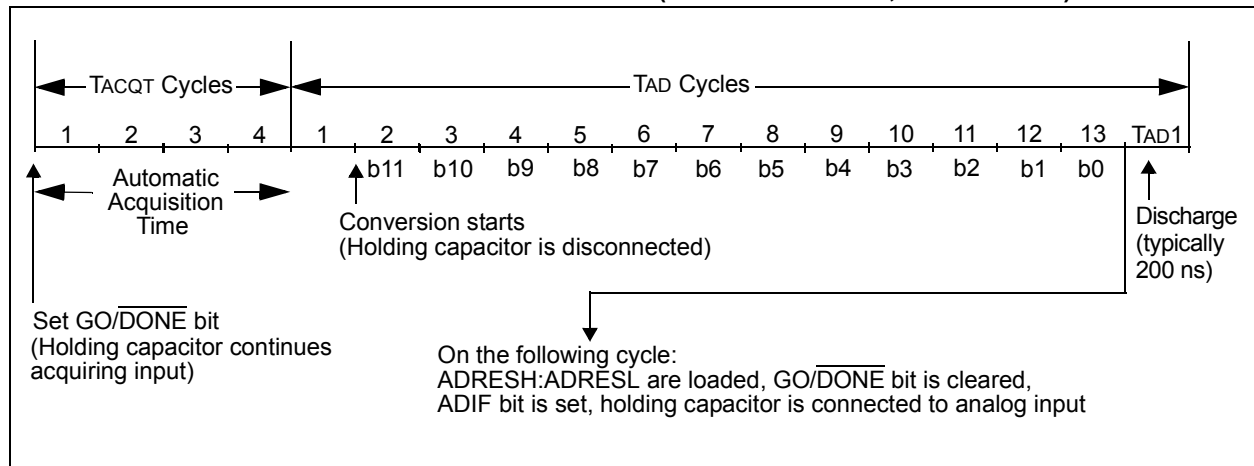


FIGURE 2-5: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 010, TACQ = 4 TAD)



PIC18F8723 FAMILY

TABLE 4-1: A/D CONVERTER CHARACTERISTICS: PIC18F8723 FAMILY (INDUSTRIAL)

Param No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions	
A01	NR	Resolution	—	—	12	bit		$\Delta V_{REF} \geq 3.0V$
A03	EIL	Integral Linearity Error	—	$<\pm 1$	± 2.0	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	± 2.0	LSB	$V_{DD} = 5.0V$	
A04	EDL	Differential Linearity Error	—	$<\pm 1$	$+1.5/-1.0$	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	$+1.5/-1.0$	LSB	$V_{DD} = 5.0V$	
A06	EOFF	Offset Error	—	$<\pm 1$	± 5	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	± 3	LSB	$V_{DD} = 5.0V$	
A07	EGN	Gain Error	—	$<\pm 1$	± 1.25	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	± 2.00	LSB	$V_{DD} = 5.0V$	
A10	—	Monotonicity	Guaranteed ⁽¹⁾			—		$V_{SS} \leq V_{AIN} \leq V_{REF}$
A20	ΔV_{REF}	Reference Voltage Range ($V_{REFH} - V_{REFL}$)	3	—	$V_{DD} - V_{SS}$	V		For 12-bit resolution
A21	V_{REFH}	Reference Voltage High	$V_{SS} + 3.0V$	—	$V_{DD} + 0.3V$	V		For 12-bit resolution
A22	V_{REFL}	Reference Voltage Low	$V_{SS} - 0.3V$	—	$V_{DD} - 3.0V$	V		For 12-bit resolution
A25	V_{AIN}	Analog Input Voltage	V_{REFL}	—	V_{REFH}	V		
A30	Z_{AIN}	Recommended Impedance of Analog Voltage Source	—	—	2.5	k Ω		
A50	I_{REF}	V_{REF} Input Current ⁽²⁾	—	—	5	μA		During V_{AIN} acquisition. During A/D conversion cycle.
			—	—	150	μA		

Note 1: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

Note 2: V_{REFH} current is from the RA3/AN3/ V_{REF+} pin or V_{DD} , whichever is selected as the V_{REFH} source. V_{REFL} current is from the RA2/AN2/ V_{REF-}/V_{REF} pin or V_{SS} , whichever is selected as the V_{REFL} source.

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