Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	70
Program Memory Size	96KB (48K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf8628t-i-pt

PIC18F8723 FAMILY

64/80-Pin, 1-Mbit, Enhanced Flash Microcontrollers with 12-Bit A/D and nanoWatt Technology

Peripheral Highlights:

- 12-Bit, Up to 16-Channel Analog-to-Digital Converter module (A/D):
  - Auto-acquisition capability
  - Conversion available during Sleep
- Two Master Synchronous Serial Port (MSSP) modules supporting 2/3/4-Wire SPI (all four modes) and I²C™ Master and Slave modes
- Two Capture/Compare/PWM (CCP) modules
- Three Enhanced Capture/Compare/PWM (ECCP) modules:
  - One, two or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart
- Two Enhanced Addressable USART modules:
  - Supports RS-485, RS-232 and LIN 1.2
  - Auto-wake-up on Start bit
  - Auto-Baud Detect
- Dual Analog Comparators with Input Multiplexing
- High-Current Sink/Source 25 mA/25 mA
- Four Programmable External Interrupts
- Four Input Change Interrupts

External Memory Interface:

- Address Capability of Up to 2 Mbytes
- 8-Bit or 16-Bit Interface
- 8, 12, 16 and 20-Bit Address modes

Power-Managed Modes:

- Run: CPU on, Peripherals on
- Idle: CPU off, Peripherals on
- Sleep: CPU off, Peripherals off
- Idle mode Currents Down to 15 µA Typical
- Sleep Current Down to 0.2 µA Typical
- Timer1 Oscillator: 1.8 µA, 32 kHz, 2V
- Watchdog Timer: 2.1 µA
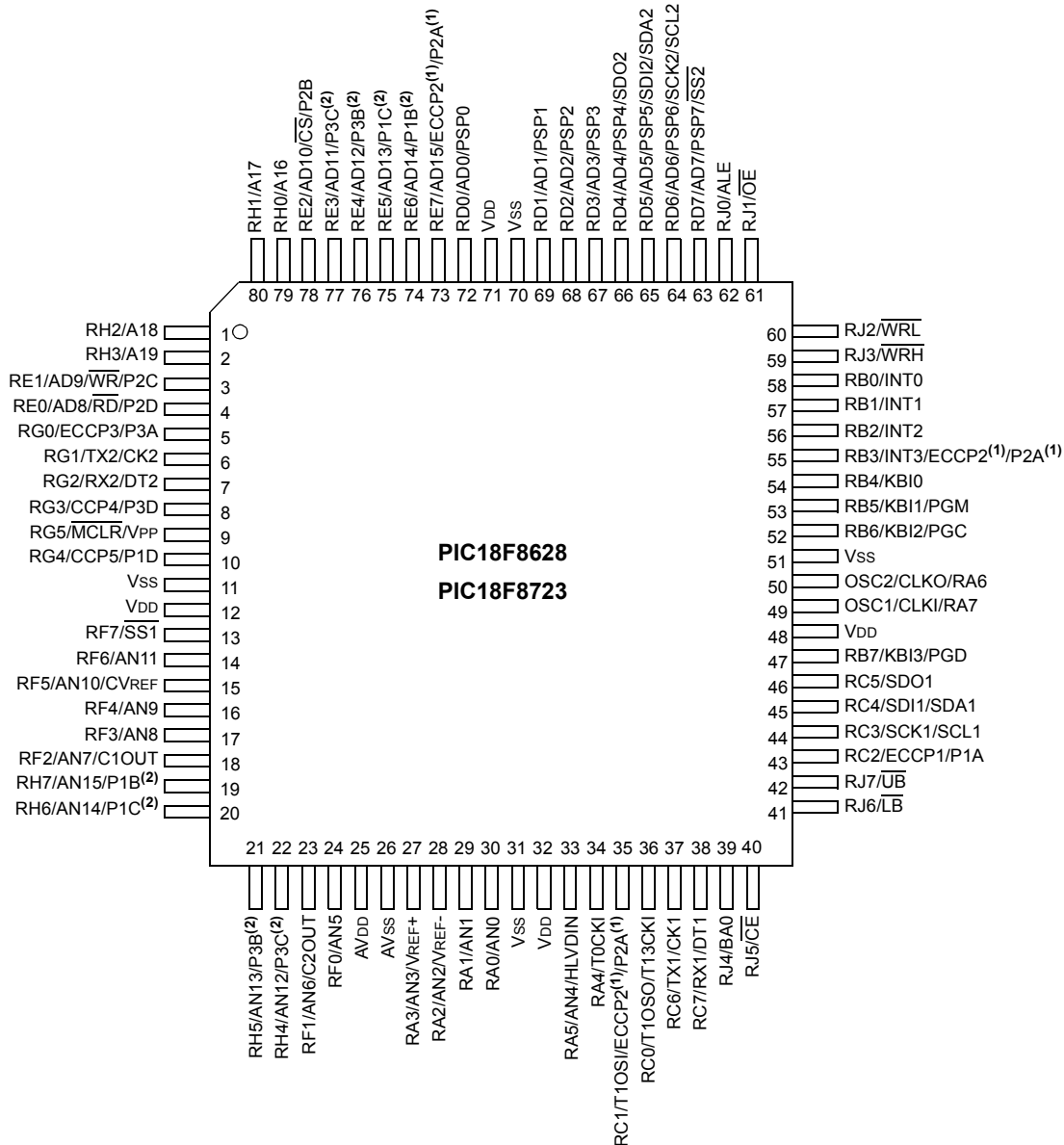
Special Microcontroller Features:

- C Compiler Optimized Architecture:
  - Optional extended instruction set designed to optimize re-entrant code
- 100,000 Erase/Write Cycle Enhanced Flash Program Memory Typical
- 1,000,000 Erase/Write Cycle Data EEPROM Memory Typical
- Flash/Data EEPROM Retention: 100 Years Typical
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 131s
- Single-Supply In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Wide Operating Voltage Range: 2.0V to 5.5V
- Fail-Safe Clock Monitor
- Two-Speed Oscillator Start-up
- nanoWatt Technology

> **Note:** This document is supplemented by the *"PIC18F8722 Family Data Sheet"* (DS39646). See **Section 1.0 "Device Overview"**.

Device	Program Memory		Data Memory		I/O	12-Bit A/D (ch)	CCP/ ECCP (PWM)	MSSP			EUSART	Comparators	Timers 8/16-Bit	External Bus
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)					SPI	Master I²C™				
PIC18F6628	96K	49152	3936	1024	54	12	2/3	2	Y	Y	2	2	2/3	N
PIC18F6723	128K	65536	3936	1024	54	12	2/3	2	Y	Y	2	2	2/3	N
PIC18F8628	96K	49152	3936	1024	70	16	2/3	2	Y	Y	2	2	2/3	Y
PIC18F8723	128K	65536	3936	1024	70	16	2/3	2	Y	Y	2	2	2/3	Y

Pin Diagrams (Continued)

80-Pin TQFP

Top pins (80 to 61):
- 80 RH1/A17
- 79 RH0/A16
- 78 RE2/AD10/$\overline{CS}$/P2B
- 77 RE3/AD11/P3C[2]
- 76 RE4/AD12/P3B[2]
- 75 RE5/AD13/P1C[2]
- 74 RE6/AD14/P1B[2]
- 73 RE7/AD15/ECCP2[1]/P2A[1]
- 72 RD0/AD0/PSP0
- 71 VDD
- 70 VSS
- 69 RD1/AD1/PSP1
- 68 RD2/AD2/PSP2
- 67 RD3/AD3/PSP3
- 66 RD4/AD4/PSP4/SDO2
- 65 RD5/AD5/PSP5/SDI2/SDA2
- 64 RD6/AD6/PSP6/SCK2/SCL2
- 63 RD7/AD7/PSP7/$\overline{SS2}$
- 62 RJ0/ALE
- 61 RJ1/$\overline{OE}$

Left pins (1 to 20):
- 1 RH2/A18
- 2 RH3/A19
- 3 RE1/AD9/$\overline{WR}$/P2C
- 4 RE0/AD8/$\overline{RD}$/P2D
- 5 RG0/ECCP3/P3A
- 6 RG1/TX2/CK2
- 7 RG2/RX2/DT2
- 8 RG3/CCP4/P3D
- 9 RG5/$\overline{MCLR}$/VPP
- 10 RG4/CCP5/P1D
- 11 VSS
- 12 VDD
- 13 RF7/$\overline{SS1}$
- 14 RF6/AN11
- 15 RF5/AN10/CVREF
- 16 RF4/AN9
- 17 RF3/AN8
- 18 RF2/AN7/C1OUT
- 19 RH7/AN15/P1B[2]
- 20 RH6/AN14/P1C[2]

Center label:
PIC18F8628
PIC18F8723

Right pins (60 to 41):
- 60 RJ2/$\overline{WRL}$
- 59 RJ3/$\overline{WRH}$
- 58 RB0/INT0
- 57 RB1/INT1
- 56 RB2/INT2
- 55 RB3/INT3/ECCP2[1]/P2A[1]
- 54 RB4/KBI0
- 53 RB5/KBI1/PGM
- 52 RB6/KBI2/PGC
- 51 VSS
- 50 OSC2/CLKO/RA6
- 49 OSC1/CLKI/RA7
- 48 VDD
- 47 RB7/KBI3/PGD
- 46 RC5/SDO1
- 45 RC4/SDI1/SDA1
- 44 RC3/SCK1/SCL1
- 43 RC2/ECCP1/P1A
- 42 RJ7/$\overline{UB}$
- 41 RJ6/$\overline{LB}$

Bottom pins (21 to 40):
- 21 RH5/AN13/P3B[2]
- 22 RH4/AN12/P3C[2]
- 23 RF1/AN6/C2OUT
- 24 RF0/AN5
- 25 AVDD
- 26 AVSS
- 27 RA3/AN3/VREF+
- 28 RA2/AN2/VREF-
- 29 RA1/AN1
- 30 RA0/AN0
- 31 VSS
- 32 VDD
- 33 RA5/AN4/HLVDIN
- 34 RA4/T0CKI
- 35 RC1/T1OSI/ECCP2[1]/P2A[1]
- 36 RC0/T1OSO/T13CKI
- 37 RC6/TX1/CK1
- 38 RC7/RX1/DT1
- 39 RJ4/BA0
- 40 RJ5/$\overline{CE}$

Note 1: The ECCP2/P2A pin placement is determined by the CCP2MX Configuration bit and Processor mode settings.
2: P1B, P1C, P3B and P3C pin placement is determined by the ECCPMX Configuration bit.

PIC18F8723

Table of Contents

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F6628
- PIC18LF6628
- PIC18F6723
- PIC18LF6723
- PIC18F8628
- PIC18LF8628
- PIC18F8723
- PIC18LF8723

> **Note:** This data sheet documents only the devices' features and specifications that are in addition to the features and specifications of the PIC18F8722 family devices. For information on the features and specifications shared by the PIC18F8723 family and PIC18F8722 family devices, see the *"PIC18F8722 Family Data Sheet"* (DS39646).

The PIC18F8723 family of devices offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high-endurance, Enhanced Flash program memory. In addition to these features, the PIC18F8723 introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power-sensitive applications.

1.1 Special Features

- **12-Bit A/D Converter:** The PIC18F8723 family implements a 12-bit A/D Converter. A/D Converters in both families incorporate programmable acquisition time. This allows for a channel to be selected and a conversion to be initiated, without waiting for a sampling period and thus, reducing code overhead.

1.2 Details on Individual Family Members

Devices in the PIC18F8723 family are available in 64-pin and 80-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in the following ways:

- Flash program memory (96 Kbytes for PIC18FX628 devices and 128 Kbytes for PIC18FX723).
- A/D channels (12 for PIC18F6628/6723 devices and 16 for PIC18F8628/8723 devices).
- I/O ports (seven bidirectional ports on PIC18F6628/6723 devices and nine bidirectional ports on PIC18F8628/8723 devices).
- External Memory Bus, configurable for 8 and 16-bit operation

All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1-2 and Table 1-3.

Like all Microchip PIC18 devices, members of the PIC18F8723 family are available as both standard and low-voltage devices. Standard devices with Enhanced Flash memory, designated with an "F" in the part number (such as PIC18**F**6628), accommodate an operating V_{DD} range of 4.2V to 5.5V. Low-voltage parts, designated by "LF" (such as PIC18**LF**6628), function over an extended V_{DD} range of 2.0V to 5.5V.

PIC18F8723 FAMILY

TABLE 1-1: DEVICE FEATURES

Features	PIC18F6628	PIC18F6723	PIC18F8628	PIC18F8723
Operating Frequency	DC – 40 MHz	DC – 40 MHz	DC – 40 MHz	DC – 40 MHz
Program Memory (Bytes)	96K	128K	96K	128K
Program Memory (Instructions)	49152	65536	49152	65536
Data Memory (Bytes)	3936	3936	3936	3936
Data EEPROM Memory (Bytes)	1024	1024	1024	1024
Interrupt Sources	28	28	29	29
I/O Ports	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G, H, J	Ports A, B, C, D, E, F, G, H, J
Timers	5	5	5	5
Capture/Compare/PWM Modules	2	2	2	2
Enhanced Capture/Compare/ PWM Modules	3	3	3	3
Enhanced USART	2	2	2	2
Serial Communications	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART
Parallel Communications (PSP)	Yes	Yes	Yes	Yes
12-Bit Analog-to-Digital Module	12 Input Channels	12 Input Channels	16 Input Channels	16 Input Channels
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT
Programmable High/Low-Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions; 83 with Extended Instruction Set Enabled	75 Instructions; 83 with Extended Instruction Set Enabled	75 Instructions; 83 with Extended Instruction Set Enabled	75 Instructions; 83 with Extended Instruction Set Enabled
Packages	64-Pin TQFP	64-Pin TQFP	80-Pin TQFP	80-Pin TQFP

FIGURE 1-2: **PIC18F8628/8723 (80-PIN) BLOCK DIAGRAM**

Note 1: See Table 1-3 for I/O port pin descriptions.

2: RG5 is only available when $\overline{MCLR}$ functionality is disabled.

3: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, refer to **Section 2.0 "Oscillator Configurations"** of the *"PIC18F8722 Family Data Sheet"* (DS39646).

TABLE 1-2: **PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
				PORTA is a bidirectional I/O port.
RA0/AN0	24			
RA0		I/O	TTL	Digital I/O.
AN0		I	Analog	Analog input 0.
RA1/AN1	23			
RA1		I/O	TTL	Digital I/O.
AN1		I	Analog	Analog input 1.
RA2/AN2/V$_{REF}$-	22			
RA2		I/O	TTL	Digital I/O.
AN2		I	Analog	Analog input 2.
V$_{REF}$-		I	Analog	A/D reference voltage (low) input.
RA3/AN3/V$_{REF}$+	21			
RA3		I/O	TTL	Digital I/O.
AN3		I	Analog	Analog input 3.
V$_{REF}$+		I	Analog	A/D reference voltage (high) input.
RA4/T0CKI	28			
RA4		I/O	ST	Digital I/O.
T0CKI		I	ST	Timer0 external clock input.
RA5/AN4/HLVDIN	27			
RA5		I/O	TTL	Digital I/O.
AN4		I	Analog	Analog input 4.
HLVDIN		I	Analog	High/Low-Voltage Detect input.
RA6				See the OSC2/CLKO/RA6 pin.
RA7				See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
        ST = Schmitt Trigger input with CMOS levels   Analog = Analog input
        I = Input   O = Output
        P = Power   I^{2}C™ = I^{2}C/SMBus input buffer

Note 1: Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

    2: Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
				PORTC is a bidirectional I/O port.
RC0/T1OSO/T13CKI	30			
RC0		I/O	ST	Digital I/O.
T1OSO		O	—	Timer1 oscillator output.
T13CKI		I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/ECCP2/ P2A	29			
RC1		I/O	ST	Digital I/O.
T1OSI		I	CMOS	Timer1 oscillator input.
ECCP2[1]		I/O	ST	Enhanced Capture 2 input/Compare 2 output/ PWM2 output.
P2A[1]		O	—	ECCP2 PWM output A.
RC2/ECCP1/P1A	33			
RC2		I/O	ST	Digital I/O.
ECCP1		I/O	ST	Enhanced Capture 1 input/Compare 1 output/ PWM1 output.
P1A		O	—	ECCP1 PWM output A.
RC3/SCK1/SCL1	34			
RC3		I/O	ST	Digital I/O.
SCK1		I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL1		I/O	ST	Synchronous serial clock input/output for I^2C™ mode.
RC4/SDI1/SDA1	35			
RC4		I/O	ST	Digital I/O.
SDI1		I	ST	SPI data in.
SDA1		I/O	ST	I^2C data I/O.
RC5/SDO1	36			
RC5		I/O	ST	Digital I/O.
SDO1		O	—	SPI data out.
RC6/TX1/CK1	31			
RC6		I/O	ST	Digital I/O.
TX1		O	—	EUSART1 asynchronous transmit.
CK1		I/O	ST	EUSART1 synchronous clock (see related RX1/DT1).
RC7/RX1/DT1	32			
RC7		I/O	ST	Digital I/O.
RX1		I	ST	EUSART1 asynchronous receive.
DT1		I/O	ST	EUSART1 synchronous data (see related TX1/CK1).

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I^2C™ = I^2C/SMBus input buffer

Note 1: Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.
2: Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

TABLE 1-3: **PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
				PORTH is a bidirectional I/O port.
RH0/A16	79			
RH0		I/O	ST	Digital I/O.
A16		I/O	TTL	External memory address/data 16.
RH1/A17	80			
RH1		I/O	ST	Digital I/O.
A17		I/O	TTL	External memory address/data 17.
RH2/A18	1			
RH2		I/O	ST	Digital I/O.
A18		I/O	TTL	External memory address/data 18.
RH3/A19	2			
RH3		I/O	ST	Digital I/O.
A19		I/O	TTL	External memory address/data 19.
RH4/AN12/P3C	22			
RH4		I/O	ST	Digital I/O.
AN12		I	Analog	Analog input 12.
P3C[5]		O	—	ECCP3 PWM output C.
RH5/AN13/P3B	21			
RH5		I/O	ST	Digital I/O.
AN13		I	Analog	Analog input 13.
P3B[5]		O	—	ECCP3 PWM output B.
RH6/AN14/P1C	20			
RH6		I/O	ST	Digital I/O.
AN14		I	Analog	Analog input 14.
P1C[5]		O	—	ECCP1 PWM output C.
RH7/AN15/P1B	19			
RH7		I/O	ST	Digital I/O.
AN15		I	Analog	Analog input 15.
P1B[5]		O	—	ECCP1 PWM output B.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power I^{2}C™/SMB = I^{2}C/SMBus input buffer

Note 1: Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).
   2: Default assignment for ECCP2 in all operating modes (CCP2MX is set).
   3: Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).
   4: Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).
   5: Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

REGISTER 2-3:   ADCON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7   **ADFM:** A/D Result Format Select bit

                 1 = Right justified
                 0 = Left justified

bit 6   **Unimplemented:** Read as '0'

bit 5-3   **ACQT2:ACQT0:** A/D Acquisition Time Select bits

                 111 = 20 T_{AD}
                 110 = 16 T_{AD}
                 101 = 12 T_{AD}
                 100 = 8 T_{AD}
                 011 = 6 T_{AD}
                 010 = 4 T_{AD}
                 001 = 2 T_{AD}
                 000 = 0 T_{AD}**(1)**

bit 2-0   **ADCS2:ADCS0:** A/D Conversion Clock Select bits

                 111 = F_{RC} (clock derived from A/D RC oscillator)**(1)**
                 110 = $F_{OSC}/64$
                 101 = $F_{OSC}/16$
                 100 = $F_{OSC}/4$
                 011 = F_{RC} (clock derived from A/D RC oscillator)**(1)**
                 010 = $F_{OSC}/32$
                 001 = $F_{OSC}/8$
                 000 = $F_{OSC}/2$

Note 1:   If the A/D F_{RC} clock source is selected, a delay of one T_{CY} (instruction cycle) is added before the A/D clock starts. This allows the SLEEP instruction to be executed before starting a conversion.

2.4 Operation in Power-Managed Modes

The selection of the automatic acquisition time and A/D conversion clock is determined in part by the clock source and frequency while in a power-managed mode.

If the A/D is expected to operate while the device is in a power-managed mode, the ADCS2:ADCS0 bits in ADCON2 should be updated in accordance with the clock source to be used. The ACQT2:ACQT0 bits do not need to be adjusted as the ADCS2:ADCS0 bits adjust the T_{AD} time for the new clock speed. After entering the mode, an A/D acquisition or conversion may be started. Once started, the device should continue to be clocked by the same clock source until the conversion has been completed.

If desired, the device may be placed into the corresponding Idle mode during the conversion. If the device clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

Operation in Sleep mode requires the A/D F_{RC} clock to be selected. If the ACQT2:ACQT0 bits are set to '`000`' and a conversion is started, the conversion will be delayed one instruction cycle to allow execution of the `SLEEP` instruction and entry to Sleep mode. The IDLEN bit (OSCCON<7>) must have already been cleared prior to starting the conversion.

2.5 Configuring Analog Port Pins

The ADCON1, TRISA, TRISF and TRISH registers all configure the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (V_{OH} or V_{OL}) will be converted.

The A/D operation is independent of the state of the CHS3:CHS0 bits and the TRIS bits.

Note 1:	When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Analog conversion on pins configured as digital pins can be performed. The voltage on the pin will be accurately converted.
2:	Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.

PIC18F8723 FAMILY

2.8 Use of the ECCP2 Trigger

An A/D conversion can be started by the Special Event Trigger of the ECCP2 module. This requires that the CCP2M3:CCP2M0 bits (CCP2CON<3:0>) be programmed as '1011' and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/$\overline{\text{DONE}}$ bit will be set, starting the A/D acquisition and conversion, and the Timer1 (or Timer3) counter will be reset to zero. Timer1 (or Timer3) is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving ADRESH:ADRESL to the desired location). The appropriate analog input channel must be selected and the minimum acquisition period is either timed by the user, or an appropriate T_{ACQ} time selected before the Special Event Trigger sets the GO/$\overline{\text{DONE}}$ bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the Special Event Trigger will be ignored by the A/D module but will still reset the Timer1 (or Timer3) counter.

TABLE 2-2: REGISTERS ASSOCIATED WITH A/D OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	(3)
PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	(3)
PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	(3)
IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP	(3)
PIR2	OSCFIF	CMIF	—	EEIF	BCL1IF	HLVDIF	TMR3IF	CCP2IF	(3)
PIE2	OSCFIE	CMIE	—	EEIE	BCL1IE	HLVDIE	TMR3IE	CCP2IE	(3)
IPR2	OSCFIP	CMIP	—	EEIP	BCL1IP	HLVDIP	TMR3IP	CCP2IP	(3)
ADRESH	A/D Result Register High Byte								(3)
ADRESL	A/D Result Register Low Byte								(3)
ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON	(3)
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	(3)
ADCON2	ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	(3)
TRISA	TRISA7[1]	TRISA6[1]	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	(3)
TRISF	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	(3)
TRISH[2]	TRISH7	TRISH6	TRISH5	TRISH4	TRISH3	TRISH2	TRISH1	TRISH0	(3)

Legend: — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

Note 1: PORTA<7:6> and their direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

    2: These registers are not implemented on PIC18F6628/6723 devices.

    3: For these Reset values, see the *"PIC18F8722 Family Data Sheet"* (DS39646).

3.0 SPECIAL FEATURES OF THE CPU

Note:	For additional details on the Configuration bits, refer to **Section 25.1 "Configuration Bits" in** the *"PIC18F8722 Family Data Sheet"* (DS39646). Device ID information presented in this section is for the PIC18F8723 family only.

PIC18F8723 family devices include several features intended to maximize reliability and minimize cost through elimination of external components. These include:

• Device ID Registers

3.1 Device ID Registers

The Device ID registers are "read-only" registers. They identify the device type and revision to device programmers and can be read by firmware using table reads.

TABLE 3-1: DEVICE IDs

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
3FFFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx[1]
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	xxxx xxxx[1]

Legend: x = unknown

Note 1: See Register 3-1 and Register 3-2 for DEVID values. DEVID registers are read-only and cannot be programmed by the user.

PIC18F8723 FAMILY

REGISTER 3-1: **DEVID1: DEVICE ID REGISTER 1 FOR PIC18F8723 FAMILY DEVICES**

R	R	R	R	R	R	R	R
DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0
bit 7							bit 0

Legend:		
R = Read-only bit	P = Programmable bit	U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed		u = Unchanged from programmed state

bit 7-5 **DEV2:DEV0:** Device ID bits
See Register 3-2 for a complete listing.

bit 4-0 **REV4:REV0:** Revision ID bits
These bits are used to indicate the device revision.

REGISTER 3-2: **DEVID2: DEVICE ID REGISTER 2 FOR PIC18F8723 FAMILY DEVICES**

R	R	R	R	R	R	R	R
DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3
bit 7							bit 0

Legend:		
R = Read-only bit	P = Programmable bit	U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed		u = Unchanged from programmed state

bit 7-0 **DEV10:DEV3:** Device ID bits

DEV10:DEV3 (DEVID2<7:0>)	DEV2:DEV0 (DEVID1<7:5>)	Device
0100 1001	110	PIC18F6628
0100 1010	000	PIC18F6723
0100 1001	111	PIC18F8628
0100 1010	001	PIC18F8723

4.0   ELECTRICAL CHARACTERISTICS

Note: Other than some basic data, this section documents only the PIC18F8723 family's specifications that differ from those of the PIC18F8722 family devices. For detailed information on the electrical specifications shared by the PIC18F8723 family and PIC18F8722 family devices, see the *"PIC18F8722 Family Data Sheet"* (DS39646).

Absolute Maximum Ratings[†]

Ambient temperature under bias...-40°C to +125°C

Storage temperature .... -65°C to +150°C

Voltage on any pin with respect to VSS (except VDD and $\overline{MCLR}$) .... -0.3V to (VDD + 0.3V)

Voltage on VDD with respect to VSS .... -0.3V to +7.5V

Voltage on $\overline{MCLR}$ with respect to VSS **(Note 2)** .... 0V to +13.25V

Total power dissipation **(Note 1)** 1.0W

Maximum current out of VSS pin ....300 mA

Maximum current into VDD pin ....250 mA

Input clamp current, IIK (VI < 0 or VI > VDD)..±20 mA

Output clamp current, IOK (VO < 0 or VO > VDD) ....±20 mA

Maximum output current sunk by any I/O pin...25 mA

Maximum output current sourced by any I/O pin ....25 mA

Maximum current sunk by all ports ....200 mA

Maximum current sourced by all ports ....200 mA

Note 1: Power dissipation is calculated as follows:
Pdis = VDD x {IDD − Σ IOH} + Σ {(VDD − VOH) x IOH} + Σ(VOL x IOL)

2: Voltage spikes below VSS at the RG5/$\overline{MCLR}$/VPP pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the RG5/$\overline{MCLR}$/VPP pin, rather than pulling this pin directly to VSS.

† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FIGURE 4-3: PIC18LF8723 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)
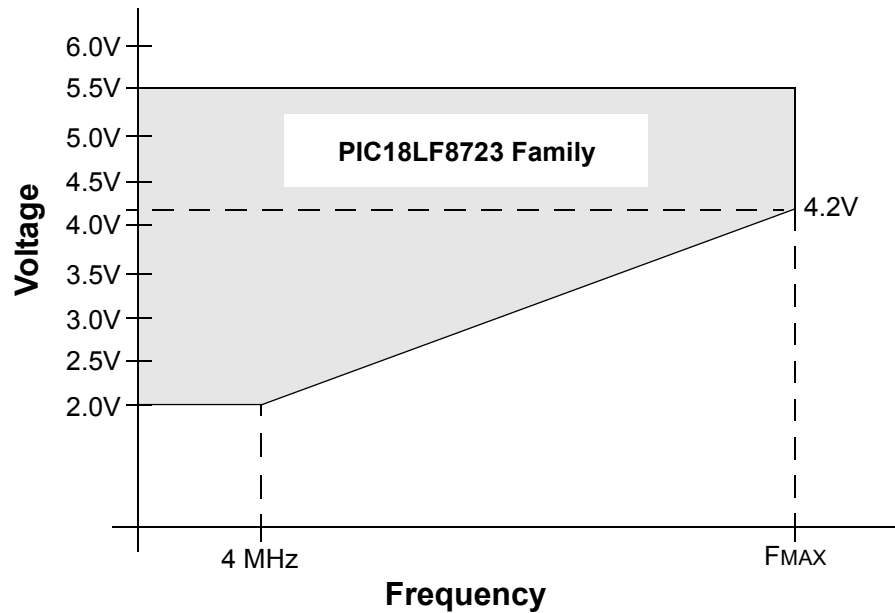
In 8-Bit External Memory mode:
F_{MAX} = (9.55 MHz/V) ($V_{DDAPPMIN}$ – 2.0V) + 4 MHz, if $V_{DDAPPMIN} \leq 4.2V$;
F_{MAX} = 25 MHz, if $V_{DDAPPMIN}$ > 4.2V.

In all other modes:
F_{MAX} = (16.36 MHz/V) ($V_{DDAPPMIN}$ – 2.0V) + 4 MHz;
F_{MAX} = 40 MHz, if $V_{DDAPPMIN}$ > 4.2V.

Note: $V_{DDAPPMIN}$ is the minimum voltage of the PIC® device in the application.

NOTES:

APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

Not Applicable

APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

Not Currently Available

NOTES:

PIC18F8723 FAMILY PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Examples:

a) PIC18LF6723-I/PT 301 = Industrial temp., TQFP package, Extended V$_{DD}$ limits, QTP pattern #301.

b) PIC18F6723-E/PT = Extended temp., TQFP package, standard V$_{DD}$ limits.

Device[1] [2]: PIC18F6628/6723, PIC18F8628/8723, V$_{DD}$ range 4.2V to 5.5V

PIC18LF6628/6723, PIC18LF6628/6723(V$_{DD}$ range 2.0V to 5.5V

Temperature Range:
I = -40°C to +85°C (Industrial)
E = -40°C to +125°C (Extended)

Package:
PT = TQFP (Thin Quad Flatpack)

Pattern: QTP, SQTP, Code or Special Requirements (blank otherwise)

Note 1: F = Standard Voltage Range
LF = Wide Voltage Range
2: T = in tape and reel TQFP packages only.