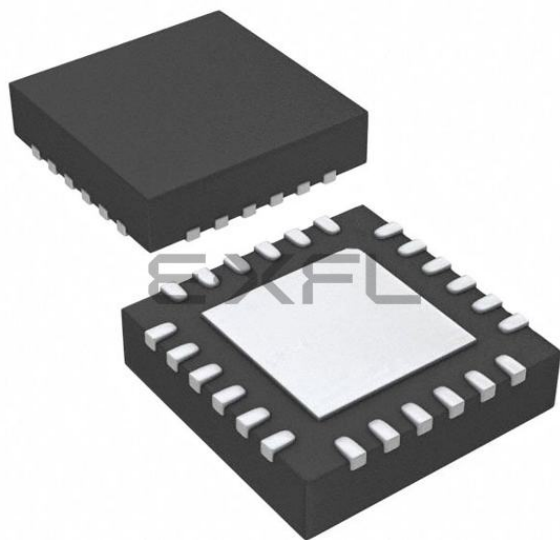




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Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	17
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VQFN Exposed Pad
Supplier Device Package	24-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32hg110f32g-a-qfn24

1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32HG110 devices.

Table 1.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (°C)	Package
EFM32HG110F32G-B-QFN24	32	4	25	1.98 - 3.8	-40 - 85	QFN24
EFM32HG110F64G-B-QFN24	64	8	25	1.98 - 3.8	-40 - 85	QFN24

Adding the suffix 'R' to the part number (e.g. EFM32HG110F32G-B-QFN24R) denotes tape and reel.

Visit **www.silabs.com** for information on global distributors and representatives.

Figure 3.3. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 14 MHz

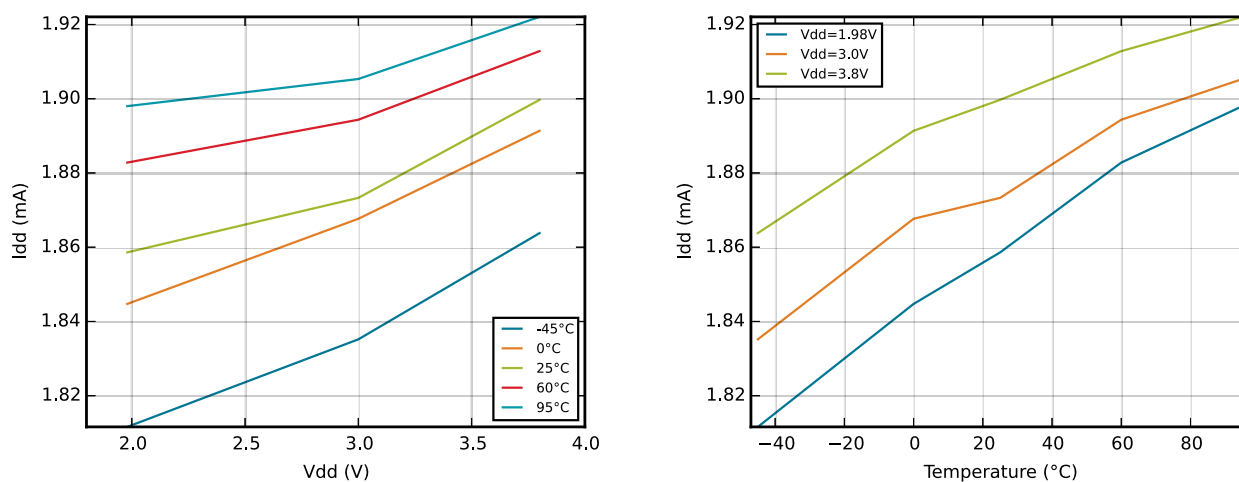


Figure 3.4. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 11 MHz

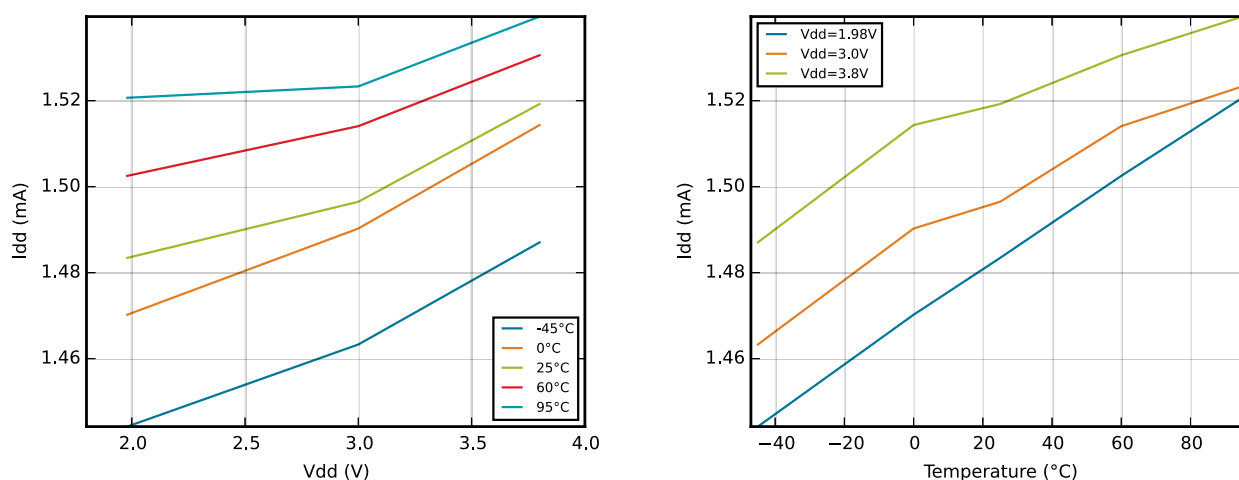
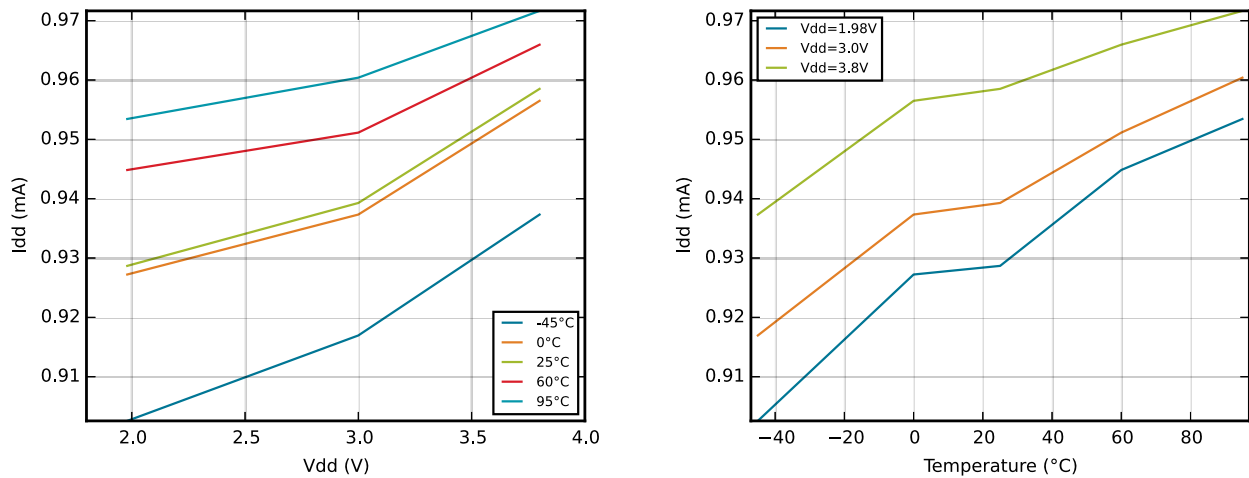


Figure 3.5. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 6.6 MHz



3.4.2 EM1 Current Consumption

Figure 3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 24 MHz

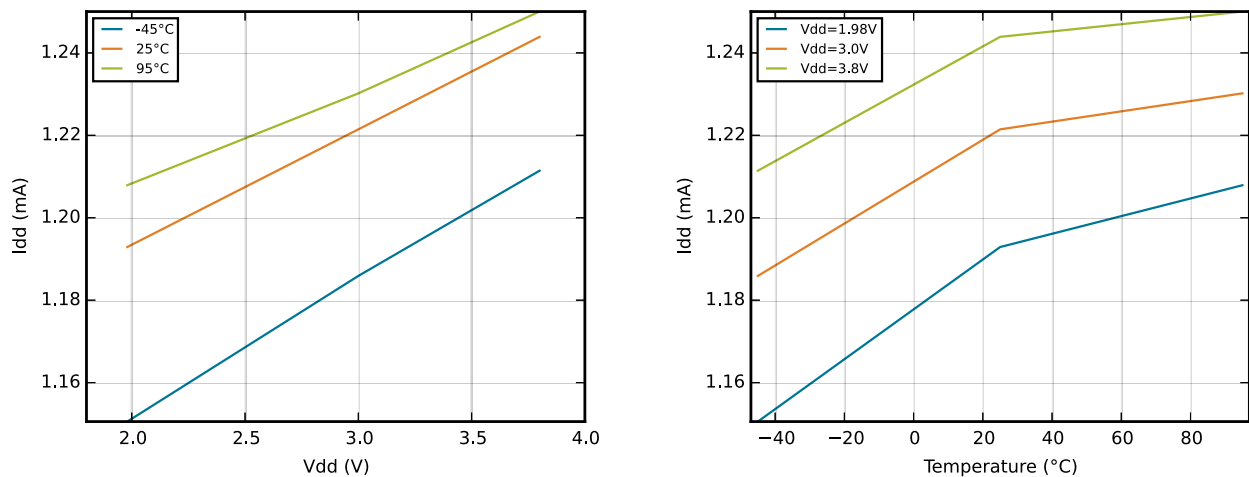


Figure 3.9. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11 MHz

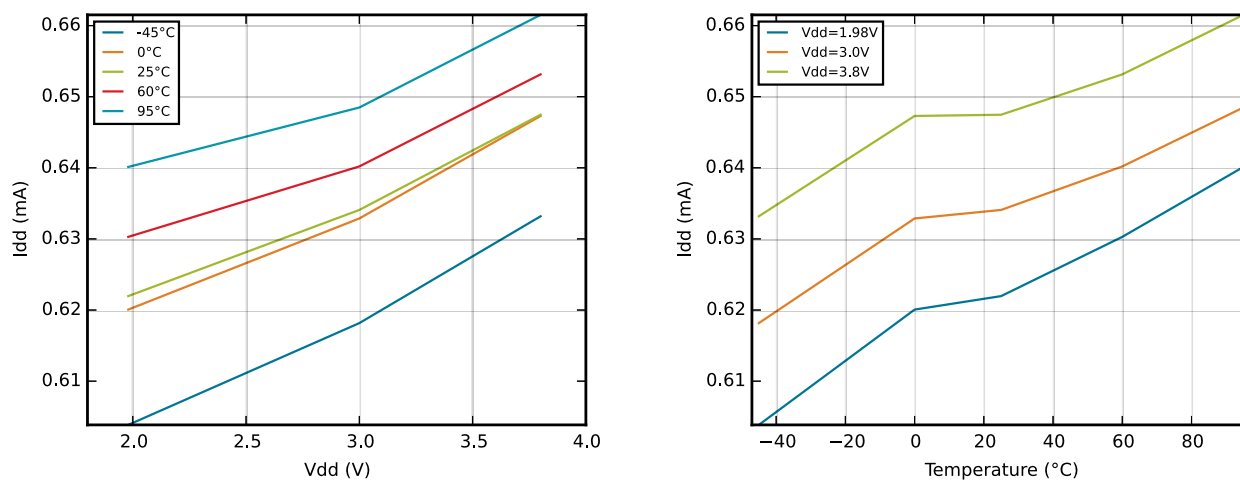
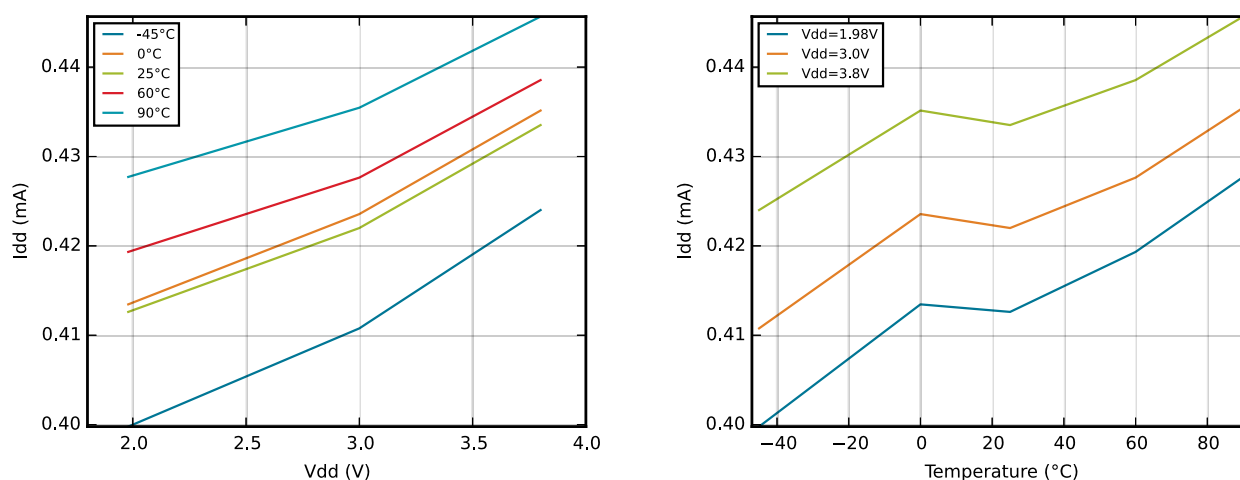
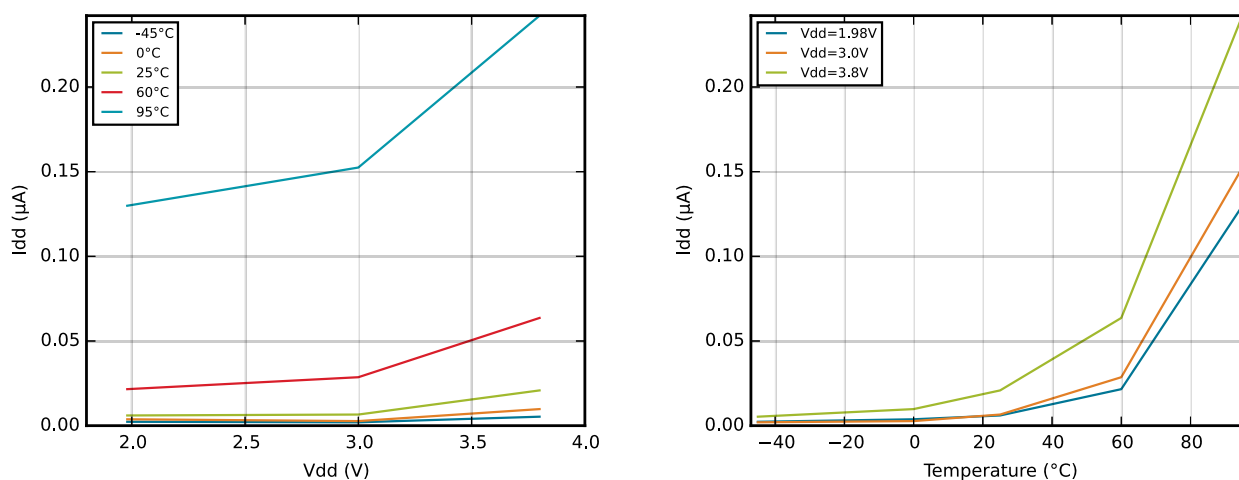


Figure 3.10. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 6.6 MHz



3.4.5 EM4 Current Consumption

Figure 3.13. EM4 current consumption.



3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 3.4. Energy Modes Transitions

Symbol	Parameter	Min	Typ	Max	Unit
t_{EM10}	Transition time from EM1 to EM0		0		HF-CORE-CLK cycles
t_{EM20}	Transition time from EM2 to EM0		2		μs
t_{EM30}	Transition time from EM3 to EM0		2		μs
t_{EM40}	Transition time from EM4 to EM0		163		μs

3.6 Power Management

The EFM32HG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

Table 3.5. Power Management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{BODextthr-}	BOD threshold on falling external supply voltage	EM0	1.74		1.96	V
		EM2	1.71	1.86	1.98	V
V _{BODextthr+}	BOD threshold on rising external supply voltage			1.85		V
t _{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		μs
C _{DECOUPLE}	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		μF

3.7 Flash

Table 3.6. Flash

Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC _{FLASH}	Flash erase cycles before failure		20000			cycles
RET _{FLASH}	Flash data retention	T _{AMB} <150°C	10000			h
		T _{AMB} <85°C	10			years
		T _{AMB} <70°C	20			years
t _{W_PROG}	Word (32-bit) programming time		20			μs
t _{P_ERASE}	Page erase time		20	20.4	20.8	ms
t _{D_ERASE}	Device erase time		40	40.8	41.6	ms
I _{ERASE}	Erase current				7 ¹	mA
I _{WRITE}	Write current				7 ¹	mA
V _{FLASH}	Supply voltage during flash erase and write		1.98		3.8	V

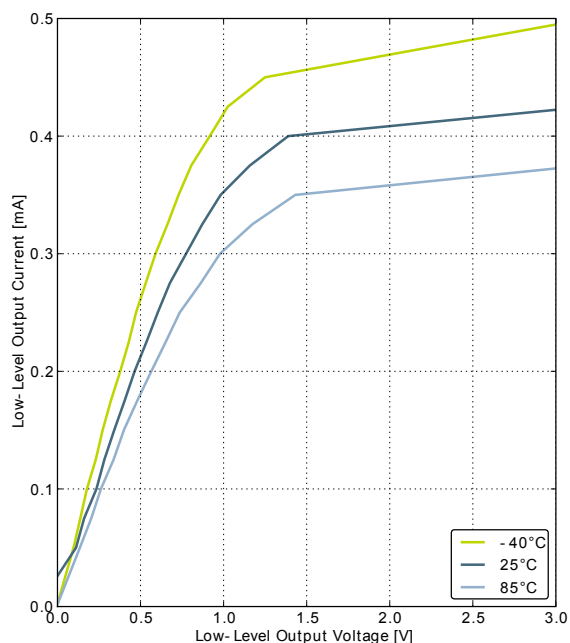
¹Measured at 25°C

3.8 General Purpose Input Output

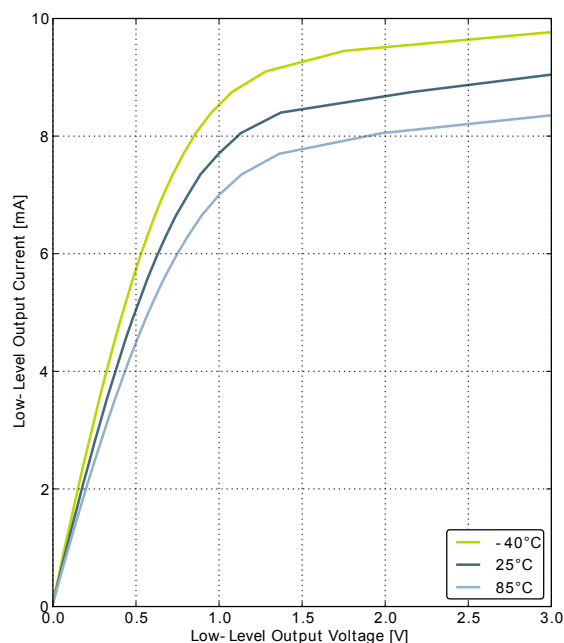
Table 3.7. GPIO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{IOIL}	Input low voltage				0.30V _{DD}	V
V _{IOIH}	Input high voltage		0.70V _{DD}			V
V _{IOOH}	Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sourcing 0.1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.80V _{DD}		V
		Sourcing 0.1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.90V _{DD}		V

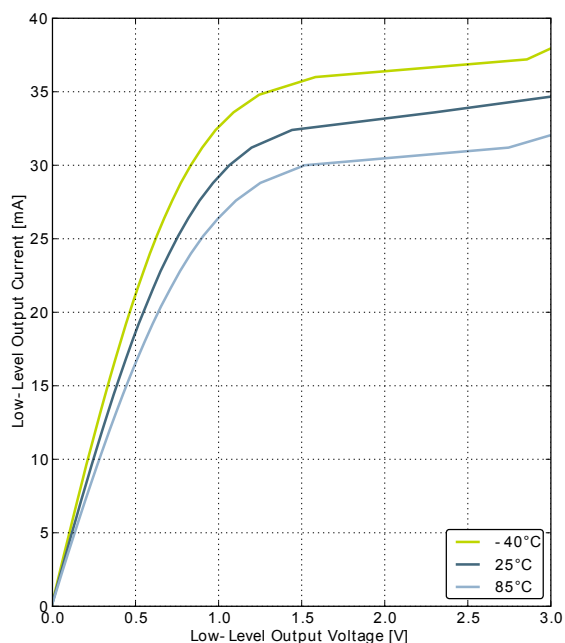
Figure 3.16. Typical Low-Level Output Current, 3V Supply Voltage



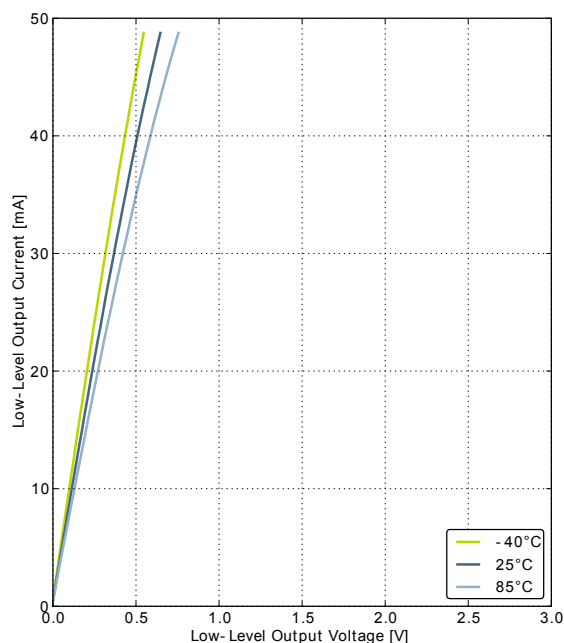
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

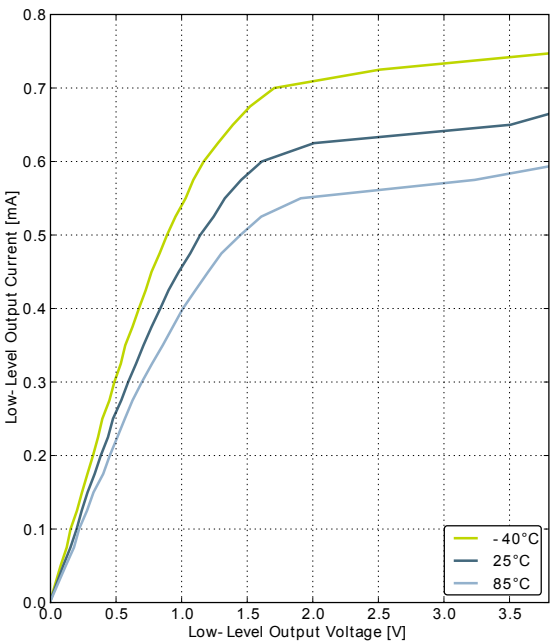


GPIO_Px_CTRL DRIVEMODE = STANDARD

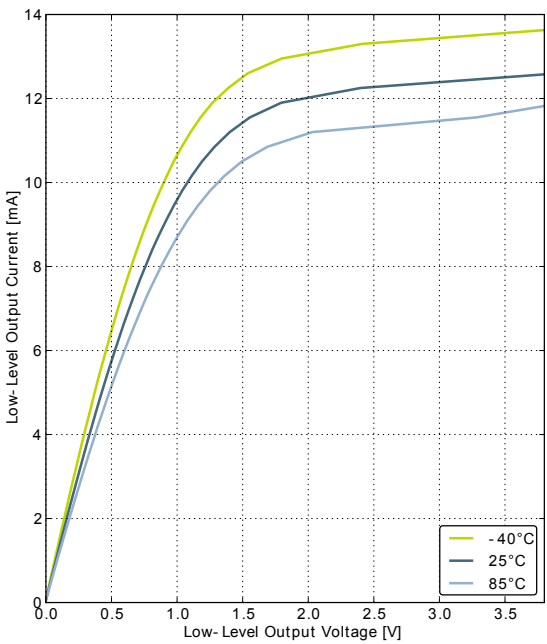


GPIO_Px_CTRL DRIVEMODE = HIGH

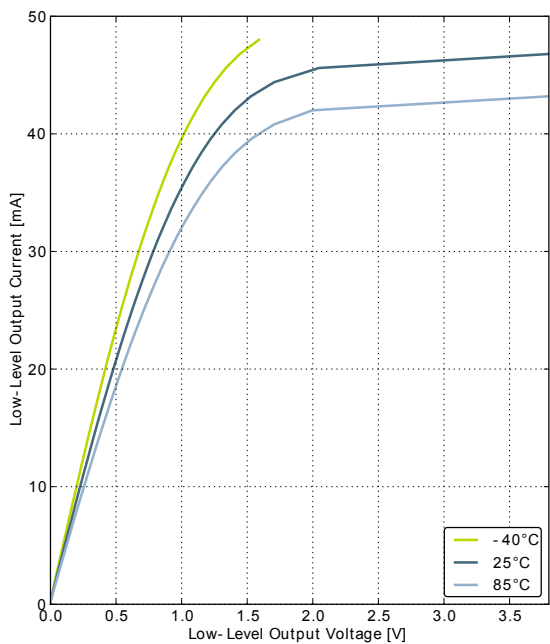
Figure 3.18. Typical Low-Level Output Current, 3.8V Supply Voltage



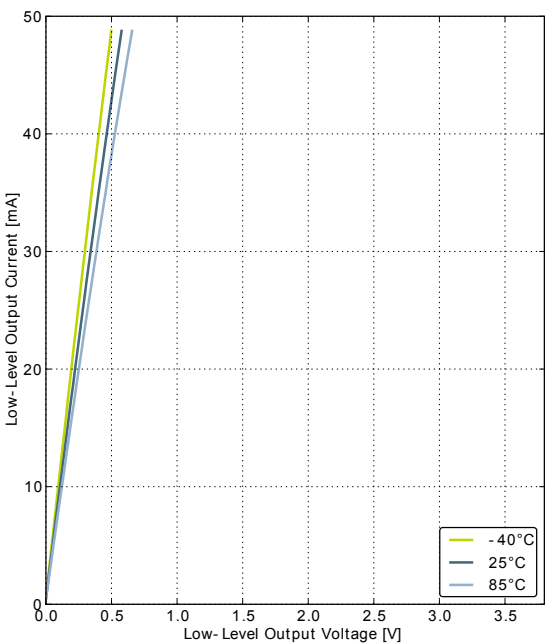
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

3.9 Oscillators

3.9.1 LFXO

Table 3.8. LFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR_{LFXO}	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
C_{LFXOL}	Supported crystal external load range		5		25	pF
I_{LFXO}	Current consumption for core and buffer after startup.	ESR=30 kOhm, C_L =10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t_{LFXO}	Start- up time.	ESR=30 kOhm, C_L =10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		1100		ms

For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

3.9.2 HFXO

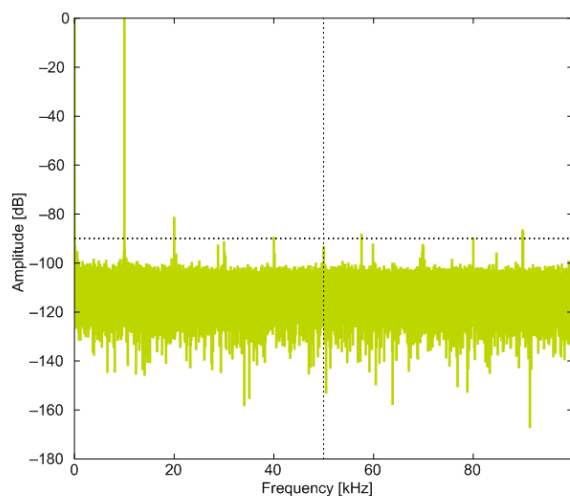
Table 3.9. HFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFXO}	Supported frequency, any mode		4		25	MHz
ESR_{HFXO}	Supported crystal equivalent series resistance (ESR)	Crystal frequency 25 MHz		30	100	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
g_{mHFXO}	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C_{HFXOL}	Supported crystal external load range		5		25	pF
I_{HFXO}	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, C_L =20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		μ A
		25 MHz: ESR=30 Ohm, C_L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		μ A
t_{HFXO}	Startup time	25 MHz: ESR=30 Ohm, C_L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11		785		μ s

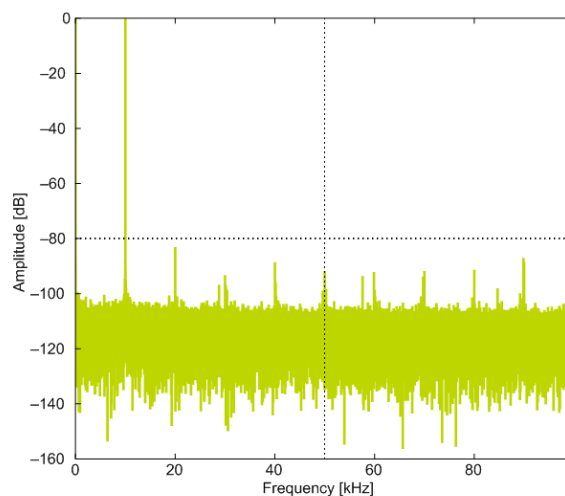
Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		66		dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		68		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		66		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	62	66		dB
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference		69		dB
SFDR _{ADC}	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		73		dBc
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		77		dBc
		1 MSamples/s, 12 bit, differential, V_{DD} reference		76		dBc
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		75		dBc
		1 MSamples/s, 12 bit, differential, 5V reference		69		dBc
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dBc

3.10.1 Typical performance

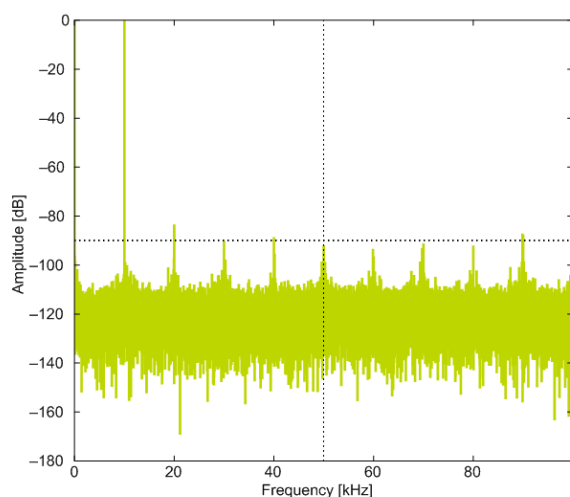
Figure 3.28. ADC Frequency Spectrum, $V_{dd} = 3V$, Temp = 25°C



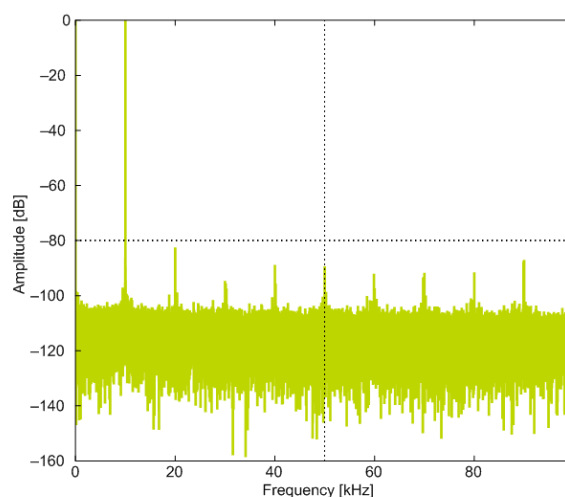
1.25V Reference



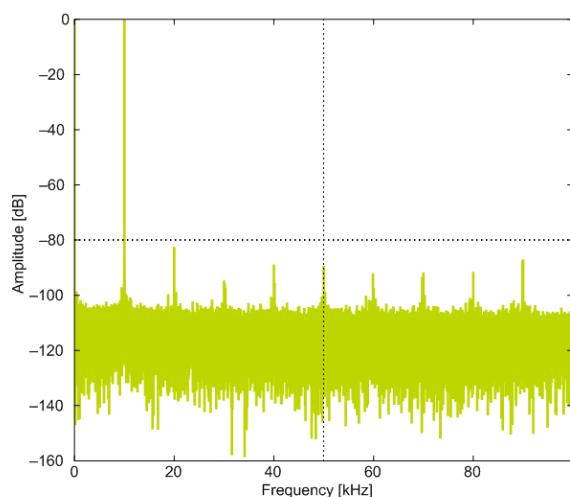
2.5V Reference



2XVDDVSS Reference



5VDIFF Reference



VDD Reference

Figure 3.35. IDAC Sink Current as a function of voltage from IDAC_OUT

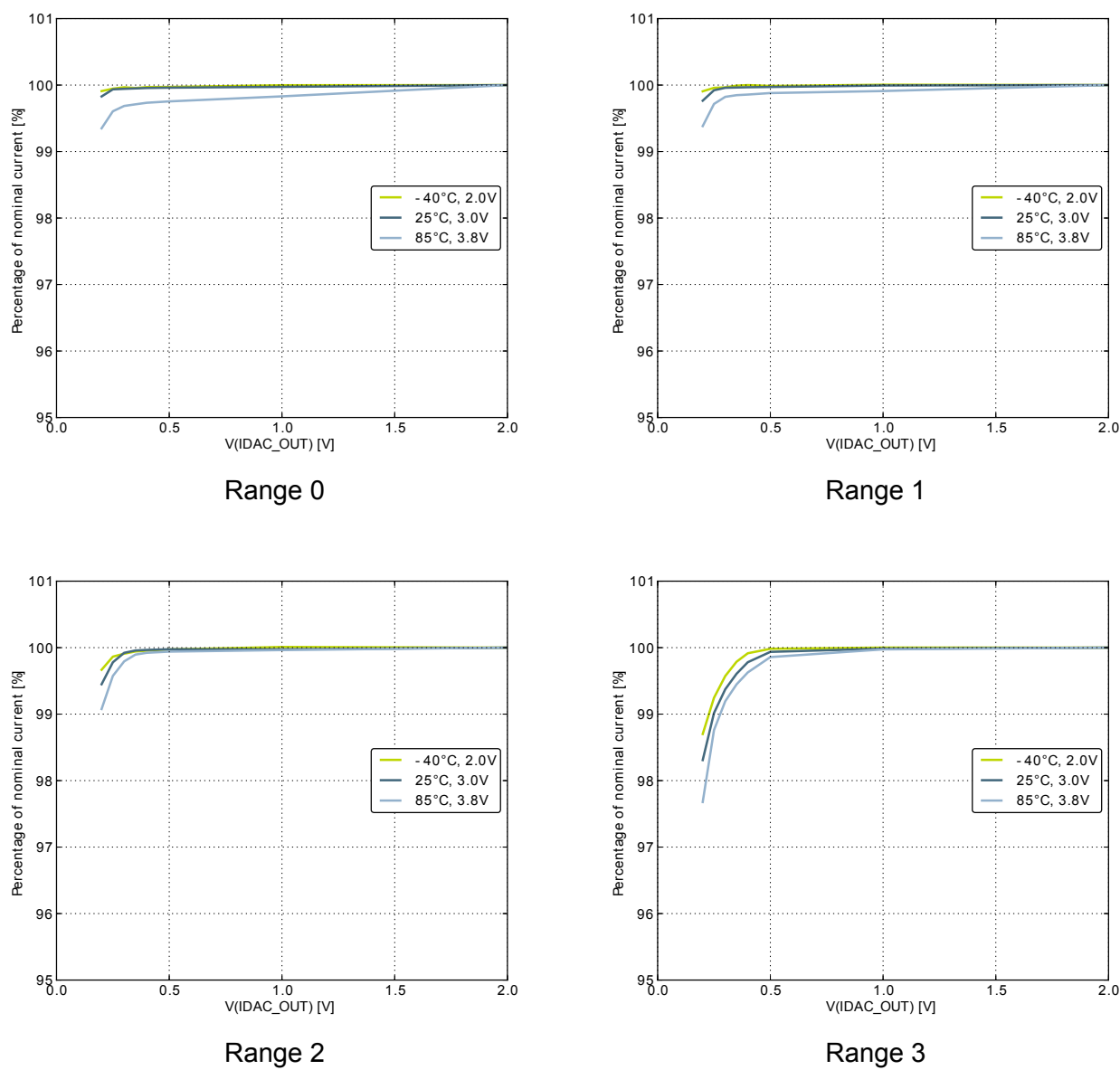
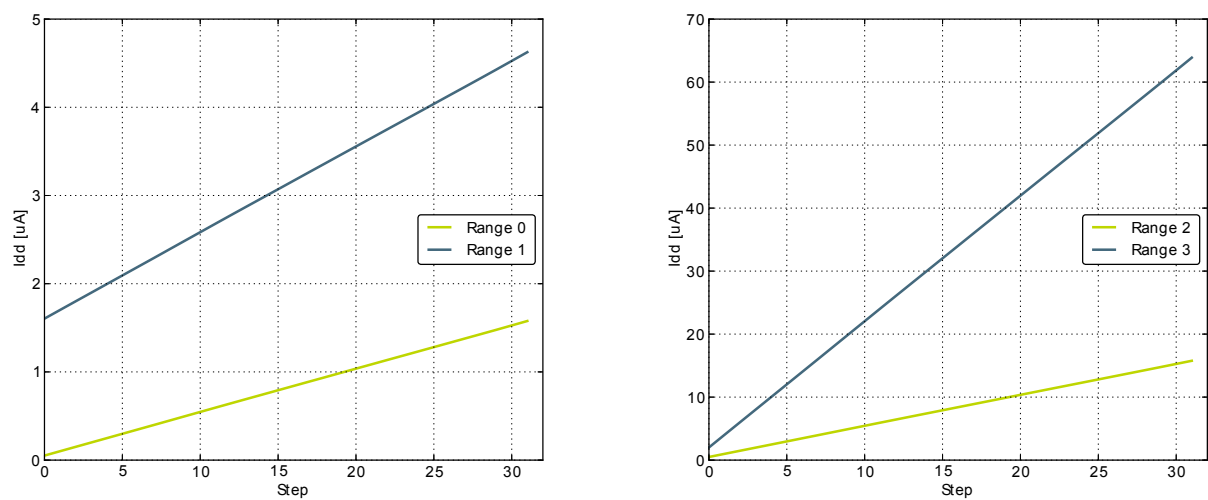


Figure 3.36. IDAC linearity



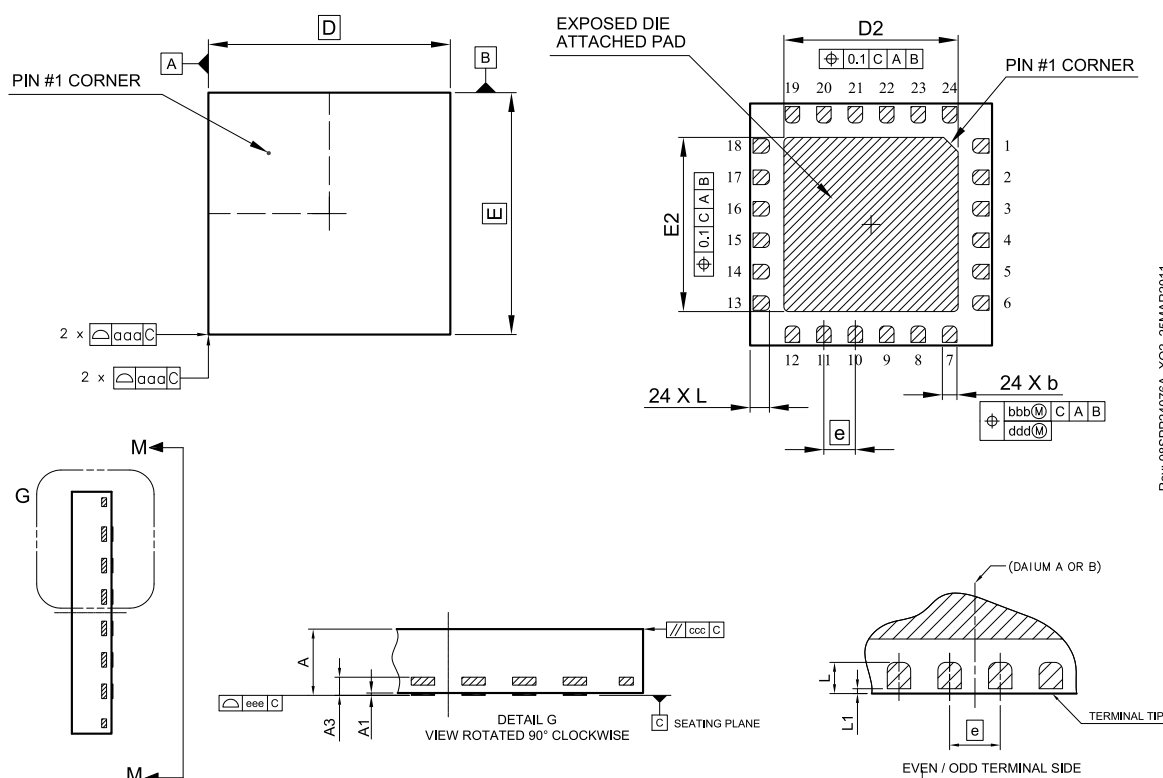
QFN24 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
2	IOVDD_0	Digital IO power supply 0.			
3	PC0	ACMP0_CH0	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5/6 US1_TX #0 US1_CS #5 I2C0_SDA #4	PRS_CH2 #0
4	PC1	ACMP0_CH1	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5/6 US1_TX #5 US1_RX #0 I2C0_SCL #4	PRS_CH3 #0
5	PB7	LFXTAL_P	TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
6	PB8	LFXTAL_N	TIM1_CC1 #3	US0_RX #4 US1_CS #0	
7	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
8	PB11	IDAC0_OUT	TIM1_CC2 #3 PCNT0_S1IN #4	US1_CLK #4	CMU_CLK1 #3 ACMP0_O #3
9	AVDD_2	Analog power supply 2.			
10	PB13	HFXTAL_P		US0_CLK #4/5 LEU0_TX #1	
11	PB14	HFXTAL_N		US0_CS #4/5 LEU0_RX #1	
12	AVDD_0	Analog power supply 0.			
13	PD6	ADC0_CH6	TIM1_CC0 #4 PCNT0_S0IN #3	US1_RX #2/3 I2C0_SDA #1	ACMP0_O #2
14	PD7	ADC0_CH7	TIM1_CC1 #4 PCNT0_S1IN #3	US1_TX #2/3 I2C0_SCL #1	CMU_CLK0 #2
15	VDD_DREG	Power supply for on-chip voltage regulator.			
16	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.			
17	PC14		TIM0_CDTI1 #1/6 TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3 US1_CS #3/4 LEU0_TX #5	PRS_CH0 #2
18	PC15		TIM0_CDTI2 #1/6 TIM1_CC2 #0	US0_CLK #3 US1_CLK #3 LEU0_RX #5	PRS_CH1 #2
19	PF0		TIM0_CC0 #5	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0 BOOT_TX
20	PF1		TIM0_CC1 #5	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0 GPIO_EM4WU3 BOOT_RX
21	PF2		TIM0_CC2 #5/6 TIM2_CC0 #3	US1_TX #4 LEU0_TX #4	CMU_CLK0 #3 PRS_CH0 #3 GPIO_EM4WU4
22	IOVDD_5	Digital IO power supply 5.			
23	PE12	ADC0_CH0	TIM1_CC2 #1 TIM2_CC1 #3	US0_RX #3 US0_CLK #0/6 I2C0_SDA #6	CMU_CLK1 #2 PRS_CH1 #3
24	PE13	ADC0_CH1	TIM2_CC2 #3	US0_TX #3 US0_CS #0/6 I2C0_SCL #6	ACMP0_O #0 PRS_CH2 #3 GPIO_EM4WU5

Table 4.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PA0
Port B	-	PB14	PB13	-	PB11	-	-	PB8	PB7	-	-	-	-	-	-	-
Port C	PC15	PC14	-	-	-	-	-	-	-	-	-	-	-	-	PC1	PC0
Port D	-	-	-	-	-	-	-	-	PD7	PD6	-	-	-	-	-	-
Port E	-	-	PE13	PE12	-	-	-	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	-	-	-	-	-	PF2	PF1	PF0

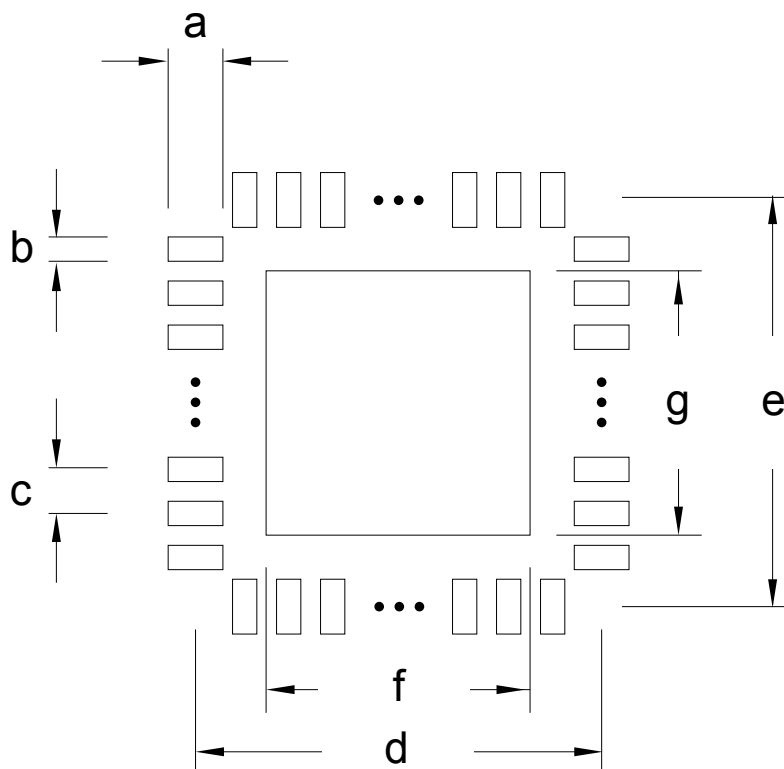
4.4 QFN24 Package

Figure 4.2. QFN24

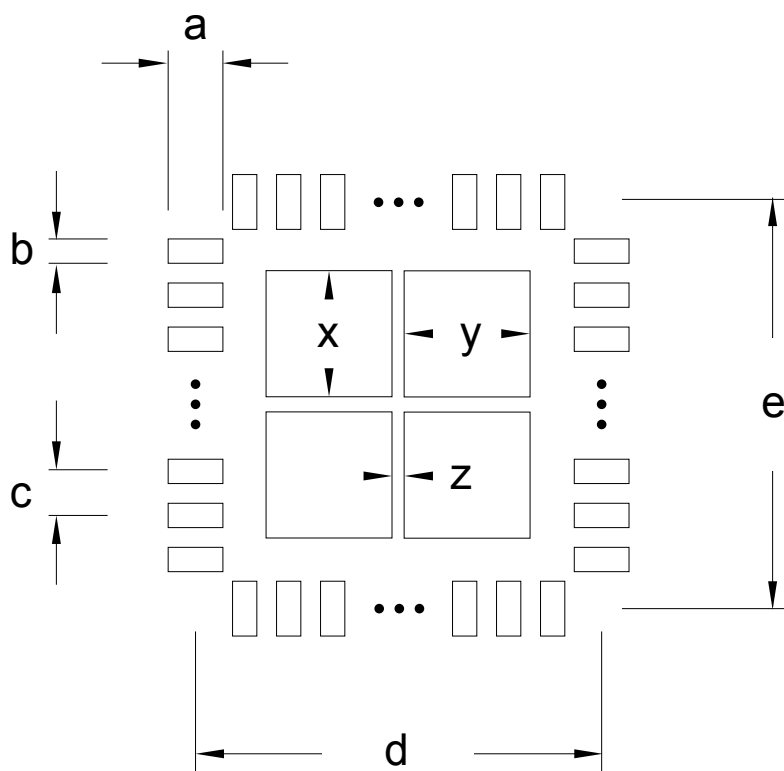


Note:

1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional

Figure 5.2. QFN24 PCB Solder Mask**Table 5.2. QFN24 PCB Solder Mask Dimensions (Dimensions in mm)**

Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.92	e	5.00
b	0.42	f	3.72
c	0.65	g	3.72
d	5.00	-	-

Figure 5.3. QFN24 PCB Stencil Design**Table 5.3. QFN24 PCB Stencil Design Dimensions (Dimensions in mm)**

Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.60	e	5.00
b	0.25	x	1.00
c	0.65	y	1.00
d	5.00	z	0.50

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Figure 4.2 (p. 56) .

5.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

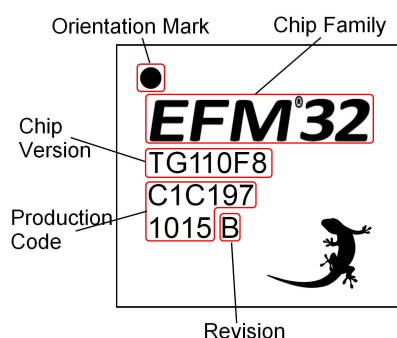
Place as many and as small as possible vias underneath each of the solder patches under the ground pad.

6 Chip Marking, Revision and Errata

6.1 Chip Marking

In the illustration below package fields and position are shown.

Figure 6.1. Example Chip Marking (top view)



6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 61) .

6.3 Errata

Please see the errata document for EFM32HG110 for description and resolution of device erratas. This document is available in Simplicity Studio and online at:

<http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit>

A Disclaimer and Trademarks

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