**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | e200z2, e200z4, e200z4 |
| Core Size | 32-Bit Tri-Core |
| Speed | 80MHz/160MHz |
| Connectivity | CANbus, Ethernet, FlexRay, I²C, LINbus, SPI, UART/USART |
| Peripherals | DMA, LVD, POR, Zipwire |
| Number of I/O | - |
| Program Memory Size | 2.5MB (2.5M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 64K x 8 |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 12b SAR, 16b Sigma-Delta |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-TQFP Exposed Pad |
| Supplier Device Package | 144-eTQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/spc574k72e5c6far |

**Table 9. Conducted emissions testing specifications(1)(Continued)**

| Module | Signal | Single/ Differential | Functional configuration | Emission test method | BISS limits(2)(3) |
|---|---|---|---|---|---|
| | | | | 150 Ω | |
| SIPI | RF_TX | Differential | C1-S3 | Yes | As per *Figure 5* |
| | RF_RX | | | Yes | As per *Figure 5* |
| | SysClk Tx | Single (10/20 MHz) | | Yes | As per *Figure 5* |
| | SysClk Rx | | | Yes | As per *Figure 5* |
| SCI | TXD | Single | C1-S3 | Yes | As per *Figure 5* |
| | RXD | | | Yes | As per *Figure 5* |
| LINFlex | LINTX | Single | C1-S3, C5-S3 | Yes | As per *Figure 5* |
| | LINRX | | | Yes | As per *Figure 5* |
| Oscillator | XTAL | Single | C1-S3 | Yes | As per *Figure 5* |
| | EXTAL | | | Yes | As per *Figure 5* |
| External clock | SYSCLK(6) | Single | C1-S3 | Yes | As per *Figure 5* |
| GPIO | GPIO(7) | Single | C1-S3, C5-S3 | Yes | As per *Figure 5* |
| 1.2 V core supply voltage | $V_{DD\_LV}$ | N/A | C1-S3 | Yes | As per *Figure 6* |
| I/O supply voltage | $V_{DD\_HV\_IO}$ | N/A | C1-S3 | Yes | As per *Figure 6* |
| Power management controller (PMC) supply voltage | $V_{DD\_HV\_PMC}$ | N/A | C1-S3 | Yes | As per *Figure 6* |

1. Reference “BISS Generic IC EMC Test Specification”, section 9.3, “Emission test configuration for ICs with CPU”.
2. All pins of the microcontroller are defined as ‘Local’ (according to BISS specification). Therefore, the supply pin on the microcontroller are tested to ‘Local’ requirements.
3. Limits apply to signal under test in static mode only
4. BISS port limits measured with SCK frequency below 10 MHz
5. BISS port limits: The 25/50 MHz clocks for an Ethernet RMII interface could cause the limits specified in *Figure 5 (BISS port limits)* to be exceeded unless care is taken in the application to ensure high EMC.
6. BISS port limits measured with clock less than 10 MHz and only one clock enabled at a time
7. BISS port limits: GPIO toggling less than 50 kHz and not more than 40 GPIO pins toggling simultaneously

**Table 10. RF immunity—Direct Power Injection (DPI) test specifications(1)**

| Module | Signal | Monitor pin | Function | BISS signal/power supply limit class |
|---|---|---|---|---|
| Oscillator | XTAL | EXTCLK | C11 | 0 dBm |
| Reset | PORST | GPIO | C10 | 12 dBm |
| | ESR0 | GPIO | C10 | 12 dBm |
| Test controller | TESTMODE | GPIO | C10 | 12 dBm |
| VDD core | $V_{DD\_LV}$ | Power | C10 | 12 dBm |
| VDD I/O | $V_{DD\_HV\_IO}$ | Power | C10 | 12 dBm |
| VDD FlexRay I/O | $V_{DD\_HV\_IO\_FLX}$ | Power | C10 | 12 dBm |

**Table 16. DC electrical specifications(1)(Continued)**

| Symbol | | C | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $V_{REF\_BG\_LR}$ | CC | C | Bandgap line regulation | $T_J$ = –40 °C<br>$V_{DD\_HV\_ADV}$ = 5 V ± 10% | — | — | 8000 | ppm/V |
| | | C | | $T_J$ = 150 °C<br>$V_{DD\_HV\_ADV}$ = 5 V ± 10% | — | — | 4000 | |

1. The ranges in this table are design targets and actual data may vary in the given range.
2. Application with maximum consumption, excludes lock step (safety) core, unloaded I/O with LVDS pins active and terminated.
3. Application with maximum consumption, excludes lock step (safety) core, unloaded I/O with LVDS pins active and terminated, with active flash program and erase.
4. Typical application consumption, unloaded I/O with LVDS pins active and terminated.
5. Device in STOP mode running from the internal RCOSC, with the external oscillator and ADCs disabled. Includes regulator consumption for $V_{DD\_LV}$ generation. Includes static I/O current with no pins toggling. $V_{DD\_HV}$ refers to all 5 V supplies ($V_{DD\_HV\_ADV}$, $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_JTAG}$, $V_{DD\_HV\_IO\_FLEX}$, and $V_{DD\_HV\_PMC}$). The $I_{DDAR}$ current can be further reduced by disabling the I/O pad compensation cells via the PDO bits in the ME_<mode>_MC registers in the mode entry module (MC_ME).
6. Leakage of $V_{DD\_LV\_BD}$ at junction temperature of 150 °C with production device powered estimated at 120 mA
7. Aurora and LFAST enabled, further consumption of 70 mA on $V_{DD\_HV\_IO\_BD}$ supply for Aurora transmission line
8. $I_{SPIKE}$ value is only valid for the use cases defined for the $I_{DDAPP}$ and $I_{DDAPP\_LV}$ specifications and its conditions given in *Table 16 (DC electrical specifications)*.
9. Moving window, valid for $I_{DDAPP}$ and its conditions given in *Table 16 (DC electrical specifications)*, with a maximum of 90 mA for the worst case application.
10. Condition 1: For power on period from 0 V up to normal operation with reset asserted.
    Condition 2: From reset asserted until IRCOSC frequency.
    Condition 3: Increasing frequency from IRCOSC to PLL full frequency.
    Condition 4: reverse order for power down to 0 V.
11. Current variation is considered during boot or during shut-down sequence. Progressive clock switching should be use to guarantee low current variation.This does not include current requested for the loading of the capacitances on the VDD_LV domain. Please refer to *Section 3.17.1, Power management integration*, Iclamp specification
12. $I_{DDOFF}$ is the minimum guaranteed consumption of the device during power-up. It can be used to correctly size power-off ballast in case of current injection during power-off state.Power up/down current transients can be limited by controlling the clock ramp rates with the Progressive Clock Frequency Switching block on the device.
13. The temperature coefficient and line regulation specifications are used to calculate the reference voltage drift at an operating point within the specified voltage and temperature operating conditions.

## 3.9 I/O pad specification

The following table describes the different pad type configurations.

**Table 17. I/O pad specification descriptions**

| Pad type | Description |
|---|---|
| Weak configuration | Provides a good compromise between transition time and low electromagnetic emission.<br>Pad impedance is centered around 800 Ω. |
| Medium configuration | Provides transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.<br>Pad impedance is centered around 200 Ω. |
| Strong configuration | Provides fast transition speed; used for fast interface.<br>Pad impedance is centered around 50 Ω. |

**Table 18. I/O input DC electrical characteristics(Continued)**

| Symbol | | C | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| **AUTOMOTIVE** | | | | | | | | |
| $V_{IHAUT}$(1) | SR | P | Input high level AUTOMOTIVE | 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V | 3.8 | — | $V_{DD\_HV\_IO}$ + 0.3 | V |
| $V_{ILAUT}$(2) | SR | P | Input low level AUTOMOTIVE | 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V | –0.3 | — | 2.1(3) | V |
| $V_{HYSAUT}$(4) | — | C | Input hysteresis AUTOMOTIVE | 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V | 0.4(6) | — | — | V |
| $V_{DRFTAUT}$ | — | C | Input $V_{IL}/V_{IH}$ temperature drift | 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V | — | — | 100(5) | mV |
| **CMOS** | | | | | | | | |
| $V_{IHCMOS\_H}$(6) | SR | C | Input high level CMOS (with hysteresis) | 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V | 0.65 * $V_{DD\_HV\_IO}$ | — | $V_{DD\_HV\_IO}$ + 0.3 | V |
| | | P | | 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V | | | | |
| $V_{IHCMOS}$(6) | SR | C | Input high level CMOS (without hysteresis) | 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V | 0.6 * $V_{DD\_HV\_IO}$ | — | $V_{DD\_HV\_IO}$ + 0.3 | V |
| | | P | | 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V | | | | |
| $V_{ILCMOS\_H}$(6) | SR | C | Input low level CMOS (with hysteresis) | 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V | –0.3 | — | 0.35 * $V_{DD\_HV\_IO}$ | V |
| | | P | | 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V | | | | |
| $V_{ILCMOS}$(6) | SR | C | Input low level CMOS (without hysteresis) | 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V | –0.3 | — | 0.4 * $V_{DD\_HV\_IO}$ | V |
| | | P | | 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V | | | | |
| $V_{HYSCMOS}$ | — | C | Input hysteresis CMOS | 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V | 0.1 * $V_{DD\_HV\_IO}$ | — | — | V |
| | | | | 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V(7) | | | | |
| $V_{DRFTCMOS}$ | — | C | Input $V_{IL}/V_{IH}$ temperature drift CMOS | 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V | — | — | 100(5) | mV |
| | | | | 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V | | | | |
| **INPUT CHARACTERISTICS**(8) | | | | | | | | |
| $I_{LKG}$ | CC | P | Digital input leakage | 4.5 V < $V_{DD\_HV}$ < 5.5 V<br>0.1*$V_{DD\_HV}$ < $V_{IN}$ < 0.9*$V_{DD\_HV}$<br>TJ < 150 °C | — | — | 1 | µA |
| $I_{LKG\_MED}$ | CC | C | Digital input leakage for MEDIUM pad | 4.5 V < $V_{DD_H}$V < 5.5 V<br>$V_{SS\_HV}$ < $V_{IN}$ < $V_{DD\_HV}$ | — | — | 500 | nA |
| $C_{IN}$ | CC | D | Digital input capacitance | GPIO input pins | — | — | 10 | pF |
| | | | | Ethernet input pins | — | — | 8 | |

1. A good approximation for the variation of the minimum value with supply is given by formula $V_{IHAUT}$ = 0.69 × $V_{DD\_HV\_IO}$.
2. A good approximation for the variation of the maximum value with supply is given by formula $V_{ILAUT}$ = 0.49 × $V_{DD\_HV\_IO}$.
3. Sum of $V_{ILAUT}$ and $V_{HYSAUT}$ is guaranteed to remain above 2.6 V in the 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V. Production test done with 2.06 V limit at cold, $T_j$ < 25 °C.
4. A good approximation of the variation of the minimum value with supply is given by formula $V_{HYSAUT}$ = 0.11 × $V_{DD\_HV\_IO}$.
5. In a 1 ms period, assuming stable voltage and a temperature variation of ±30 °C, $V_{IL}/V_{IH}$ shift is within ±50 mV. For SENT requirement refer to *Note: on page 46*.

**Table 20. WEAK configuration output buffer electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value[2] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $R_{OH\_W}$ | CC | P | PMOS output impedance weak configuration | 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, $I_{OH}$ < 0.5 mA | — | — | 1040 | Ω |
| $R_{OL\_W}$ | CC | P | NMOS output impedance weak configuration | 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, $I_{OL}$ < 0.5 mA | — | — | 1040 | Ω |
| $f_{MAX\_W}$ | CC | T | Output frequency weak configuration | $C_L$ = 25 pF[3] | — | — | 2 | MHz |
| | | | | $C_L$ = 50 pF[3] | — | — | 1 | |
| | | D | | $C_L$ = 200 pF[3] | — | — | 0.25 | |
| $t_{TR\_W}$ | CC | T | Transition time output pin weak configuration[4] | $C_L$ = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V | 40 | — | 120 | ns |
| | | | | $C_L$ = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V | 80 | — | 240 | |
| | | D | | $C_L$ = 200 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V | 320 | — | 820 | |
| | | | | $C_L$ = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5] | 50 | — | 150 | |
| | | | | $C_L$ = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5] | 100 | — | 300 | |
| | | | | $C_L$ = 200 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5] | 350 | — | 1050 | |
| $\lvert t_{SKEW\_W} \rvert$ | CC | T | Difference between rise and fall time | — | — | — | 25 | % |
| $I_{DCMAX\_W}$ | CC | D | Maximum DC current | — | — | — | 4 | mA |
| $T_{PHL/PLH}$ | CC | D | Propagation delay | $C_L$ = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V | — | — | 120 | ns |
| | | | | $C_L$ = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V | — | — | 150 | |
| | | | | $C_L$ = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V | — | — | 240 | |
| | | | | $C_L$ = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5] | — | — | 300 | |

1. All VDD_HV_IO conditions for 4.5V to 5.5V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0V to 3.6V are valid for VSIO[VSIO_xx] = 0
2. All values need to be confirmed during device validation.
3. $C_L$ is the sum of external capacitance. Device and package capacitances ($C_{IN}$, defined in *Table 18*) are to be added to calculate total signal capacitance ($C_{TOT}$ = $C_L$ + $C_{IN}$).
4. Transition time maximum value is approximated by the following formula:

   0 pF < $C_L$ < 50 pF$t_{TR_W}$(ns) = 22 ns + $C_L$(pF) × 4.4 ns/pF

   50 pF < $C_L$ < 200 pF$t_{TR_W}$(ns) = 50 ns + $C_L$(pF) × 3.85 ns/pF
5. Only for $V_{DD\_HV\_IO\_JTAG}$ segment when VSIO[VSIO_IJ] = 0 or $V_{DD\_HV\_IO\_FLEX}$ segment when VSIO[VSIO_IF] = 0.

*Table 21* shows the MEDIUM configuration output buffer electrical characteristics.

**Table 21. MEDIUM configuration output buffer electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value[2] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $R_{OH\_M}$ | CC | P | PMOS output impedance MEDIUM configuration | 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, $I_{OH}$ < 2 mA | — | — | 270 | Ω |
| $R_{OL\_M}$ | CC | P | NMOS output impedance MEDIUM configuration | 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, $I_{OL}$ < 2 mA | — | — | 270 | Ω |
| $f_{MAX\_M}$ | CC | T | Output frequency MEDIUM configuration | $C_L$ = 25 pF[3] | — | — | 12 | MHz |
| | | | | $C_L$ = 50 pF[4] | — | — | 6 | |
| | | D | | $C_L$ = 200 pF[4] | — | — | 1.5 | |
| $t_{TR\_M}$ | CC | T | Transition time output pin MEDIUM configuration[4] | $C_L$ = 25 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V | 10 | — | 30 | ns |
| | | | | $C_L$ = 50 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V | 20 | — | 60 | |
| | | D | | $C_L$ = 200 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V | 60 | — | 200 | |
| | | | | $C_L$ = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5] | 12 | — | 42 | |
| | | | | $C_L$ = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5] | 24 | — | 86 | |
| | | | | $C_L$ = 200 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5] | 70 | — | 300 | |
| $\lvert t_{SKEW\_M} \rvert$ | CC | T | Difference between rise and fall time | — | — | — | 25 | % |
| $I_{DCMAX\_M}$ | CC | D | Maximum DC current | — | — | — | 4 | mA |
| $T_{PHL/PLH}$ | CC | D | Propagation delay | $C_L$ = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V | — | — | 35 | ns |
| | | | | $C_L$ = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V | — | — | 42 | |
| | | | | $C_L$ = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V | — | — | 70 | |
| | | | | $C_L$ = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5] | — | — | 85 | |

1. All VDD_HV_IO conditions for 4.5V to 5.5V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0V to 3.6V are valid for VSIO[VSIO_xx] = 0
2. All values need to be confirmed during device validation.
3. $C_L$ is the sum of external capacitance. Device and package capacitances ($C_{IN}$, defined in *Table 18*) are to be added to calculate total signal capacitance ($C_{TOT} = C_L + C_{IN}$).
4. Transition time maximum value is approximated by the following formula:

   0 pF < $C_L$ < 50 pF$t_{TR_M}$(ns) = 5.6 ns + $C_L$(pF) × 1.11 ns/pF

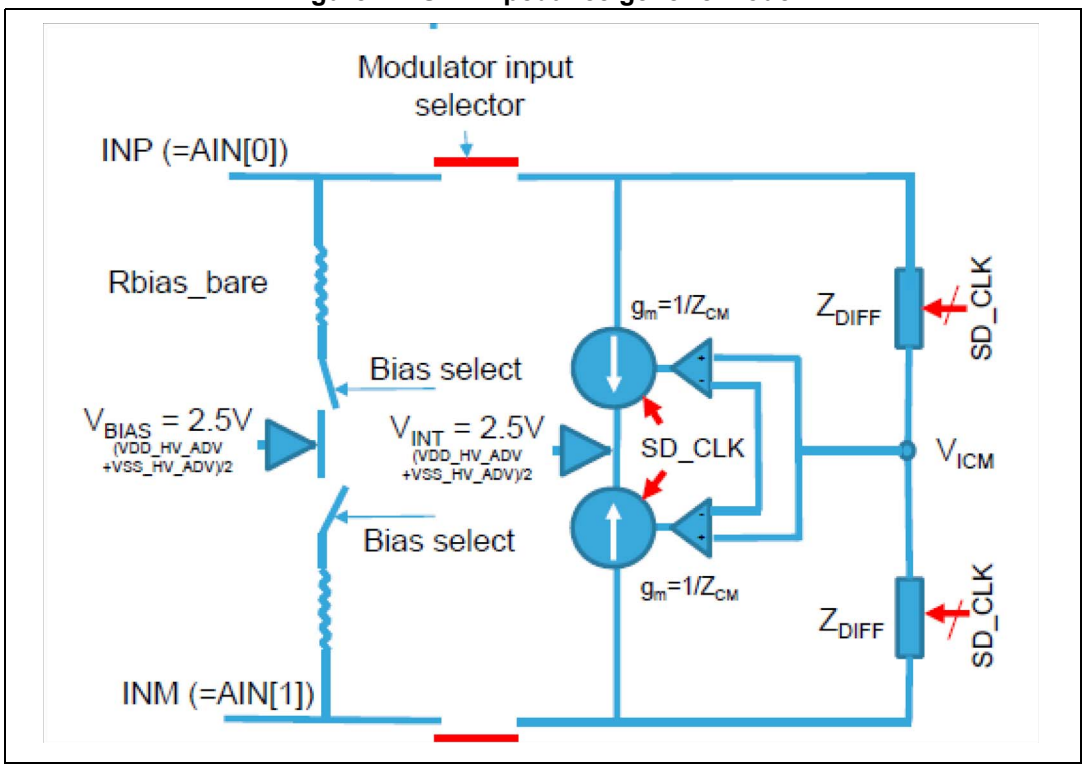
   50 pF < $C_L$ < 200 pF$t_{TR_M}$(ns) = 13 ns + $C_L$(pF) × 0.96 ns/pF

11. S/D ADC is functional in the range 3.0 – 4.5 V, SNR parameter degrades by 9 dB. Degraded SNR value based on simulation.
12. This parameter is guaranteed by bench validation with a small sample of devices across process variations.
13. Input impedance is valid over the full input frequency range.Input impedance is calculated in megaohms by the formula 25.6/(Gain * $f_{ADCD\_M}$).
14. Impedance given at $F_{ADCD\_M}$ = 16MHz. Impedance is inversely proportional to frequency: $Z_{DIFF}(F_{ADCD\_M})$ = $16MHz/F_{ADCD\_M}*Z_{DIFF}$
15. Impedance given at $F_{ADCD\_M}$ = 16MHz. Impedance is inversely proportional to frequency: $Z_{CM}(F_{ADCD\_M})$ = $16MHz/F_{ADCD\_M}*Z_{CM}$
16. SNR values guaranteed only if external noise on the ADC input pin is attenuated by the required SNR value in the frequency range of $f_{ADCD\_M} - f_{ADCD\_S}$ to $f_{ADCD\_M} + f_{ADCD\_S}$, where $f_{ADCD\_M}$ is the input sampling frequency, and $f_{ADCD\_S}$ is the output sample frequency. A proper external input filter should be used to remove any interfering signals in this frequency range.
17. The ±1% passband ripple specification is equivalent to 20 * $\log_{10}$ (0.99) = 0.087 dB.
18. Propagation of the information from the pin to the register CDR[CDATA] and flags SFR[DFEF], SFR[DFFF] is given by the different modules that need to be crossed: delta/sigma filters, high pass filter, fifo module, clock domain synchronizers. The time elapsed between data availability at pin and internal S/D module registers is given by the below formula:

    REGISTER LATENCY = tLATENCY + 0.5/fADCD_S + 2 (~+1)/fADCD_M + 2(~+1)fPBRIDGEx_CLK

    where fADCD_S is the frequency of the sampling clock, fADCD_M is the frequency of the modulator, and fPBRIDGEx_CLK is the frequency of the peripheral bridge clock feeds to the ADC S/D module. The (~+1) symbol refers to the number of clock cycles uncertainty (from 0 to 1 clock cycle) to be added due to resynchronization of the signal during clock domain crossing.
    Some further latency may be added by the target module (core, DMA, interrupt) controller to process the data received from the ADC S/D module.
19. This capacitance does not include pin capacitance, that can be considered together with external capacitance, before sampling switch.
20. Consumption is given after power-up, when steady state is reached. Extra consumption up to 2 mA may be required during internal circuitry set-up.

**Figure 17. S/D impedance generic model**



### 3.15.1 LFAST interface timing diagrams

**Figure 18. LFAST and MSC/DSPI LVDS timing definition**

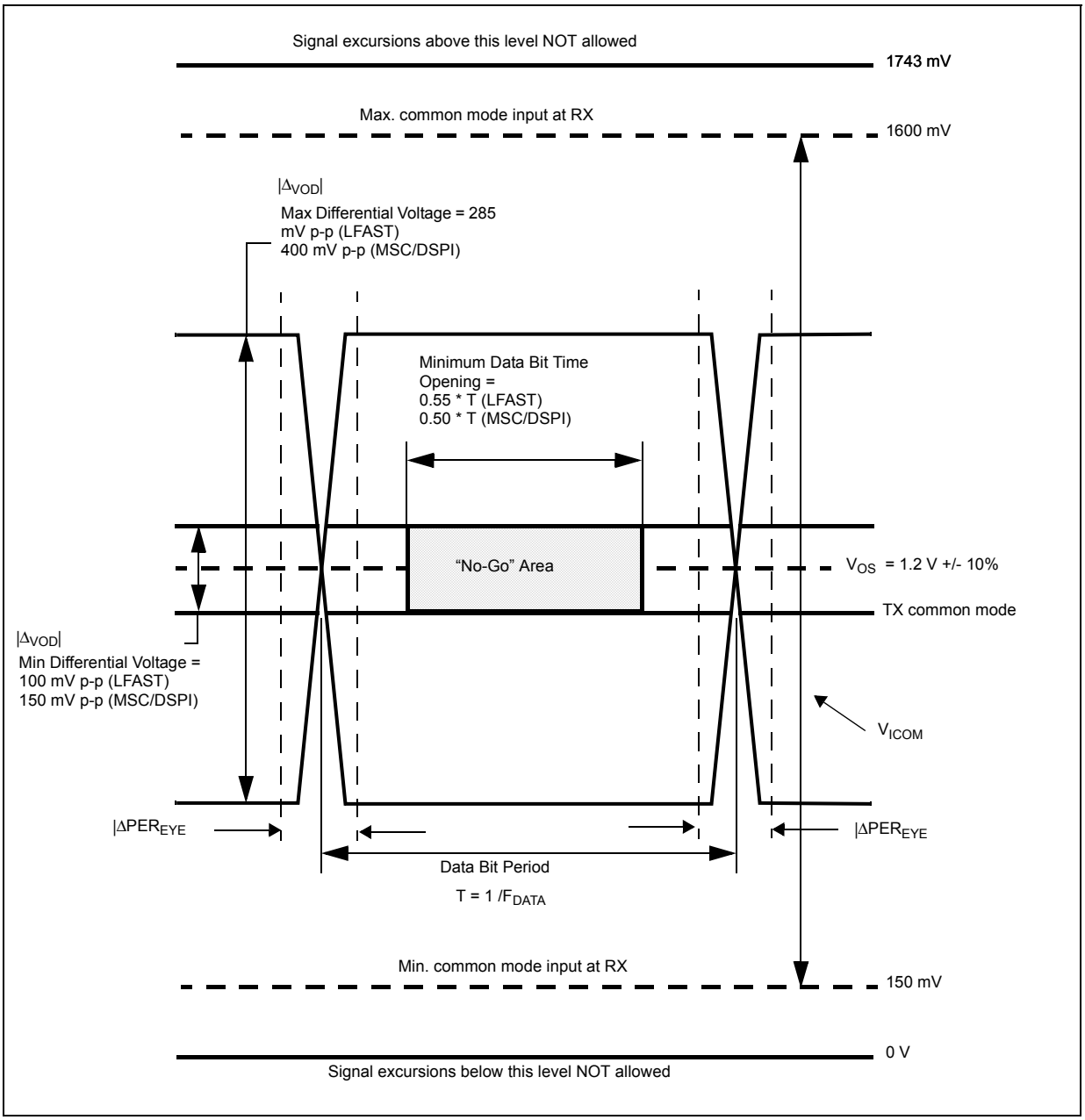


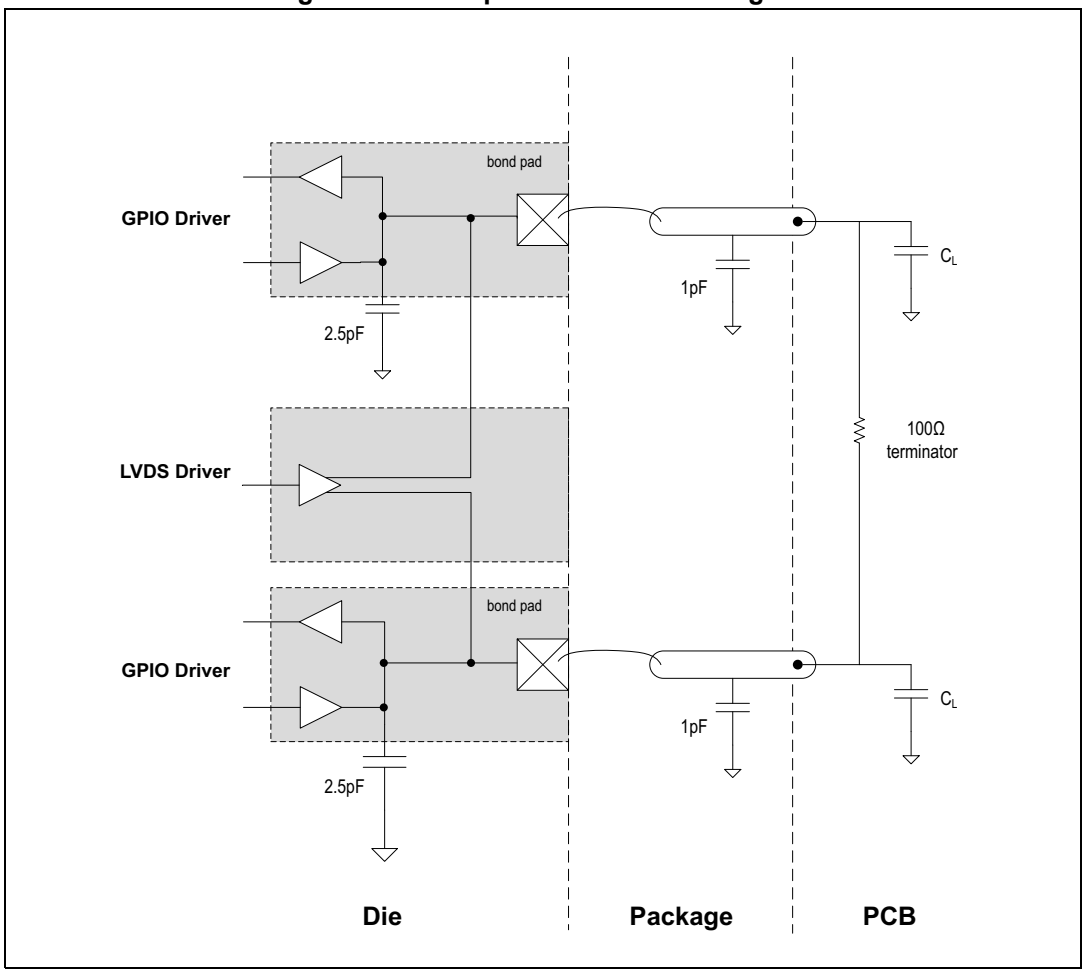
**Table 36. LVDS pad startup and receiver electrical characteristics[1][2](Continued)**

| Symbol | | C | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $t_{SM2NM\_TX}$ | CC | T | Transmitter startup time (sleep mode to normal mode)[7] | Not applicable to the MSC/DSPI LVDS pad | — | 0.2 | 0.5 | µs |
| $t_{PD2NM\_RX}$ | CC | T | Receiver startup time (power down to normal mode)[8] | — | — | 20 | 40 | ns |
| $t_{PD2SM\_RX}$ | CC | T | Receiver startup time (power down to sleep mode)[9] | Not applicable to the MSC/DSPI LVDS pad | — | 20 | 50 | ns |
| $I_{LVDS\_BIAS}$ | CC | C | LVDS bias current consumption | Tx or Rx enabled | — | — | 0.95 | mA |
| **TRANSMISSION LINE CHARACTERISTICS (PCB Track)** | | | | | | | | |
| $Z_0$ | SR | D | Transmission line characteristic impedance | — | 47.5 | 50 | 52.5 | Ω |
| $Z_{DIFF}$ | SR | D | Transmission line differential impedance | — | 95 | 100 | 105 | Ω |
| **RECEIVER** | | | | | | | | |
| $V_{ICOM}$ | SR | T | Common mode voltage | — | 0.15 (10) | — | 1.6[11] | V |
| $\|\Delta_{VI}\|$ | SR | T | Differential input voltage[12] | — | 100 | — | — | mV |
| $R_{IN}$ | CC | D | Terminating resistance | $V_{DD\_HV\_IO}$ = 5.0 V ± 10% | 80 | 125 | 150 | Ω |
| | | D | | $V_{DD\_HV\_IO}$ = 3.3 V ± 10% | 80 | 115 | 150 | Ω |
| $C_{IN}$ | CC | D | Differential input capacitance[13] | — | — | 3.5 | 6.0 | pF |
| $I_{LVDS\_RX}$ | CC | C | Receiver DC current consumption | Enabled | — | — | 0.5 | mA |

1. The LVDS pad startup and receiver electrical characteristics in this table apply to both the LFAST & High-speed Debug (HSD) LVDS pad, and the MSC/DSPI LVDS pad except where noted in the conditions.
2. All LVDS pad electrical characteristics are valid from –40 °C to 150 °C.
3. All startup times are defined after a 2 peripheral bridge clock delay from writing to the corresponding enable bit in the LVDS control registers (LCR) of the LFAST and High-Speed Debug modules. The value of the LCR bits for the LFAST/HSD modules don't take effect until the corresponding SIUL2 MSCR ODC bits are set to LFAST LVDS mode. Startup times for MSC/DSPI LVDS are defined after 2 peripheral bridge clock delay after selecting MSC/DSPI LVDS in the corresponding SIUL2 MSCR ODC field.
4. Startup times are valid for the maximum external loads CL defined in both the LFAST/HSD and MSC/DSPI transmitter electrical characteristic tables.
5. Bias startup time is defined as the time taken by the current reference block to reach the settling bias current after being enabled.
6. Total transmitter startup time from power down to normal mode is $t_{STRT\_BIAS}$ + $t_{PD2NM\_TX}$ + 2 peripheral bridge clock periods.
7. Total transmitter startup time from sleep mode to normal mode is $t_{SM2NM\_TX}$ + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
8. Total receiver startup time from power down to normal mode is $t_{STRT\_BIAS}$ + $t_{PD2NM\_RX}$ + 2 peripheral bridge clock periods.
9. Total receiver startup time from power down to sleep mode is $t_{PD2SM\_RX}$ + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
10. Absolute min = 0.15 V – (285 mV/2) = 0 V

3. Valid for maximum data rate $f_{DATA}$. Value given is the capacitance on each terminal of the differential pair, as shown in *Figure 21*.
4. Valid for maximum external load $C_L$.

**Figure 21. LVDS pad external load diagram**




## 3.15.3 LFAST PLL electrical characteristics

The following table contains the electrical characteristics for the LFAST PLL.

**Table 39. LFAST PLL electrical characteristics(1)**

| Symbol | | C | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Nominal | Max | |
| $f_{RF\_REF}$ | SR | D | PLL reference clock frequency | — | 10 | — | 26 | MHz |
| $ERR_{REF}$ | CC | D | PLL input reference clock frequency error | — | –1 | — | 1 | % |
| $DC_{REF}$ | CC | D | PLL input reference clock duty cycle | — | 45 | — | 55 | % |

**Table 41. Device Power Supply Integration(Continued)**

| Symbol | | C | Parameter | Conditions[1] | Value[2] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $C_{DECFLA}$ | SR | D | Decoupling capacitance for flash supply | $V_{DD\_HV\_FLA}$/VSS pair | 100 | 220 | — | nF |
| $C_{HV\_ADC}$ | SR | D | $V_{DD\_HV\_ADV}$ external capacitance[5] | | 1 | 2.2 | — | µF |

1. $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 / 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Recommended X7R or X5R ceramic –35 % / +20 % variation across process, temperature, voltage and after aging.
4. At power-up condition before trimming.
5. For noise filtering, add a high frequency bypass capacitance of 0.1 µF between $V_{DD\_HV\_ADV}$ and $V_{SS\_HV\_ADV}$.

## 3.17.3 Device voltage monitoring

The LVD/HVDs and their associated levels for the device are given in the following table. The figure below illustrates the workings of voltage monitoring threshold.

**Figure 23. Voltage monitor threshold definition**

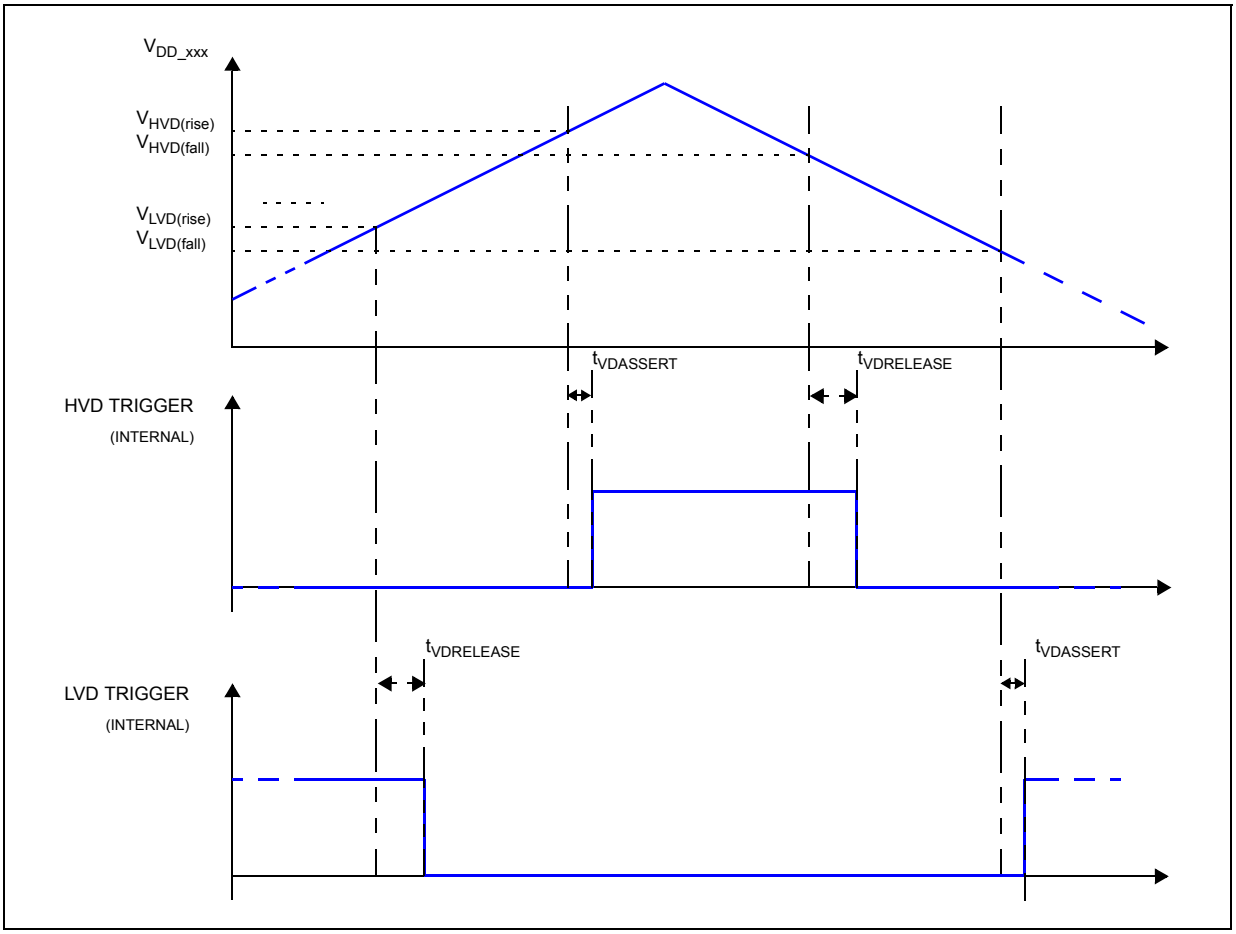


**Table 46. Flash memory Life Specification(Continued)**

| Symbol | Characteristics[1] | Value | | | | Unit |
|---|---|---|---|---|---|---|
| | | Min | C | Typ | C | |
| $N_{CER256K}$ | 256 KB CODE Flash endurance | 1 | — | 100 | — | kcycles |
| $N_{DER16K}$ | 16 KB EEPROM Flash endurance | 250 | — | — | — | kcycles |
| $t_{DR1k}$ | Minimum data retention Blocks with 0 - 1,000 P/E cycles | 20 | — | — | — | Years |
| $t_{DR10k}$ | Minimum data retention Blocks with 1,001 - 10,000 P/E cycles | 20 | — | — | — | Years |
| $t_{DR250k}$ | Minimum data retention Blocks with 10,001 - 250,000 P/E cycles | 10 | — | — | — | Years |

1. Program and erase cycles supported across specified temperature specs.

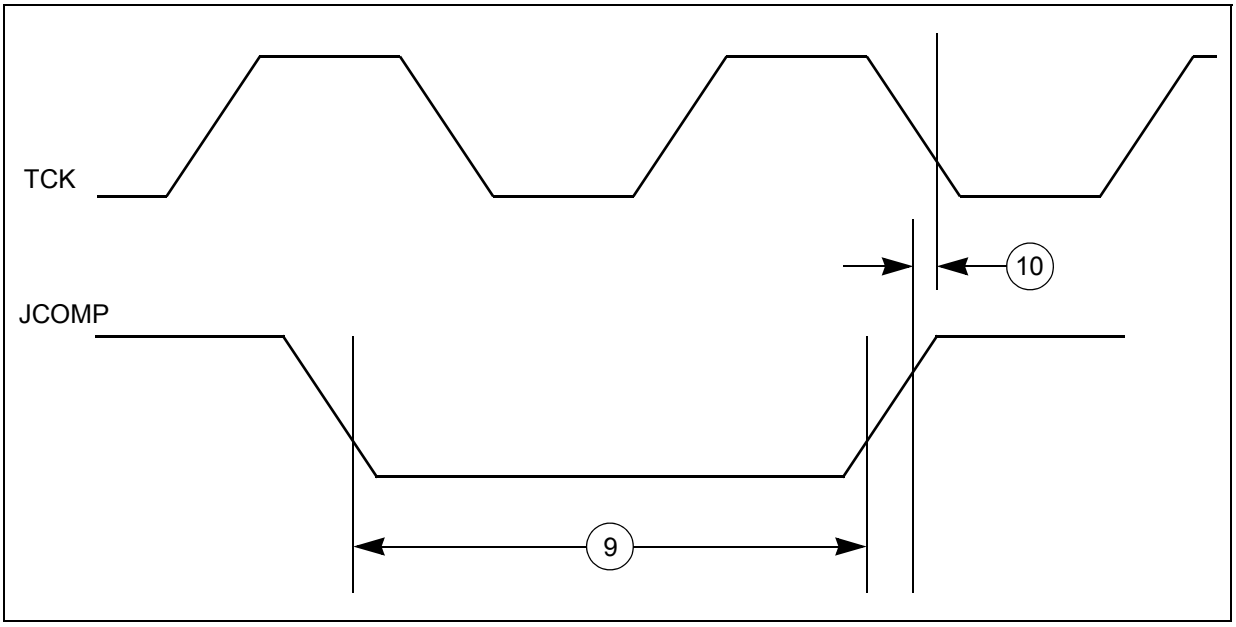
### 3.18.1 Flash read wait state and address pipeline control settings

*Table 47* describes the recommended RWSC settings at various operating frequencies based on specified intrinsic flash access times of the Flash array at 150 °C.

**Table 47. Flash memory RWSC configuration**

| Platform Frequency | Minimum RWSC settings |
|---|---|
| 0 – 25 MHz | 0 |
| 25 – 50 MHz | 1 |
| 50 – 80 MHz | 2 |
| 80 – 110 MHz | 3 |
| 110 – 140 MHz | 4 |
| 140 – 160 MHz | 5 |

**Figure 26. JTAG JCOMP timing**



4. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
5. $t_{SYS}$ is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min $t_{SYS}$ = 10 ns).
6. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
7. $t_{SDC}$ is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
8. PCSx and PCSS using same pad configuration.
9. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.
10. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

**Figure 31. DSPI CMOS master mode – classic timing, CPHA = 0**

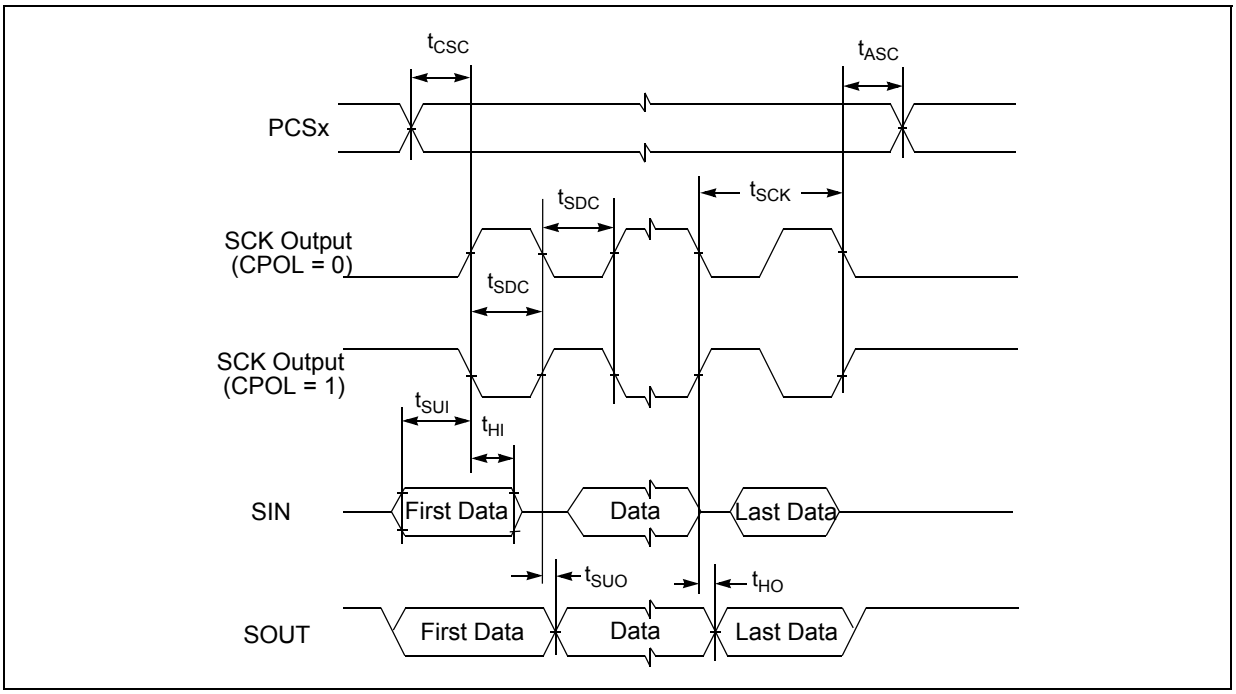


**Figure 34. DSPI CMOS master mode – modified timing, CPHA = 0**

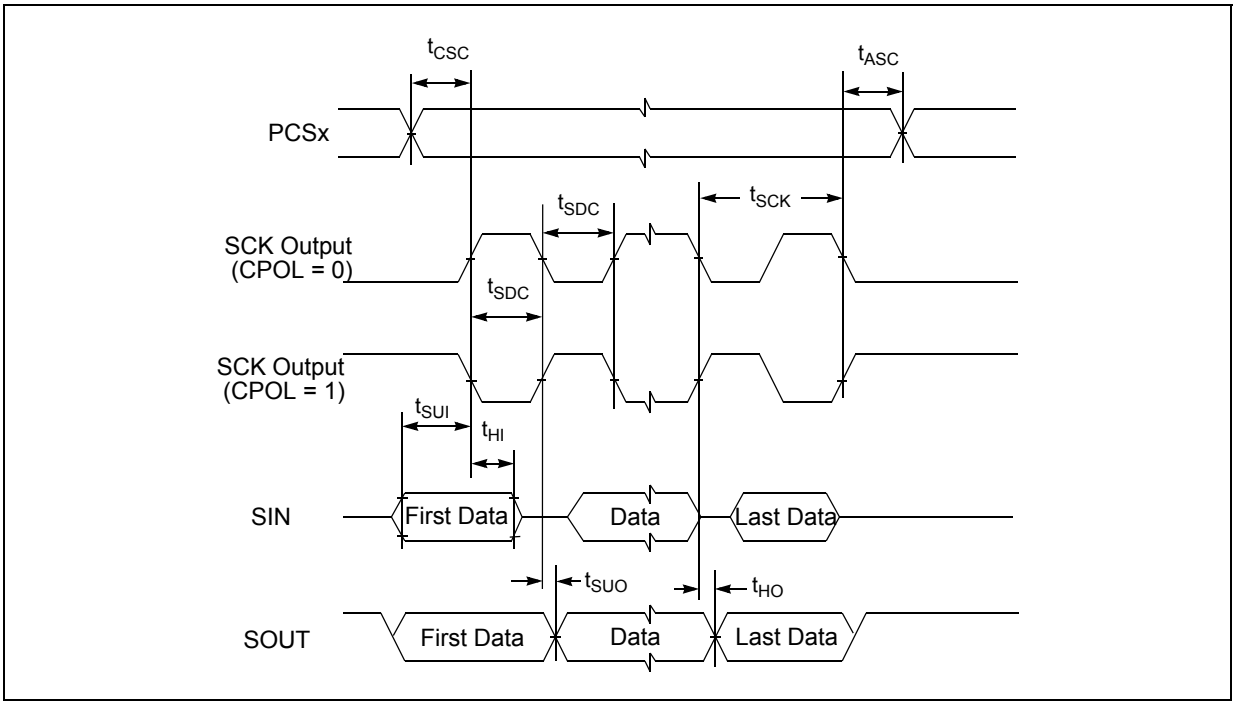



**Figure 35. DSPI CMOS master mode – modified timing, CPHA = 1**

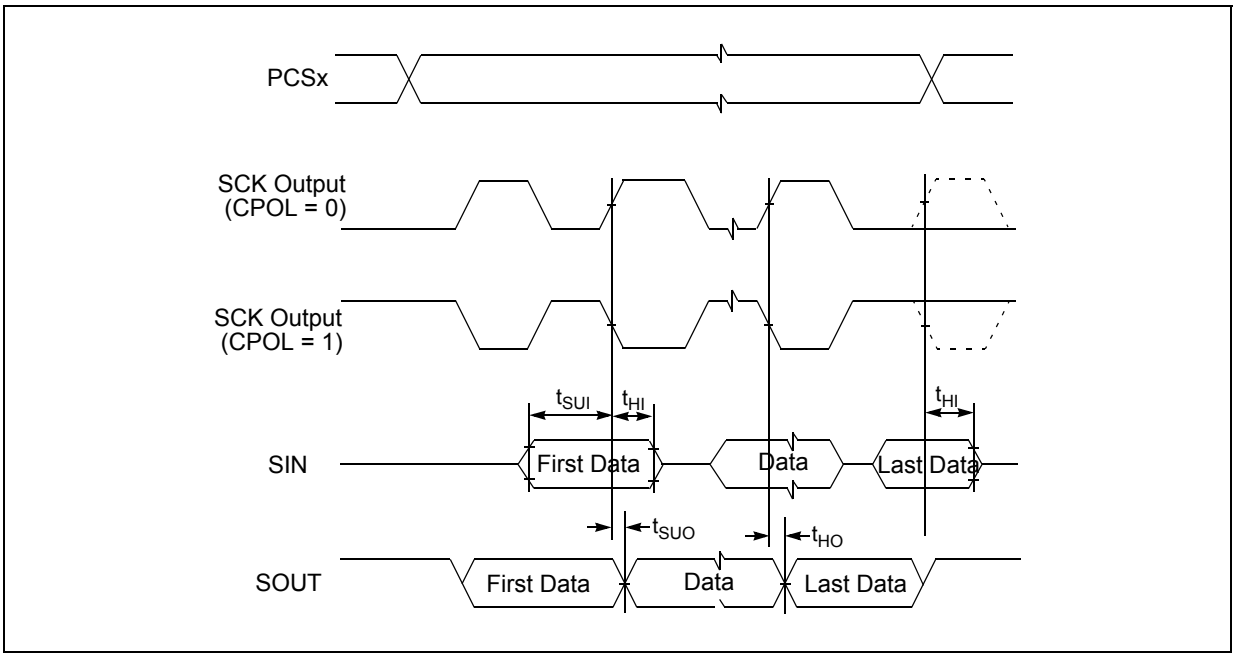
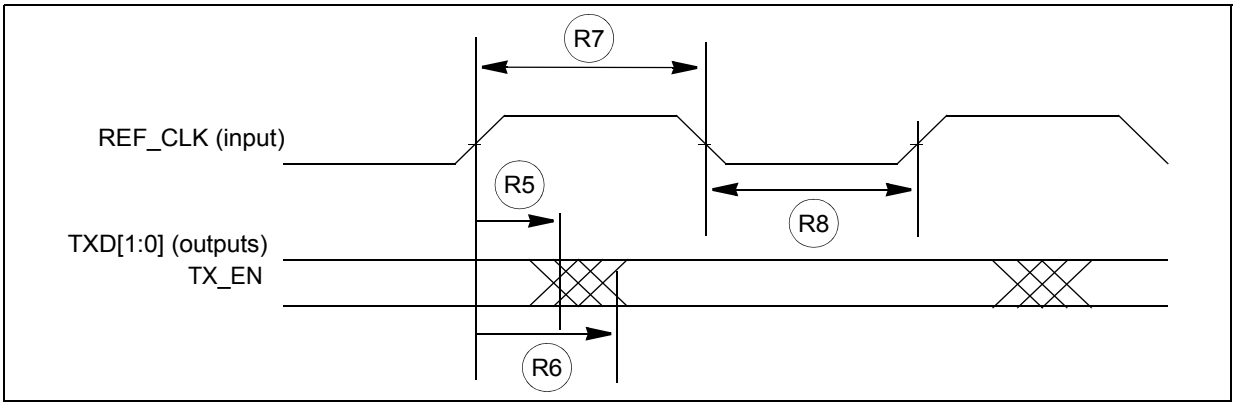


Figure 44. RMII transmit signal timing diagram




## 3.19.4 FlexRay timing

This section provides the FlexRay Interface timing characteristics for the input and output signals.

These are recommended numbers as per the FlexRay EPL v3.0 specification, and subject to change per the final timing analysis of the device.

### 3.19.4.1 TxEN

Figure 45. TxEN signal

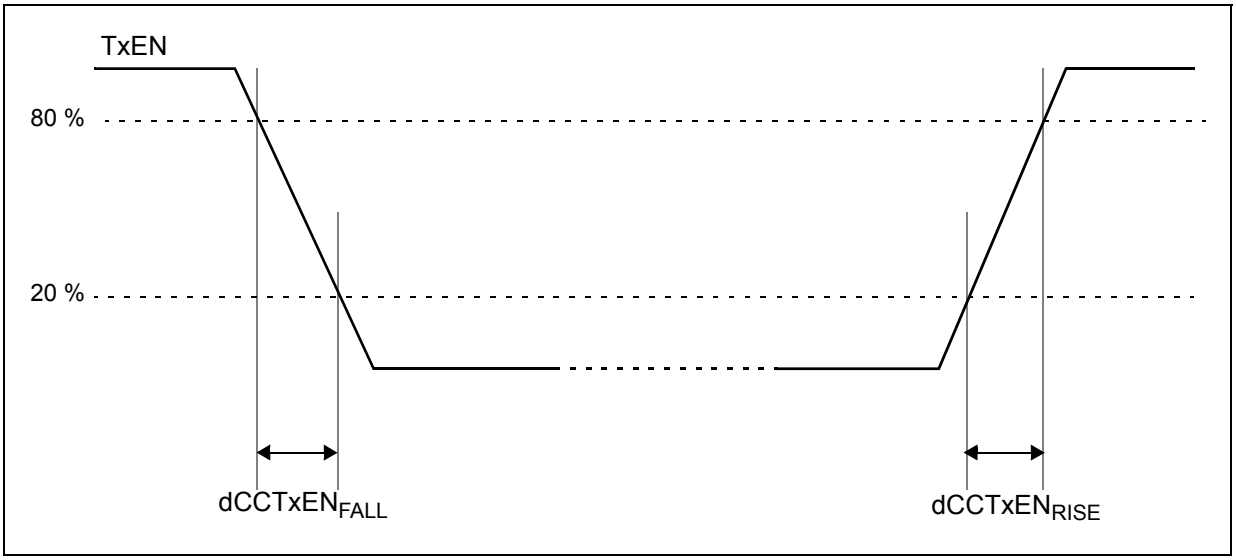



Table 62. TxEN output characteristics(1)

| Symbol | | C | Characteristic | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| dCCTxEN$_{RISE25}$ | CC | D | Rise time of TxEN signal at CC | — | 9 | ns |
| dCCTxEN$_{FALL25}$ | CC | D | Fall time of TxEN signal at CC | — | 9 | ns |

### 3.19.4.2 TxD

**Figure 47. TxD signal**

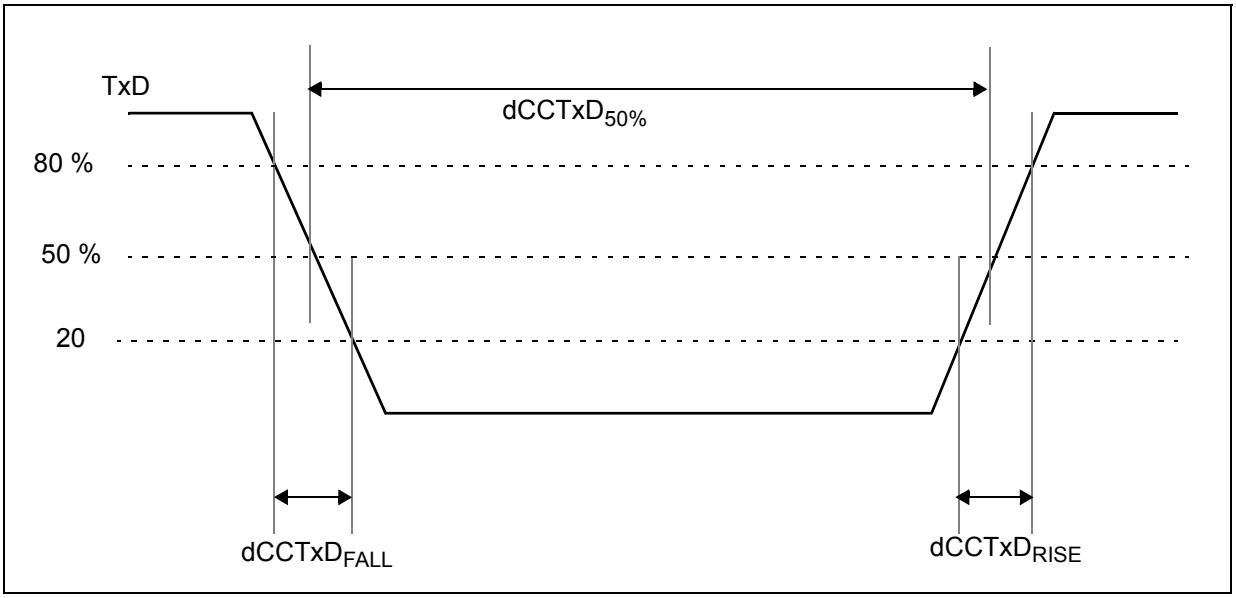
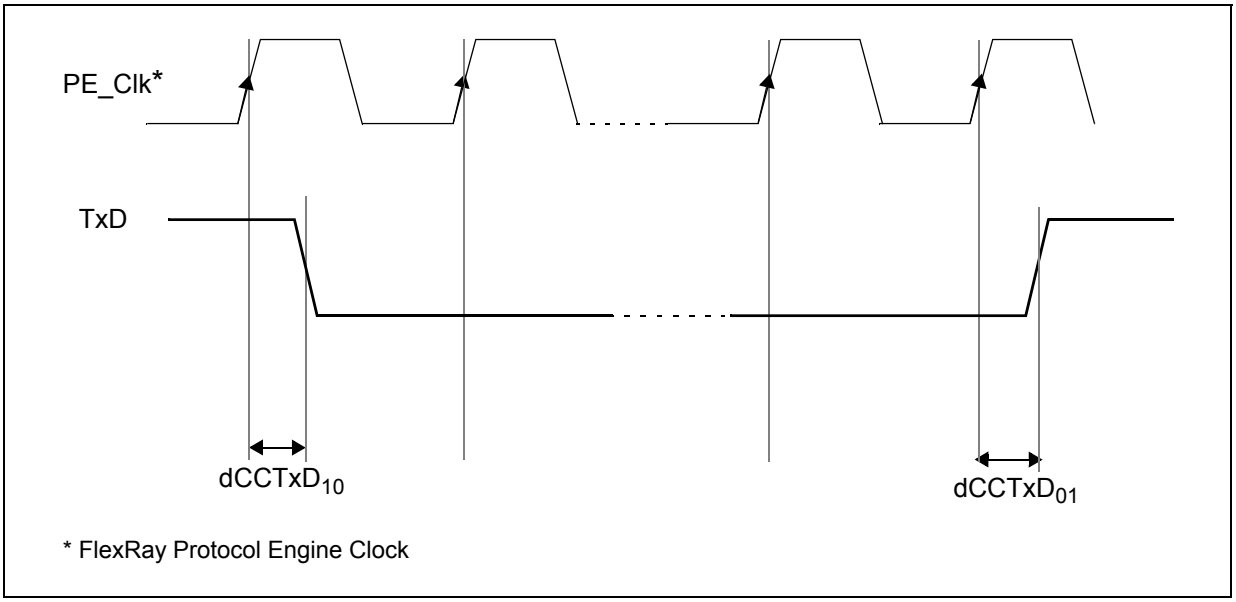



**Table 63. TxD output characteristics(1)(2)**

| Symbol | | C | Characteristic | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| dCCTxAsym | CC | D | Asymmetry of sending CC at 25 pF load (= $dCCTxD_{50\%}$ – 100 ns) | –2.45 | 2.45 | ns |
| $dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$ | CC | D | Sum of Rise and Fall time of TxD signal at the output pin(3),(4) | — | 9(5) | ns |
| | | D | | — | 9(6) | |
| $dCCTxD_{01}$ | CC | D | Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge | — | 25 | ns |
| $dCCTxD_{10}$ | CC | D | Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge | — | 25 | ns |

1. TxD pin load maximum 25 pF.
2. Specifications valid according to FlexRay EPL 3.0.1 standard with 20%–80% levels and a 10pF load at the end of a 50 Ohm, 1 ns stripline. Please refer to the Very Strong I/O pad specifications.
3. Pad configured as VERY STRONG.
4. Sum of transition time simulation is performed according to Electrical Physical Layer Specification 3.0.1 and the entire temperature range of the device has been taken into account.
5. $V_{DD\_HV\_IO}$ = 5.0 V ± 10%, Transmission line Z = 50 ohms, $t_{delay}$ = 1 ns, $C_L$ = 10 pF
6. $V_{DD\_HV\_IO}$ = 3.3 V ± 10%, Transmission line Z = 50 ohms, $t_{delay}$ = 0.6 ns, $C_L$ = 10 pF

**Figure 48. TxD Signal propagation delays**




### 3.19.4.3 RxD

**Table 64. RxD input characteristics(1)**

| Symbol | | C | Characteristic | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| C_CCRxD | CC | D | Input capacitance on RxD pin | — | 7 | pF |
| uCCLogic_1 | CC | D | Threshold for detecting logic high | 35 | 70 | % |
| uCCLogic_0 | CC | D | Threshold for detecting logic low | 30 | 65 | % |
| $dCCRxD_{01}$ | CC | D | Sum of delay from actual input to the D input of the first FF, rising edge | — | 10 | ns |
| $dCCRxD_{10}$ | CC | D | Sum of delay from actual input to the D input of the first FF, falling edge | — | 10 | ns |
| dCCRxAsymAccept15 | CC | D | Acceptance of asymmetry at receiving CC with 15 pF load | –31.5 | 44 | ns |
| dCCRxAsymAccept25 | CC | D | Acceptance of asymmetry at receiving CC with 25 pF load | –30.5 | 43 | ns |

1. FlexRay RxD timing is valid for CMOS input levels, hysteresis disabled, and $4.5\ V \le V_{DD\_HV\_IO} \le 5.5\ V$.

## 3.19.5 PSI5 timing

The following table describes the PSI5 timing.

**Table 72. Thermal characteristics for eLQFP176[1]**

| Symbol | | C | Parameter | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| $R_{\theta JA}$ | CC | D | Junction-to-ambient, natural convection[2] | Four layer board—2s2p | 25 | 28 | °C/W |
| $R_{\theta JMA}$ | CC | D | Junction-to-moving-air, ambient[2] | At 200 ft./min., four layer board—2s2p | 18 | 22 | °C/W |
| $R_{\theta JB}$ | CC | D | Junction-to-board[3] | — | 12 | 16 | °C/W |
| $R_{\theta JCtop}$ | CC | D | Junction-to-case top[4] | — | 12 | 15 | °C/W |
| $R_{\theta JCbottom}$ | CC | D | Junction-to-case bottom[5] | — | 1.5 | 3.5 | °C/W |
| $\Psi_{JT}$ | CC | D | Junction-to-package top[6] | Natural convection | 3 | 4.5 | °C/W |
| $P_d$ | CC | D | Device power dissipation | Maximum power and voltage condition | — | 2 | W |

1. The lower number in the ranges specified in the 'Value' column are based on simulation; actual data may vary in the given range. The specified characteristics are subject to change per final device design and characterization. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

### 4.5.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, $T_J$, can be obtained from the equation:

**Equation 3 $T_J = T_A + (R_{\theta JA} * P_D)$**

where:

$T_A$ = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$P_D$ = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

**Table 74. Revision history(Continued)**

| Revision | Date | Description of changes |
|---|---|---|
| 3 (cont'd) | 31 Jan 2014 | *Figure 41 (DSPI Slave Mode - Modified transfer format timing (MFTE = 0/1)—CPHA = 1)*: Changed figure title "(DSPI Slave Mode - Modified transfer format timing (MFTE = 1) — CPHA = 1)" to "(DSPI Slave Mode - Modified transfer format timing (MFTE = 0/1) — CPHA = 1)<br><br>*Figure 59 (144 LQFP-EP package mechanical drawing (1 of 3))*, *Figure 60 (144 LQFP-EP package mechanical drawing (2 of 3))*, *Figure 61 (144 LQFP-EP package mechanical drawing (3 of 3))*: Updated the figures.<br><br>*Figure 69 (172-pin FusionQuad® TQFP (1 of 4))*, *Figure 70 (172-pin FusionQuad® TQFP (2 of 4))*: Updated the figures.<br>Added 2 new figures: *Figure 71 (172-pin FusionQuad® TQFP (3 of 4))*, *Figure 72 (172-pin FusionQuad® TQFP (4 of 4))*.<br><br>In <Cross Refs>Equation 7 description,<br>$T_T$ updated to $T_B$ and $\Psi_{JT}$ updated to $\Psi_{PB}$ as mentioned in the equation.<br><br>*Table 59 (RMII serial management channel timing)*:<br>– Added note "RMII timing is valid only up to a maximum of 150 °C junction temperature" and applied K2 tag<br>– Added note "Output parameters are valid for CL = 25 pF, where CL is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value" to the value column and applied K2 tag<br><br>*Table 60 (RMII receive signal timing)*: Added note "RMII timing is valid only up to a maximum of 150 °C junction temperature"<br><br>*Table 61 (RMII transmit signal timing)*:<br>– R6 (REF_CLK to TXD[1:0], TX_EN valid) Max Value changed to 16 ns.<br>– Added footnote: *Output parameters are valid for...*<br>– Added note "RMII timing is valid only up to a maximum of 150 °C junction temperature"<br>– Updated table footnotes<br><br>*Table 64 (RxD input characteristics)*: Added footnote 1 "FlexRay RxD timing is valid for all input levels and hysteresis disabled."<br><br>*Table 71 (Thermal characteristics for eTQFP144)*:<br>– All table Min and Max values revised.<br><br>*Table 84 (Thermal characteristics for FQ172(144/28) FusionQuad® package)*:<br>– All table Min and Max values revised.<br><br>*Table 72 (Thermal characteristics for eLQFP176)*:<br>– All table Min and Max values revised.<br><br>*Table 86 (Thermal characteristics for FQ216(176/40) FusionQuad® package)*:<br>– All table Min and Max values revised.<br><br>*Section 4, Package characteristics*: Added *Table 70 (Package case numbers)* |

**Table 74. Revision history(Continued)**

| Revision | Date | Description of changes |
|---|---|---|
| 4 (cont'd) | 19 Dec 2014 | *Figure 9 (I/O output DC electrical characteristics definition)*:<br>– Updated the figure. $t_{PD10-90}$ (rising edge) replaced by $t_{PLH}$ (rising edge) and $t_{PD10-90}$ (falling edge) replaced by $t_{PHL}$ (falling edge). Added 50% dotted line.<br><br>*Table 20 (WEAK configuration output buffer electrical characteristics)*:<br>– Replaced the minimum value of $R_{OH\_W}$ with "520" from "560".<br><br>*Table 22 (STRONG configuration output buffer electrical characteristics)*:<br>– Added $\|t_{SKEW\_S}\|$ parameter.<br><br>*Table 23 (VERY STRONG configuration output buffer electrical characteristics)*:<br>– Added $I_{DCMAX\_VS}$ specification.<br><br>*Table 25 (Reset electrical characteristics)*:<br>– For $V_{HYS}$, replaced minimum value "300" with "275".<br>– For $W_{FNMI}$, replaced maximum value "20" with "15".<br><br>*Table 26 (PLL0 electrical characteristics)*:<br>– In $f_{PLL0IN}$ added a second note to parameter column.<br><br>*Table 27 (PLL1 electrical characteristics)*:<br>– Removed $t_{PLL1JIT}$.<br>– Updated all the minimum and maximum values of $g_m$.<br>– Removed note 6 from below the table.<br><br>*Table 28 (External Oscillator electrical specifications)*:<br>– In $g_m$, changed the minimum and maximum frequencies.<br><br>*Table 30 (Internal RC oscillator electrical specifications)*:<br>– Moved the footnote from $\delta f_{var\_T}$ to $\delta f_{var\_SW}$.<br>– Updated the description of $\delta f_{var\_SW}$.<br>– Removed $I_{AVDD5}$.<br>– Removed $I_{DVDD12}$.<br><br>Table 26 (SARn ADC electrical specification):<br>– Added $\Delta TUE_{10}$.<br>– For $V_{ALTREF}$ replaced "P" with "C" and added another row for "P".<br>– For $I_{ADV\_S}$, reorganised the notes and added a note to "Power Down mode".<br>– Changed the minimum and maximum value of DNL.<br>– Removed INL.<br>– Revised condition entries for $t_{ADCPRECH}$ and $\Delta V_{PRECH}$.<br><br>*Table 34 (SDn ADC electrical specification)*:<br>– Updated $SNR_{SE150}$.<br>– In $V_{cmrr}$ specification: changed min value to 54 dB (was 20 dB).<br>– Replaced "$V_{cmrr}$" with "CMRR".<br>– $\delta_{GROUP}$ specification: changed OSR = 75 max value to 699 Tclk (was 646), changed OSR = 96 max value to 949.5 Tclk (was 946.4).<br>– $V_{OFFSET}$: Changed parameter name to "Input Referred Offset Error" (was "Conversion Offset") and added footnote ("Conversion offset error must be..."). |