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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z2, e200z4, e200z4
Core Size	32-Bit Tri-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, FlexRay, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12b SAR, 16b Sigma-Delta
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP Exposed Pad
Supplier Device Package	144-eTQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc574k72e5c6fay

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1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the SPC574Kx series of microcontroller units (MCUs). For functional characteristics, see the SPC574Kx microcontroller reference manual.

1.2 Description

This family of MCUs targets automotive powertrain controller applications for four-cylinder gasoline and diesel engines, chassis control applications, transmission control applications, steering and braking applications, as well as low-end hybrid applications.

Many of the applications are considered to be functionally safe and the family is designed to achieve ISO26262 ASIL-D compliance.

1.3 Device feature summary

Table 2. SPC574Kx device feature summary

Feature		Description
Process		55 nm
Main processor	Core	e200z4
	Number of main cores	1
	Number of checker cores	1
	Local RAM (per main core)	16 KB Instruction 64 KB Data
	Single precision floating point	Yes
	VLE	Yes
	Cache	4 KB Instruction 2 KB Data
I/O processor	Core	e200z2
	Local RAM	16 KB Instruction 48 KB Data
	Single precision floating point	Yes
	LSP	Yes
	VLE	Yes
	Cache	No
Main processor frequency		160 MHz
I/O processor frequency		80 MHz
MPU		Yes

Table 10. RF immunity—Direct Power Injection (DPI) test specifications(1)(Continued)

Module	Signal	Monitor pin	Function	BISS signal/power supply limit class
VDD regulator	$V_{DD\_HV\_PMC}$	Power	C10	0 dBm
VDD Flash	$V_{DD\_HV\_FLA}$	Power	C10	12 dBm
VDD JTAG/OSC	$V_{DD\_HV\_IO\_JTAG}$	Power	C10	0 dBm

1. Reference “BISS Generic IC EMC Test Specification”, section 9.4, “Immunity test configuration for ICs with CPU”.

3.4.1 BISS port and power supply limits

Figure 5 shows the BISS port limits behavior and *Figure 6* shows BISS power supply limits behavior. Class limits apply to signal under test in static mode only.

All pins of the microcontroller are defined as ‘Local’ (according to BISS specification). Therefore, the supply pins on the microcontroller are tested to ‘Local’ requirements.

Figure 5. BISS port limits

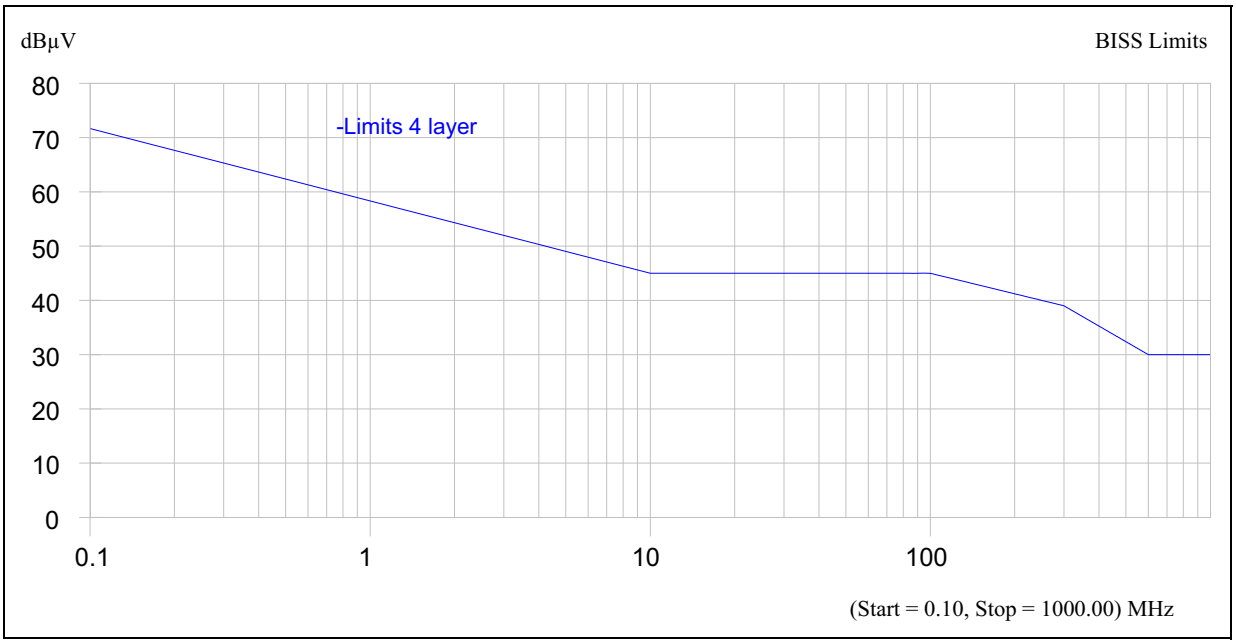
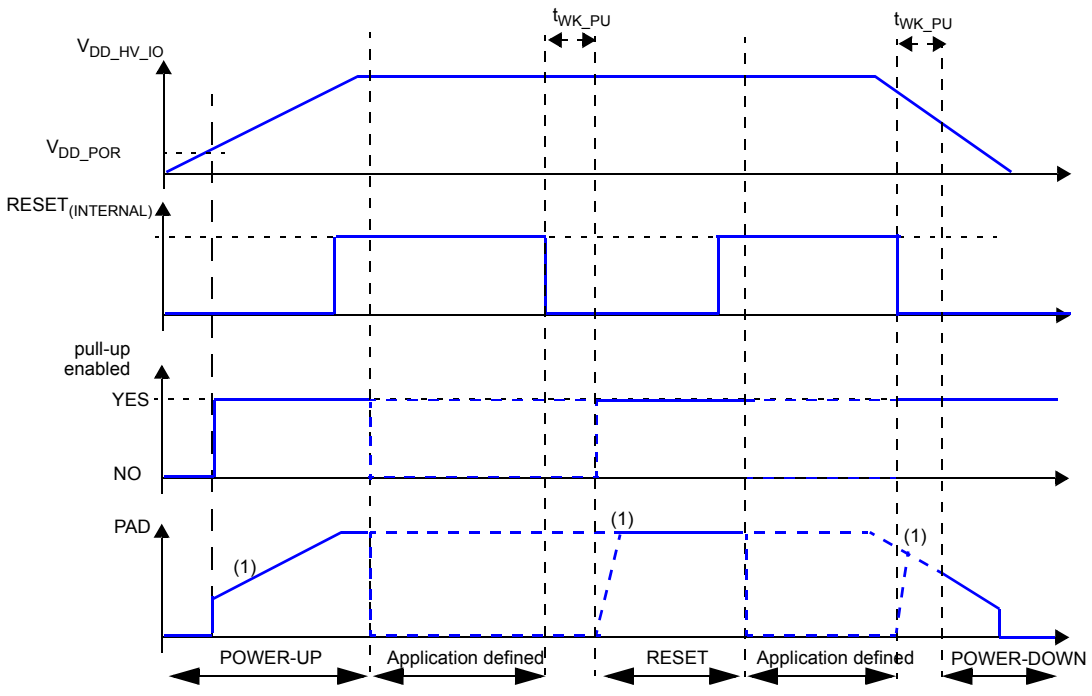


Figure 8. Weak pull-up electrical characteristics definition



1. Actual PAD slopes will depend on external capacitances and VDD_HV_IO supply.

3.9.2 I/O output DC characteristics

The figure below provides description of output DC electrical characteristics.

5. Only for $V_{DD\_HV\_IO\_JTAG}$ segment when VSIO[VSIO_IJ] = 0 or $V_{DD\_HV\_IO\_FLEX}$ segment when VSIO[VSIO_IF] = 0

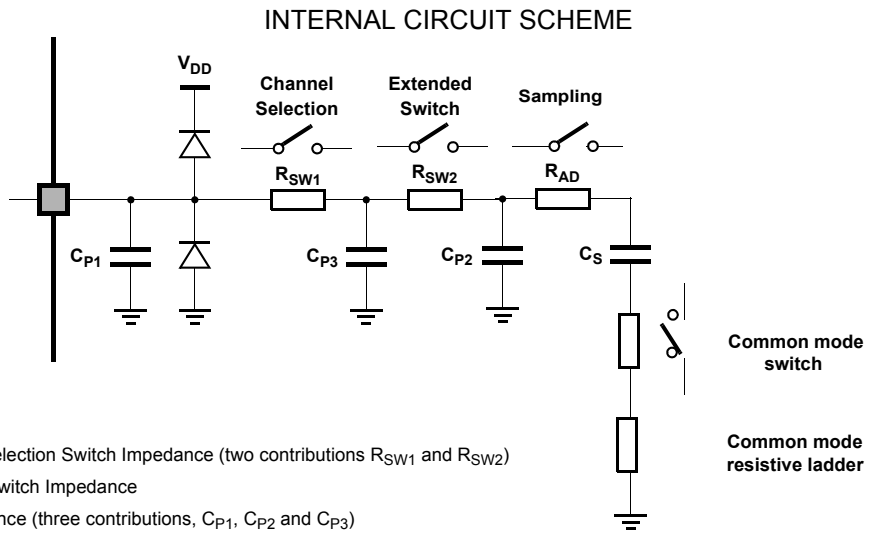
Table 22 shows the STRONG configuration output buffer electrical characteristics.

Table 22. STRONG configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
R_{OH_S}	CC	P	PMOS output impedance STRONG configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OH} < 8 mA	—	—	70	Ω
R_{OL_S}	CC	P	NMOS output impedance STRONG configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OL} < 8 mA	—	—	70	Ω
f_{MAX_S}	CC	T	Output frequency STRONG configuration	C_L = 25 pF[3]	—	—	40	MHz
				C_L = 50 pF[4]	—	—	20	
				C_L = 200 pF[4]	—	—	5	
t_{TR_S}	CC	T	Transition time output pin STRONG configuration[4]	C_L = 25 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	2.5	—	10	ns
				C_L = 50 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	3.5	—	16	
				C_L = 200 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	13	—	50	
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	4	—	15	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	6	—	27	
				C_L = 200 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	20	—	83	
I_{DCMAX_S}	CC	D	Maximum DC current	—	—	—	10	mA
$\|t_{SKEW\_S}\|$	CC	T	Difference between rise and fall time	—	—	—	25	%
$T_{PHL/PLH}$	CC	D	Propagation delay	C_L = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	12	ns
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	18	
				C_L = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	20	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	—	—	36	

1. All VDD_HV_IO conditions for 4.5V to 5.5V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0V to 3.6V are valid for VSIO[VSIO_xx] = 0
2. All values need to be confirmed during device validation.

Figure 16. Input equivalent circuit (SARB channels)



R_{SW}: Channel Selection Switch Impedance (two contributions R_{SW1} and R_{SW2})

R_{AD}: Sampling Switch Impedance

C_P: Pin Capacitance (three contributions, C_{P1}, C_{P2} and C_{P3})

C_S: Sampling Capacitance

R_{CMSW}: Common mode switch

R_{CML}: Common mode resistive ladder

The above figure can be used as approximation circuitry for external filtering definition.

Table 31. ADC pin specification(1)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
I_{LK_INUD}	CC	C	Input leakage current, two ADC channels input with weak pull-up and weak pull-down	T_J < 40 °C, no current injection on adjacent pin	—	70	nA
		C		T_J < 150 °C, no current injection on adjacent pin	—	220	
I_{LK_INUSD}	CC	C	Input leakage current, two ADC channels input with weak pull-up and strong pull-down	T_J < 40 °C, no current injection on adjacent pin	—	80	nA
		C		T_J < 150 °C, no current injection on adjacent pin	—	250	
I_{LK_INREF}	CC	C	Input leakage current, two ADC channels input with weak pull-up and weak pull-down and alternate reference	T_J < 40 °C, no current injection on adjacent pin	—	160	nA
		C		T_J < 150 °C, no current injection on adjacent pin	—	400	
I_{LK_INOUT}	CC	C	Input leakage current, two ADC channels input, GPIO output buffer with weak pull-up and weak pull-down	T_J < 40 °C, no current injection on adjacent pin	—	140	nA
		C		T_J < 150 °C, no current injection on adjacent pin	—	380	
I_{INJ}	CC	T	Injection current on analog input preserving functionality	Applies to any analog pins	–3	3	mA
C_{HV_ADC}	SR	D	$V_{DD\_HV\_ADV}$ external capacitance(2)	—	1	2.2	µF

1. All specifications in this table valid for the full input voltage range for the analog inputs.
2. For noise filtering, add a high frequency bypass capacitance of 0.1 µF between $V_{DD\_HV\_ADV}$ and $V_{SS\_HV\_ADV}$.
3. Safety pull-down is available for port pin PB[5] and PE[14]. It enables discharge of up to 100 nF from 5 V every 300 ms.

The SARn ADCs are 12-bit Successive Approximation Register analog-to-digital converters with full capacitive DAC. The SARn architecture allows input channel multiplexing.

Table 33. SARn ADC electrical specification(1)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{ALTREF}	SR	C	ADC alternate reference voltage	$V_{ALTREF} < V_{DD\_HV\_IO\_MAIN}$ $V_{ALTREF} < V_{DD\_HV\_ADV}$	4.5	5.5	V
		C			4.0	5.9	
		P		Extended range with reduce TUE $V_{ALTREF} < V_{DD\_HV\_IO\_MAIN}$ $V_{ALTREF} < V_{DD\_HV\_ADV}$	2.0	5.9	
V_{IN}	SR	D	ADC input signal	$0 < V_{IN} < V_{DD\_HV\_IO\_MAIN}$	$V_{SS\_HV\_ADR}$	$V_{DD\_HV\_ADR}$	V
f_{ADCK}	SR	P	Clock frequency	$T_J < 150$ °C	7.5	14.6	MHz
$t_{ADCPRECH}$	SR	T	ADC precharge time	Fast SAR—fast precharge	135	—	ns
				Fast SAR—full precharge	270	—	
				Slow SAR (SARADC_B)—fast precharge	270	—	
				Slow SAR (SARADC_B)—full precharge	540	—	
ΔV_{PRECH}	SR	D	ADC Precharge voltage	Full precharge $V_{PRECH} = V_{DD\_HV\_ADR}/2$ $T_J < 150$ °C	–0.25	0.25	V
		D		Fast precharge $V_{PRECH} = V_{DD\_HV\_ADR}/2$ $T_J < 150$ °C	–0.5	0.5	V
ΔV_{INTREF}	CC	P	Internal reference voltage precision	Applies to all internal reference points ($V_{SS\_HV\_ADR}$, 1/3 * $V_{DD\_HV\_ADR}$, 2/3 * $V_{DD\_HV\_ADR}$, $V_{DD\_HV\_ADR}$)	–0.20	0.20	V
$t_{ADCSAMPLE}$	SR	P	ADC sample time(2)	Fast SAR – 12-bit configuration	0.750	—	µs
		D		Fast SAR – 10-bit configuration	0.555	—	
		P		Slow SAR (SARADC_B) – 12-bit configuration	1.500	—	
		D		Slow SAR (SARADC_B) – 10-bit configuration	0.833	—	

Table 33. SARn ADC electrical specification[1](Continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
$t_{ADCEVAL}$	SR	P	ADC evaluation time	12-bit configuration (25 clock cycles)	1.712	—	µs
		D		10-bit configuration (21 clock cycles)	1.458	—	
I_{ADCSAR_REFH}[3],[4]	CC	T	ADC high reference current	Dynamic consumption (t_{conv} = 5 µs[5])	—	3.5[6]	µA
				Dynamic consumption (t_{conv} = 2.5 µs[6])	—	7	
				Static consumption (Power Down mode)	—	4	
				Bias Current[7]	—	+2	
I_{ADCSAR_REFL}[4]	CC	D	ADC low reference current	Run mode $t_{conv} \geq 5$ µs $V_{DD\_HV\_ADR}$ <= 5.5 V	—	15	µA
				Run mode t_{conv} = 2.5 µs $V_{DD\_HV\_ADR}$ <= 5.5 V	—	30	
				Power Down mode $V_{DD\_HV\_ADR}$ <= 5.5 V	—	1	
I_{ADV_S}	CC	T	$V_{DD\_HV\_ADV}$ power supply current (each ADC)	Dynamic consumption (t_{conv} = 5 µs)	—	4.0	mA
				Dynamic consumption (t_{conv} = 2.5 µs)	—	4.0	
TUE_{12}	CC	T[8]	Total unadjusted error in 12-bit configuration[9]	T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 4 V, $V_{DD\_HV\_ADR}$ > 4 V	–4	4	LSB (12b)
		P		T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 4 V, $V_{DD\_HV\_ADR}$ > 4 V	–6	6	
		T		T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 4 V, 4 V > $V_{DD\_HV\_ADR}$ > 2 V	–6	6	
		T		T_J < 150 °C, 4 V > $V_{DD\_HV\_ADV}$ > 3.5 V	–12	12	
TUE_{10}	CC	C	Total unadjusted error in 10-bit configuration	T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 4 V $V_{DD\_HV\_ADR}$ > 4 V	–1.5	1.5	LSB (10b)
		C		T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 4 V, 4 V > $V_{DD\_HV\_ADR}$ > 2 V	–2.0	2.0	

Table 34. SDn ADC electrical specification(1)(Continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$SNR_{DIFF150}$(9)	CC	T	Signal to noise ratio in differential mode 150 ksps output rate	$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 1 $T_J < 150$ °C	80	—	—	dBFS
		T		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11), $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 2 $T_J < 150$ °C	77	—	—	
		T		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11), $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 4 $T_J < 150$ °C	74	—	—	
		T		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 8 $T_J < 150$ °C	71	—	—	
		D		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 16 $T_J < 150$ °C	68	—	—	
$SNR_{DIFF333}$ (12)	CC	P	Signal to noise ratio in differential mode 333 ksps output rate	$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 1 $T_J < 150$ °C	74	—	—	dBFS
		T		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 2 $T_J < 150$ °C	71	—	—	
		T		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 4 $T_J < 150$ °C	68	—	—	
		T		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 8 $T_J < 150$ °C	65	—	—	
		D		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 16 $T_J < 150$ °C	62	—	—	

Figure 19. Power-down exit time

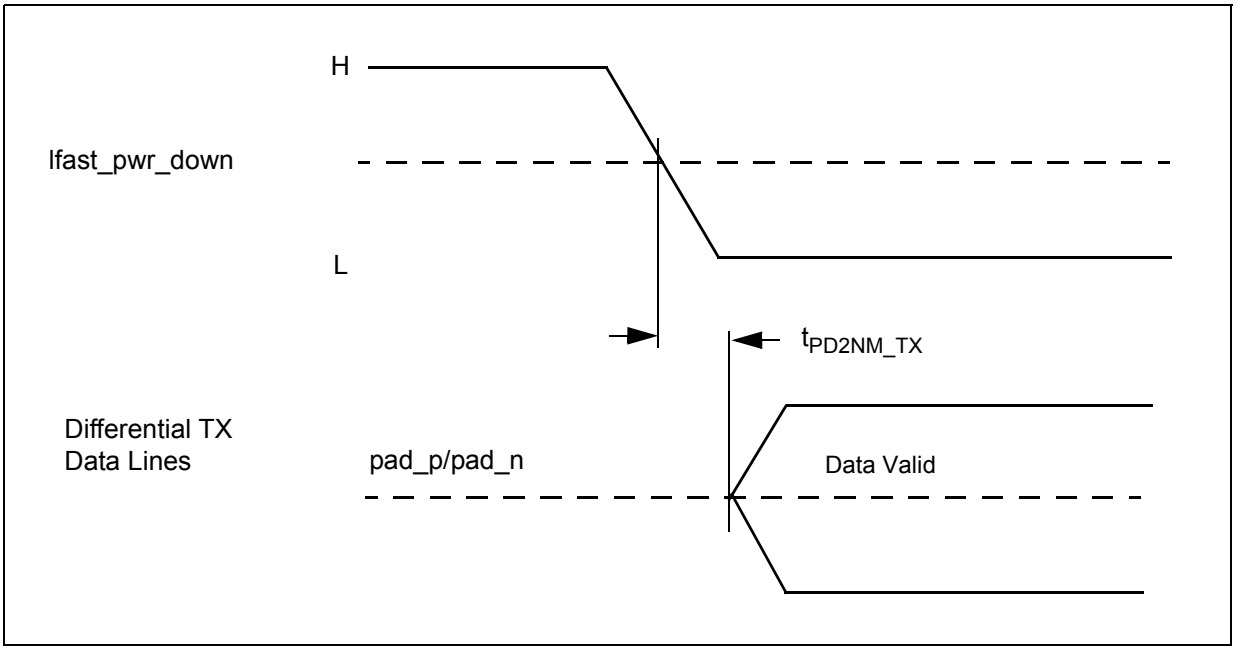
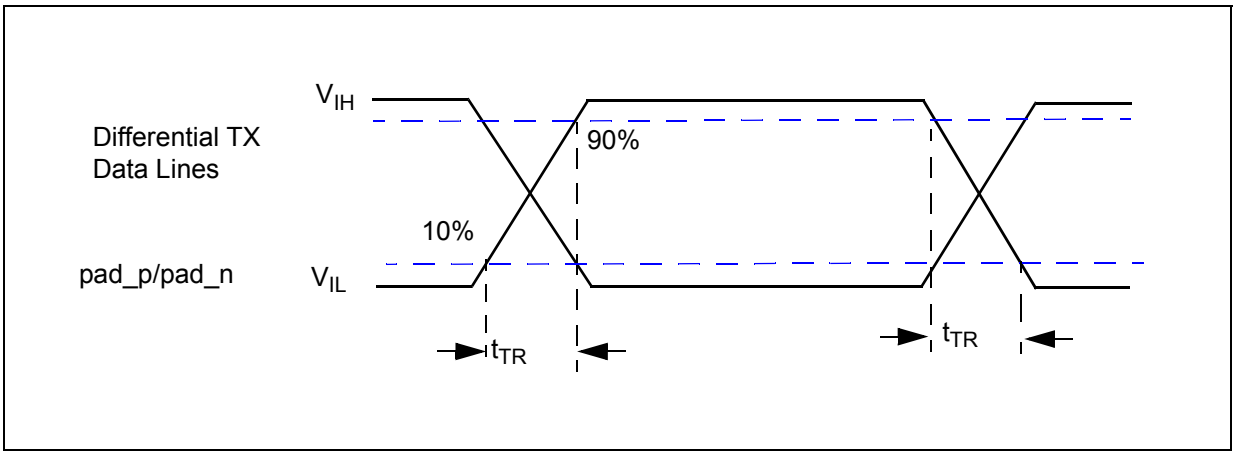


Figure 20. Rise/fall time



3.15.2 LFAST and MSC/DSPI LVDS interface electrical characteristics

The following table contains the electrical characteristics for the LFAST interface.

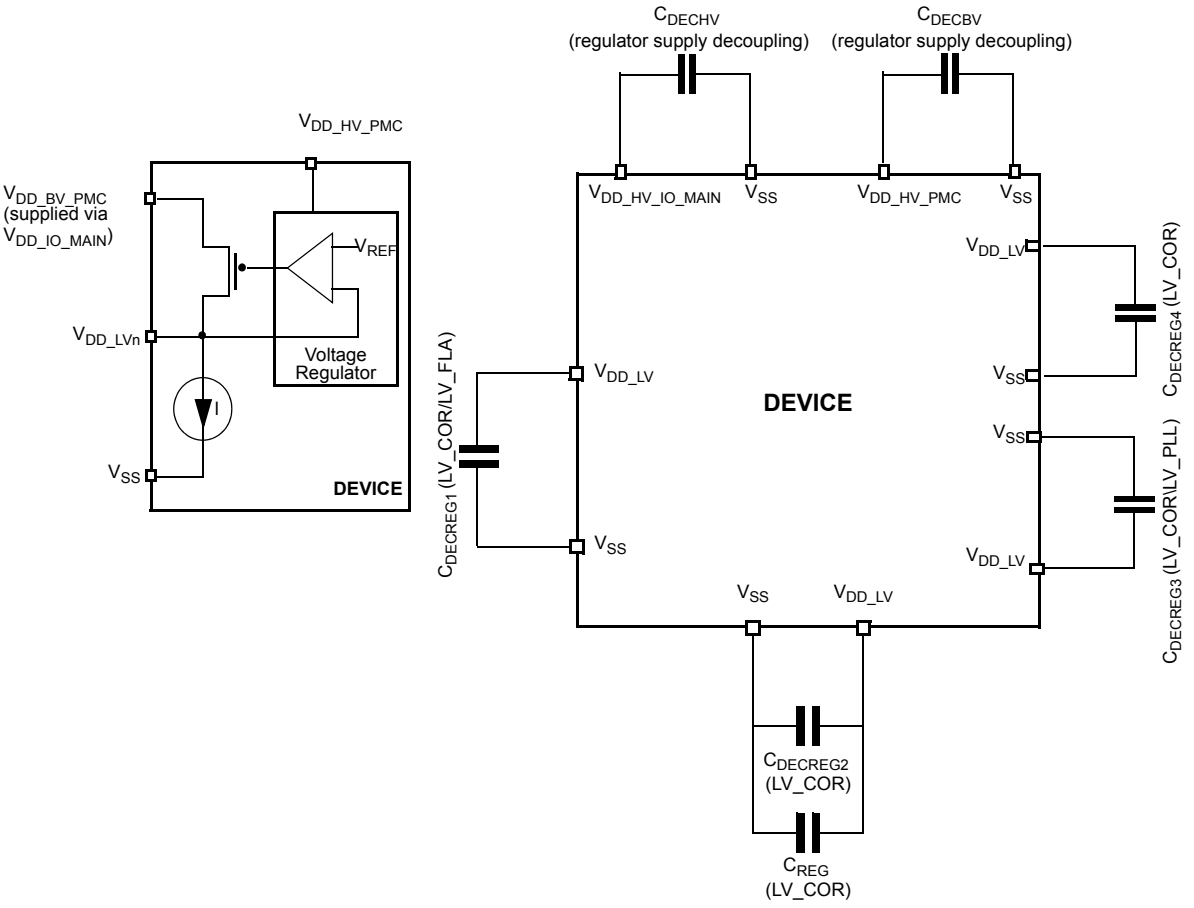
Table 36. LVDS pad startup and receiver electrical characteristics(1)(2)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
STARTUP(3),(4)								
t_{STRT_BIAS}	CC	T	Bias current reference startup time(5)	—	—	0.5	4	µs
t_{PD2NM_TX}	CC	T	Transmitter startup time (power down to normal mode)(6)	—	—	0.4	2.75	µs

3.17.1 Power management integration

Use the integration scheme provided below to ensure proper device function.

Figure 22. Voltage regulator capacitance connection



Note: The pins positions correspond to the pins positions in the pins package.

The internal voltage regulator requires external capacitance (C_{REGn}) to be connected to the device to provide a stable low voltage digital supply to the device. Placed capacitances on the board as near as possible to the associated pins and limit the serial inductance of the board to less than 5 nH.

Place a decoupling capacitor between each V_{DD_LV} supply pin and V_{SS} ground plane to ensure stable voltage. Place the capacitor as near as possible to the V_{DD_LV} supply pin.

3.17.2 Main voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage ballast supply $V_{DD\_BV\_PMC}$, internally connected to $V_{DD\_HV\_IO\_MAIN}$ supply. The regulator itself is supplied by $V_{DD\_HV\_PMC}$. Both high voltage supplies are common with $V_{DD\_HV\_IO}$.

Note: Refer to SPC574Kx_IO_Signal_Table.xls table for details regarding power connectivity.

Table 46. Flash memory Life Specification(Continued)

Symbol	Characteristics[1]	Value				Unit
		Min	C	Typ	C	
$N_{CER256K}$	256 KB CODE Flash endurance	1	—	100	—	kcycles
N_{DER16K}	16 KB EEPROM Flash endurance	250	—	—	—	kcycles
t_{DR1k}	Minimum data retention Blocks with 0 - 1,000 P/E cycles	20	—	—	—	Years
t_{DR10k}	Minimum data retention Blocks with 1,001 - 10,000 P/E cycles	20	—	—	—	Years
t_{DR250k}	Minimum data retention Blocks with 10,001 - 250,000 P/E cycles	10	—	—	—	Years

1. Program and erase cycles supported across specified temperature specs.

3.18.1 Flash read wait state and address pipeline control settings

Table 47 describes the recommended RWSC settings at various operating frequencies based on specified intrinsic flash access times of the Flash array at 150 °C.

Table 47. Flash memory RWSC configuration

Platform Frequency	Minimum RWSC settings
0 – 25 MHz	0
25 – 50 MHz	1
50 – 80 MHz	2
80 – 110 MHz	3
110 – 140 MHz	4
140 – 160 MHz	5

Figure 26. JTAG JCOMP timing

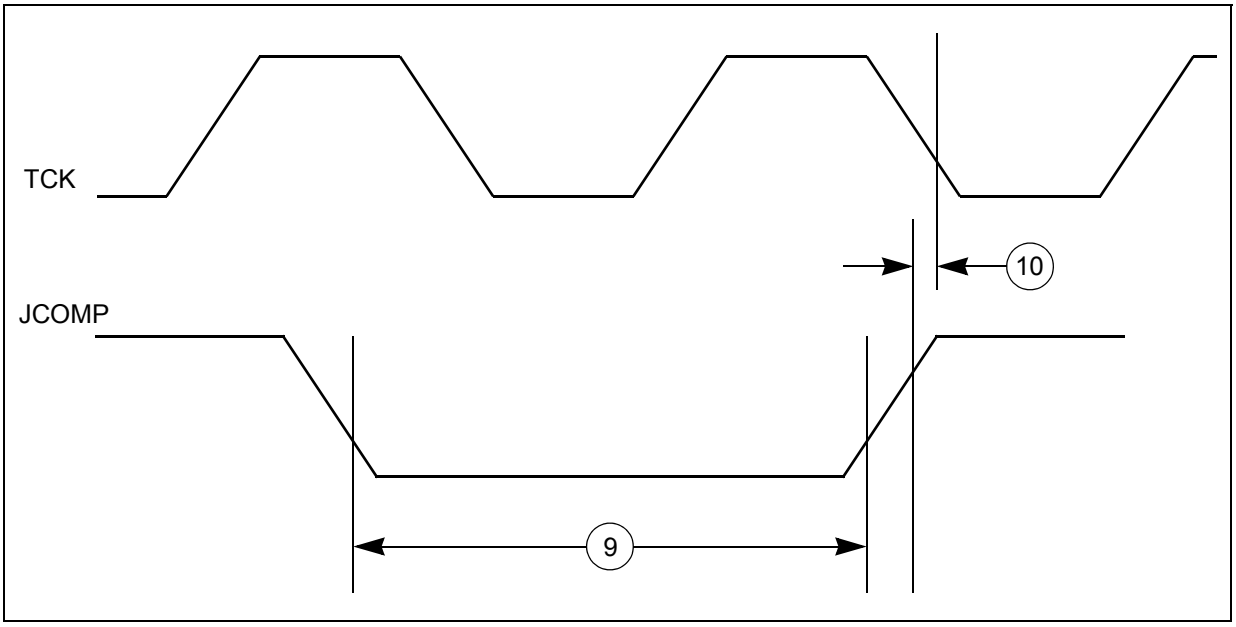
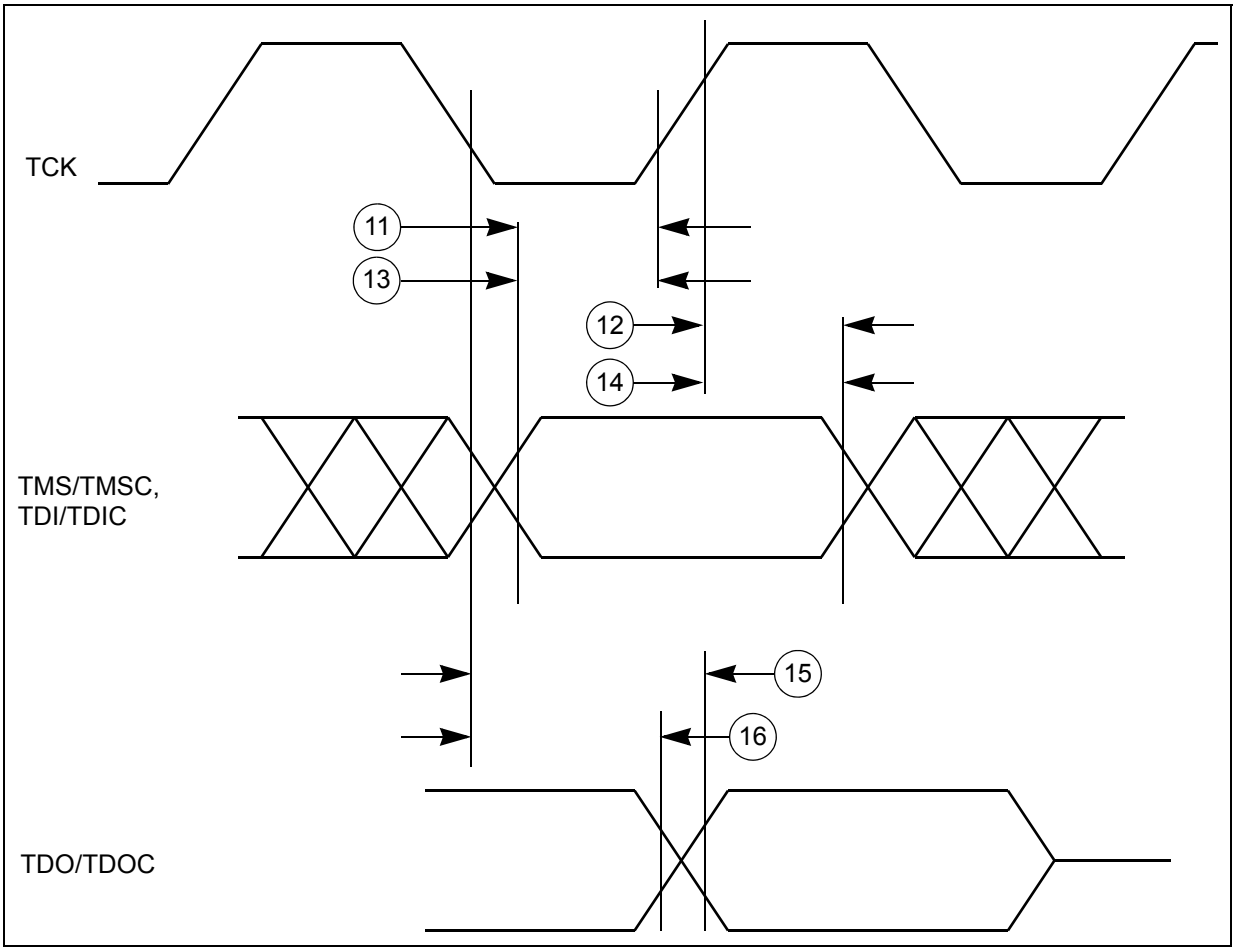


Figure 29. Nexus TDI/TDIC, TMS/TMSC, TDO/TDOC timing



3.19.1.3 Aurora LVDS interface timing

Table 50. Aurora LVDS interface timing specifications

Symbol		C	Parameter	Value			Unit
				Min	Typ	Max	
Data Rate							
—	SR	T	Data rate	—	—	1250	Mbps
STARTUP							
t_{STRT_BIAS}	CC	T	Bias startup time(1)	—	—	5	µs
t_{STRT_TX}	CC	T	Transmitter startup time(2)	—	—	5	µs
t_{STRT_RX}	CC	T	Receiver startup time(3)	—	—	4	µs

1. Startup time is defined as the time taken by LVDS current reference block for settling bias current after its pwr_down (power down) has been deasserted. LVDS functionality is guaranteed only after the startup time.
2. Startup time is defined as the time taken by LVDS transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.

Figure 37. DSPI LVDS master mode – modified timing, CPHA = 0

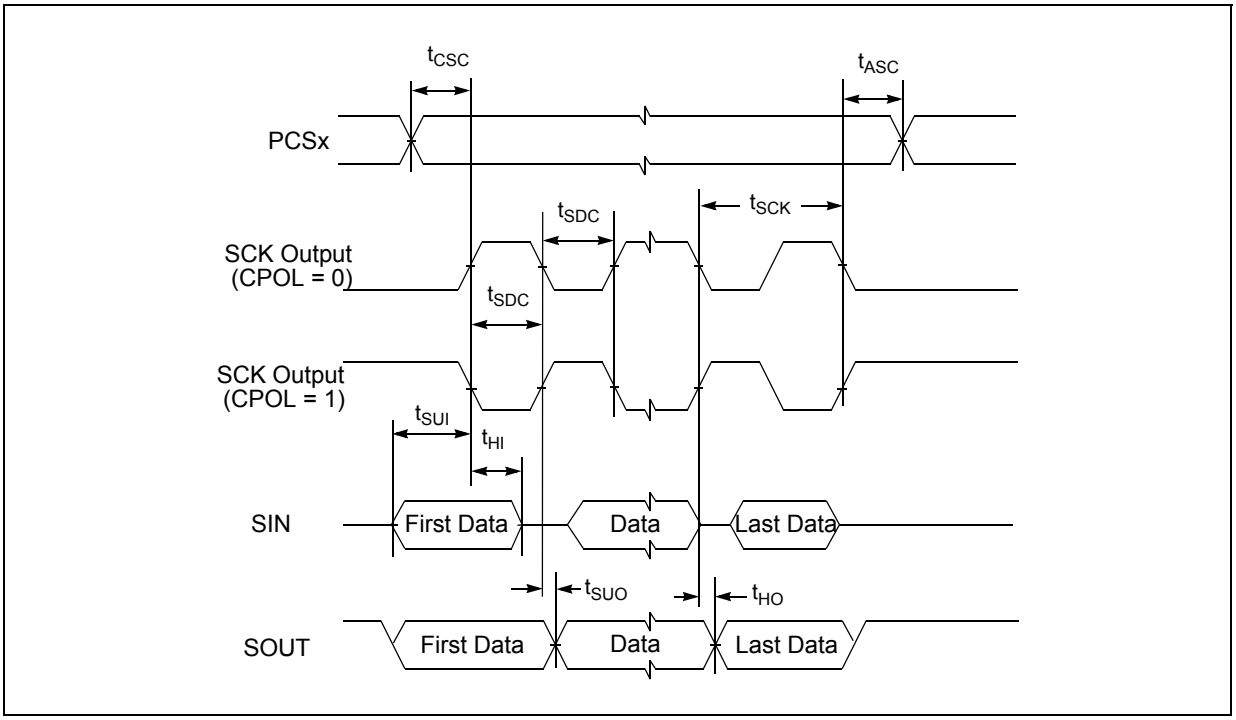


Figure 38. DSPI LVDS master mode – modified timing, CPHA = 1

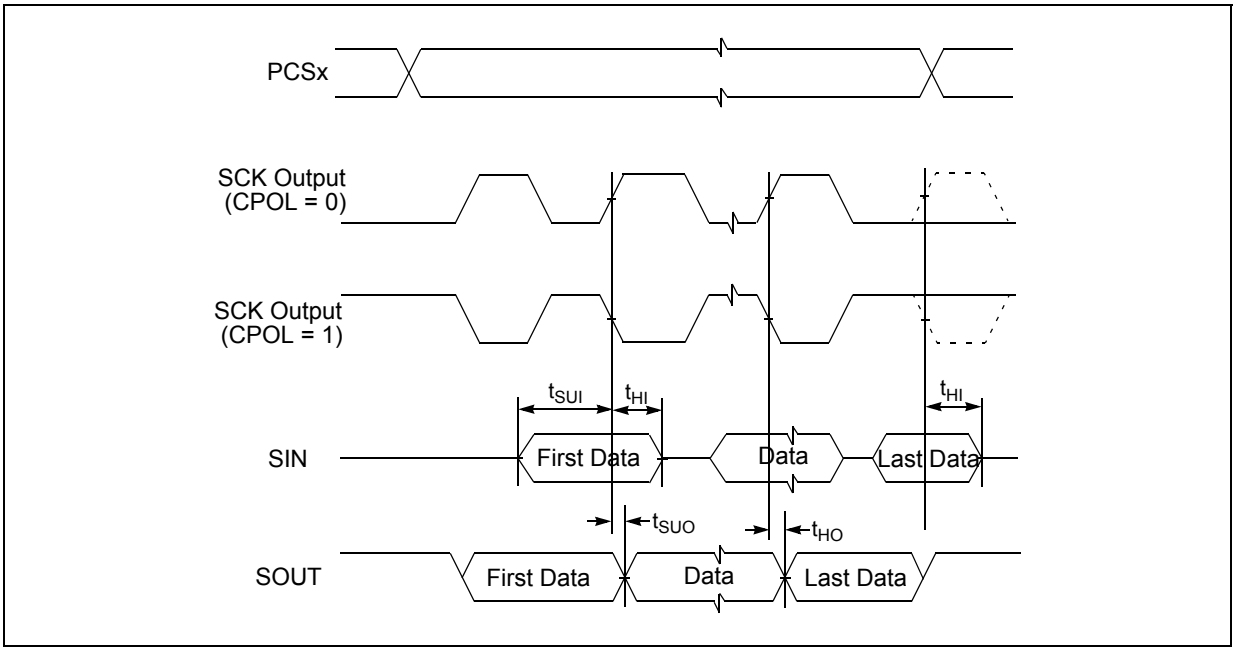


Table 74. Revision history(Continued)

Revision	Date	Description of changes
3 (cont'd)	31 Jan 2014	*Table 16 (DC electrical specifications)*: – In row I_{DDAPP} Condition f_{SYS} changed to 160 MHz, Condition T_J changed to 144 °C, Max Value changed to 260. – Footnote *fMAX as specified...application specific pattern* changed to *application with maximum consumption...* – Footnote *fMAX as specified...with active flash...* changed to *Application with maximum consumption...with active flash...* – Parameter classification of "I_{DDPE}" changed to "C". – Parameter classification of "I_{SPIKE}" changed to "T". – Parameter classification of "dI" changed to "T". – Parameter classification of "I_{SR}" changed to "D". – 3 new parameters "$I_{DD\_MAIN\_CORE\_AC}$", "$I_{DD\_CHKR\_CORE\_AC}$" and "$I_{DD\_HV\_IO\_BD}$" added. – Parameter "I_{DD_BD}" updated to "$I_{DD\_LV\_BD}$". Also modified Parameter description, added new condition "T_J = 150/165 C" and value. – Added note "Moving window, measured on application specific pattern" to "I_{SPIKE}". – Description of parameter "ISR" modified from "Current variation during power up/down" to "Current variation during boot/shut-down". – Added note "Current variation is considered during boot or during shut-down sequence. – Progressive clock switching should be use to guarantee low current variation. This does not include current requested for the loading of the capacitances on the VDD_LV domain. Please refer to Power management section, Iclamp specification" to the max value of I_{SR}. – Moved $I_{DD\_HV\_IO\_BD}$ before $I_{DD\_LV\_BD}$ – Updated the parameter, conditions column of I_{DDAR} and replaced the max value "10" with "30" – Added I_{DDOFF}, $V_{REF\_BG\_T}$, $V_{REF\_BG\_TC}$, and $V_{REF\_BG\_LR}$ – Updated Table footnote 4 and 8 *Section 3.17.2, Main voltage regulator electrical characteristics*: Updated the section *Table 18 (I/O input DC electrical characteristics)*: – V_{IHTTL} condition is 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V – V_{ILTTL} condition is 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V – V_{HYSTTL} condition is 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V – V_{IHCMOS_H} condition is 2.7 V < $V_{DD\_HV\_IO}$ < 3.0 V and 4.0 V < $V_{DD\_HV\_IO}$ < 4.5 V – V_{IHCMOS} condition is 2.7 V < $V_{DD\_HV\_IO}$ < 3.0 V and 4.0 V < $V_{DD\_HV\_IO}$ < 4.5 V – V_{ILCMOS_H} condition is 2.7 V < $V_{DD\_HV\_IO}$ < 3.0 V and 4.0 V < $V_{DD\_HV\_IO}$ < 4.5 V – V_{ILCMOS} condition is 2.7 V < $V_{DD\_HV\_IO}$ < 3.0 V and 4.0 V < $V_{DD\_HV\_IO}$ < 4.5 V – $V_{HYSCMOS}$ condition is 2.7 V < $V_{DD\_HV\_IO}$ < 3.0 V and 4.0 V < $V_{DD\_HV\_IO}$ < 4.5 V – Updated the conditions and values for parameter I_{LKG} – The conditions "3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V and 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V" split into 2 rows for the parameters V_{IHCMOS_H}, V_{IHCMOS}, V_{ILCMOS_H}, V_{ILCMOS} and $V_{HYSCMOS}$. – Added reference of Note 6 to V_{IHTTL}, V_{ILTTL}, and V_{HYSTTL}. – V_{DDE} replaced by $V_{DD\_HV\_IO}$. – $V_{DRFTAUT}$ specification, conditions column, added "4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V". – $V_{DRFTCMOS}$ specification, added 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V and 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V conditions. – I_{LKG_EBI} specification: changed "2.5 uA" Max value to "1 uA" and added condition "0.1*V_{DD_HV}<Vin<0.9*V_{DD_HV},Tj < 150 °C, 4.5V<V_{DD_HV}<5.5V'. Added second ILKG_EBI spec with conditions: "Tj < 150 °C, 4.5V < V_{DD_HV} < 5.5V' and Parameter "Digital input leakage for EBI pad, Vin = 10%/90%." Value is max 1.5 uA – Replaced "C" with "P" for I_{LKG}

Table 74. Revision history(Continued)

Revision	Date	Description of changes
3 (cont'd)	31 Jan 2014	– Removed the parameter I_{DCMAX_V} from the table. – Added new parameter "Propagation delay". – Updated the rows pertaining to R_{OH_V}, R_{OL_V}, f_{MAX_V}, t_{TR_V}, $t_{TR20-80}$, $\Sigma t_{TR20-80}$, and $\lvert t_{SKEW\_V}\rvert$ *Section 3.10, I/O pad current specification*: – In Note: *In order to ensure...remain below 10%.* changed to *...below 50%* – Changed the first note: from "In order to ensure correct functionality for SENT, the sum of all pad usage ratio within the SENT segment should remain below 50%." to "In order to maintain the required input thresholds for the SENT interface, the sum of all I/O pad output percent IR drop as defined in the I/O Signal Description table, must be below 100%. See the I/O Signal Description attachment." – In second note, changed must be below "100%" to must be below "50 %. *Table 24 (I/O consumption)*: – Removed footnote: *Data based on simulation results...* – Removed all VSIO conditions (VSIO[VSIO_xx] = 1 and VSIO[VSIO_xx] = 0) from conditions column and added footnote to I/O consumption table title: "I/O current consumption specifications for the 4.5 V <= $V_{DD\_HV\_IO}$ <= 5.5 V range are valid for VSIO_[VSIO_xx] = 1, and VSIO[VSIO_xx] = 0 for 3.0 V <= $V_{DD\_HV\_IO}$ <= 3.6 V. *Table 25 (Reset electrical characteristics)*: – Parameter classification of "V_{DD_POR} " changed from "C" to "D" – $\lvert I_{WPU}\rvert$ parameter, changed Min value from "25" to "23" and Max value from "100" to "82" uA. – $\lvert I_{WPD}\rvert$ parameter, changed Min value from "25" to "40" and Max value from "100" to "130" uA. – New "conditions" added for parameters "$\lvert I_{WPU}\rvert$" and "$\lvert I_{WPD}\rvert$". Removed "Device under power-on reset 3.0 V < VDD_HV_IO < 5.5 V, VOL > 0.9 V" under I_{OL_R} *Table 26 (PLL0 electrical characteristics)*: – Added rows $f_{PLL0PHI}$ and $f_{PLL0PHI0}$ – In footnote: *PLL0IN clock retrieved...* the second sentence now reads *Input characteristics are granted when using XOSC.* – Parameter "$t_{PLL0LOCK}$" max value changed from "100-110" to "110". *Table 27 (PLL1 electrical characteristics)*: – Changed $f_{PLL1PHI}$ Max Value to 160 *Table 28 (External Oscillator electrical specifications)*: – Removed "(External Reference)" from parameter column of V_{ILEXT} and added notes "This parameter is guaranteed by design rather than 100% tested" and "Applies to an external clock input and not to crystal mode" – Removed notes "C_{S_EXTAL}/C_{S_XTAL} have typical values of 7.5 pF in the QFP packages of the device" and "C_{S_EXTAL}/C_{S_XTAL} have typical values of 6.0 pF for bare die devices" – Updated the mIn and max values of QFP and Bare Die and removed notes from them under C_{S_EXTAL} and C_{S_XTAL} – Updated the min and max values of V_{HYS} and max values of IXTAL – Replaced "T_J = 150 °C" with "T_J = -40 °C to 150 °C" and replaced "T_J = 165 °C" with "T_J = -40 °C to 165 °C" for g_m – Added row V_{EXTAL}

Table 74. Revision history(Continued)

Revision	Date	Description of changes
3 (cont'd)	31 Jan 2014	– Differentiated rows $t_{16kprogrameep}$ with [KGD] and [Packaged part] – In row $t_{16kprogrameep}$ [Packaged part]: • Typ value changed to 31 • Initial max 25 °C changed to 40 • Initial max All temp changed to 58 • Typical end of life changed to 64 – In row $t_{16kprogrameep}$ [KGD]: • Typ value changed to 40.5 • Initial max 25 °C changed to 52.5 – In row t_{pr}: • Characteristics footnote changed to *Rate computed based on 256K sectors.* – In row $t_{fferase}$: – Characteristics footnote changed to *Only code sectors, not including EEPROM* – In row t_{PSRT}: • Characteristics footnote changed to *Time between suspend resume and...* – In row t_{PSUS}: • Initial max 25 °C value removed – In row t_{ESUS}: • characteristics footnote changed to *Timings guaranteed by design.* • Initial max 25 °C value removed – Added row t_{AICOP} – Footnote: *For memory sizes > 1 MB and...* changed to *Actual hardware programming times...* Added new Section 3.19.2, DSPI timing with CMOS and LVDS pads *Table 48 (JTAG pin AC electrical characteristics)*: Added footnote "JTAG timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 4.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the data sheet." *Table 49 (Nexus debug port timing)*: – t_{TCYC} (TCK cycle time) min value changed to 2 – Header "1K cycles" modified to "1k cycles". – Footnote 1 changed to "Nexus timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 4.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the data sheet." – Added (TDO sampled on posedge of TCK) to t_{TCYC} in the characteristics column and changed the min value from "36" to "40" Section 3.19.4, FlexRay timing: Added new section that includes "DSPI CMOS Slave timing - Modified Transfer Format (MTFE = 1)" table and timing diagrams "DSPI Slave Mode - Modified transfer format timing (MFTE = 1) — CPHA = 0" and "DSPI Slave Mode - Modified transfer format timing (MFTE = 1) — CPHA = 1". *Table 58 (DSPI CMOS Slave timing - Modified Transfer Format (MTFE = 0/1))*: – Changed table title "(MTFE = 1)" to "(MTFE = 0/1)" – Added footnote 1 to table title "DSPI slave operation is only supported for a single master and single slave on the device. Timing is valid for that case only." *Figure 40 (DSPI Slave Mode - Modified transfer format timing (MFTE = 0/1)—CPHA = 0)*: Changed figure title "(DSPI Slave Mode - Modified transfer format timing (MFTE = 1) — CPHA = 0) to "(DSPI Slave Mode - Modified transfer format timing (MFTE = 0/1) — CPHA = 0)".

Table 74. Revision history(Continued)

Revision	Date	Description of changes
4	19 Dec 2014	*Section 1.1, Document overview*: – Added note. *Table 2 (MPC5744K/SPC574Kx device feature summary)*: – Replaced “SIMD” with “LSP” in I/O processor. – Added cache row to I/O processor. – Added 140 MHz to Main processor frequency. – Added 70 MHz to I/O processor frequency. – Replaced “2 x 4 x 256-bit” with “2 x 2 x 256-bit” in Flash memory fetch accelerator. – Replaced M_CAN/M_TTCAN with CAN (M_CAN/M_TTCAN) || 3 (2/1)x. – Replaced 2/1 with 3 (2/1). – Added RMII to Ethernet. – Replaced “365 sources” with “360 sources” in Interrupt controller – Removed 1.2 V from External power supplies. – Moved notes from 144 LQFP-EP/eTQFP1445 and 176 LQFP-EP/eLQFP176 to 172-pin FusionQuad® and 216-pin FusionQuad® in Packages. *Figure 1 (Block diagram)*: – Changed “Calibration Bus” to “Calibration Interface”. *Figure 2 (Periphery allocation)*: – Replaced SRX_0 with SENT_SRX_0 and SRX_1 with SENT_SRX_1. *Section 1.5, Feature overview*: Replaced SIUL with SIUL2. – Removed “UART” from “UART Serial Boot Mode Protocol”. – Replaced “Boot Assist Module (BAM)” with “Boot Assist Flash (BAF)”. – Removed LIN from UART / LIN. – Removed FlexRay. *Figure 3 (144-pin QFP and 172-pin FQ configuration (top view))*: – Replaced VDD_LV_BD with NC/VDD_LV_BD and added a note on pin 10. – Removed FQ from the second note. *Figure 4 (176-pin QFP and 216-pin FQ configuration (top view))*: – Added note on pins 10 and 154. – Replaced VDD_LV_BD with NC/VDD_LV_BD and added a note on pin 10. *Section 2.2.1, Power supply and reference voltage pins*: – Added a note. *Table 4 (LVDSM pin descriptions)*: – Changed the signals of the port pins PA[8], PA[7], PA[9], and PA[5] in “Debug LFAST” functional block. *Section 3.2, Parameter classification*: – Removed note. Table 6 (Absolute maximum ratings): – In Notes, Changed T_J= 165 °C to 125 °C. – Changed the classification of T_{STG} from “C” to “T”. – Changed the classification of STORAGE from “C” to “—”. – Added note to $V_{DD\_HV\_ADV}$.

Table 74. Revision history(Continued)

Revision	Date	Description of changes
4 (cont'd)	19 Dec 2014	*Figure 9 (I/O output DC electrical characteristics definition)*: – Updated the figure. $t_{PD10-90}$ (rising edge) replaced by t_{PLH} (rising edge) and $t_{PD10-90}$ (falling edge) replaced by t_{PHL} (falling edge). Added 50% dotted line. *Table 20 (WEAK configuration output buffer electrical characteristics)*: – Replaced the minimum value of R_{OH_W} with "520" from "560". *Table 22 (STRONG configuration output buffer electrical characteristics)*: – Added $\|t_{SKEW\_S}\|$ parameter. *Table 23 (VERY STRONG configuration output buffer electrical characteristics)*: – Added I_{DCMAX_VS} specification. *Table 25 (Reset electrical characteristics)*: – For V_{HYS}, replaced minimum value "300" with "275". – For W_{FNMI}, replaced maximum value "20" with "15". *Table 26 (PLL0 electrical characteristics)*: – In f_{PLL0IN} added a second note to parameter column. *Table 27 (PLL1 electrical characteristics)*: – Removed $t_{PLL1JIT}$. – Updated all the minimum and maximum values of g_m. – Removed note 6 from below the table. *Table 28 (External Oscillator electrical specifications)*: – In g_m, changed the minimum and maximum frequencies. *Table 30 (Internal RC oscillator electrical specifications)*: – Moved the footnote from δf_{var_T} to δf_{var_SW}. – Updated the description of δf_{var_SW}. – Removed I_{AVDD5}. – Removed I_{DVDD12}. Table 26 (SARn ADC electrical specification): – Added ΔTUE_{10}. – For V_{ALTREF} replaced "P" with "C" and added another row for "P". – For I_{ADV_S}, reorganised the notes and added a note to "Power Down mode". – Changed the minimum and maximum value of DNL. – Removed INL. – Revised condition entries for $t_{ADCPRECH}$ and ΔV_{PRECH}. *Table 34 (SDn ADC electrical specification)*: – Updated SNR_{SE150}. – In V_{cmrr} specification: changed min value to 54 dB (was 20 dB). – Replaced "V_{cmrr}" with "CMRR". – δ_{GROUP} specification: changed OSR = 75 max value to 699 Tclk (was 646), changed OSR = 96 max value to 949.5 Tclk (was 946.4). – V_{OFFSET}: Changed parameter name to "Input Referred Offset Error" (was "Conversion Offset") and added footnote ("Conversion offset error must be...").