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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z2, e200z4, e200z4
Core Size	32-Bit Tri-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, FlexRay, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12b SAR, 16b Sigma-Delta
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-eLQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc574k72e7c6far

Figure 1. Block diagram

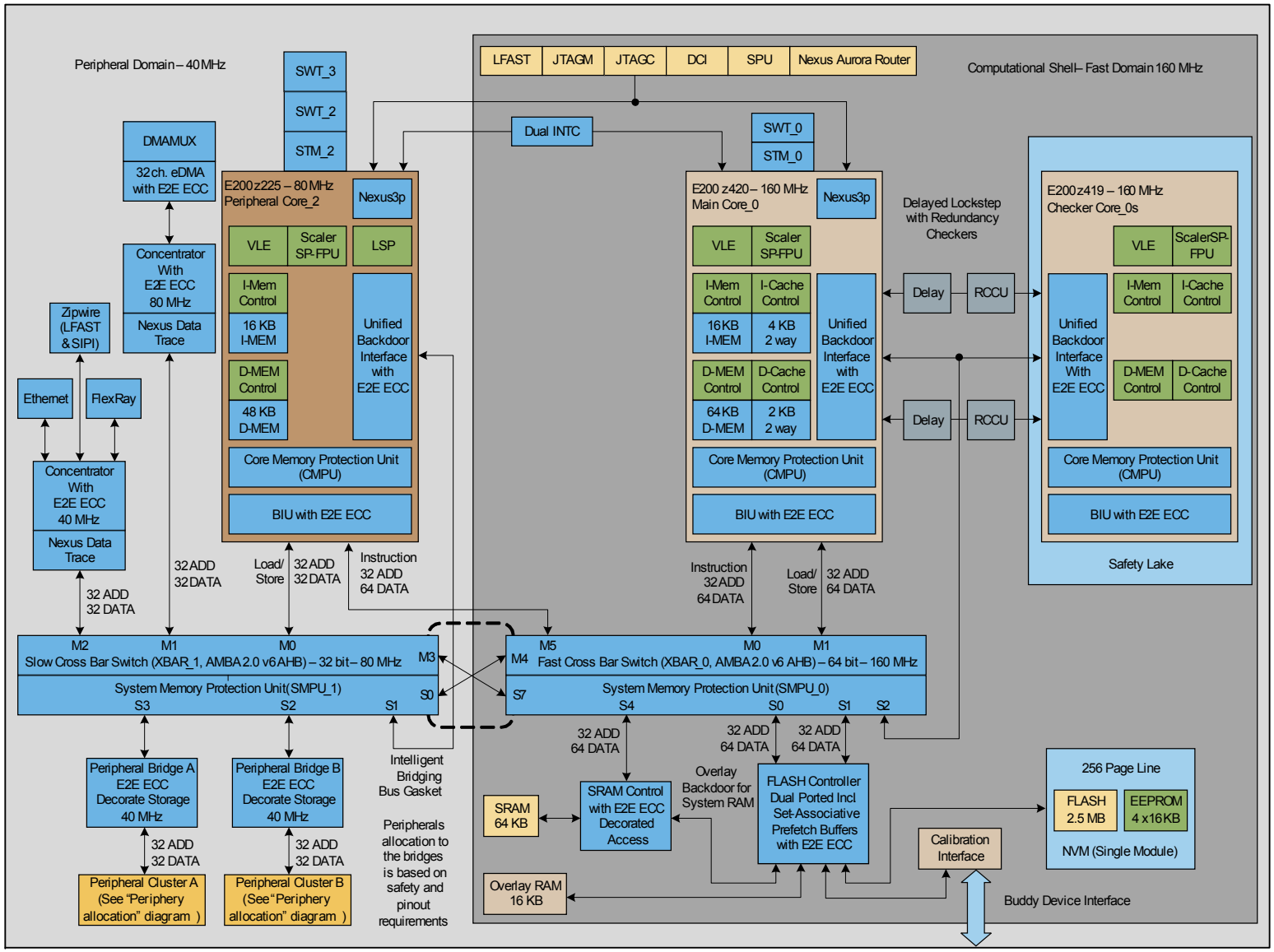
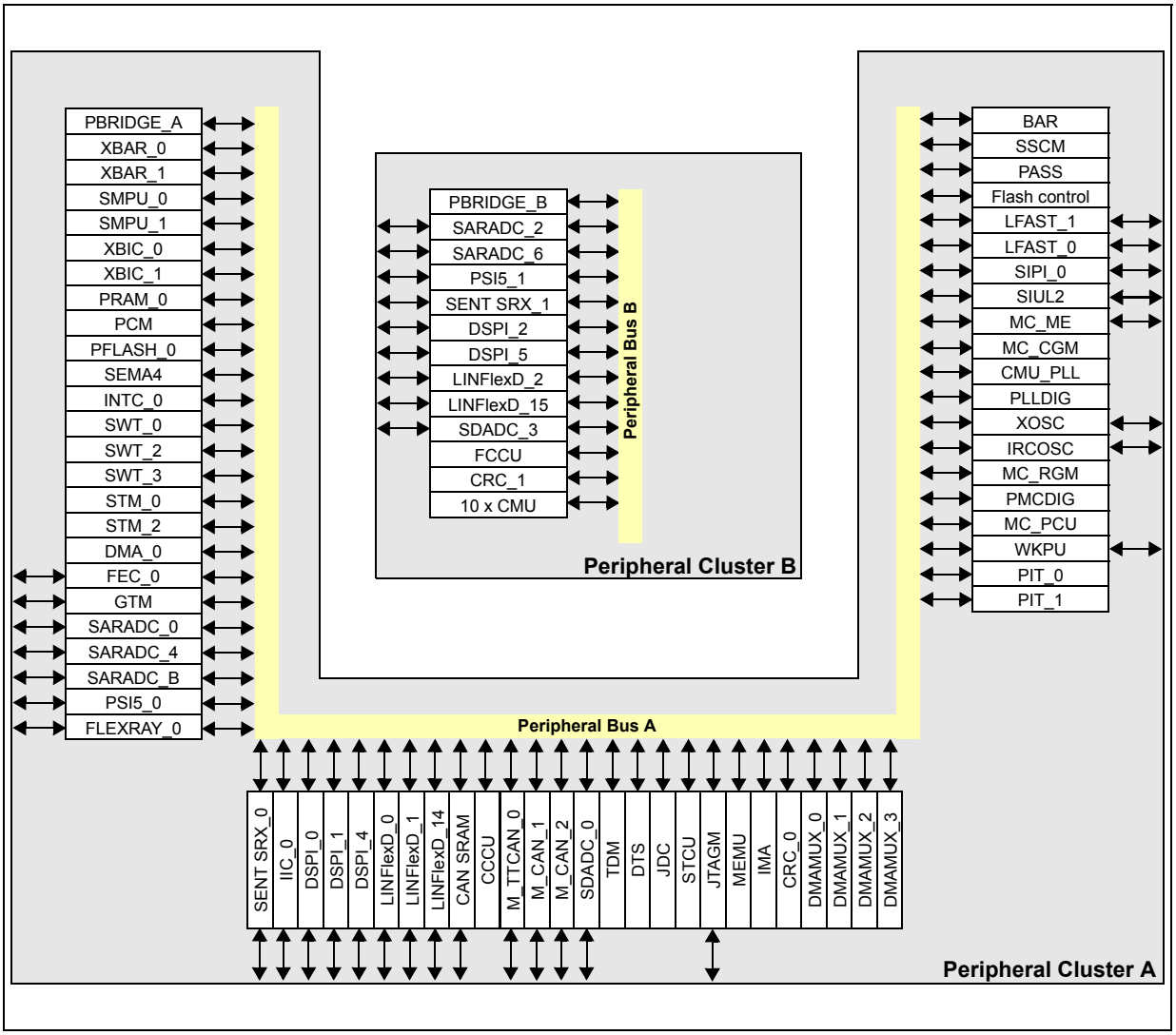


Figure 2. Periphery allocation

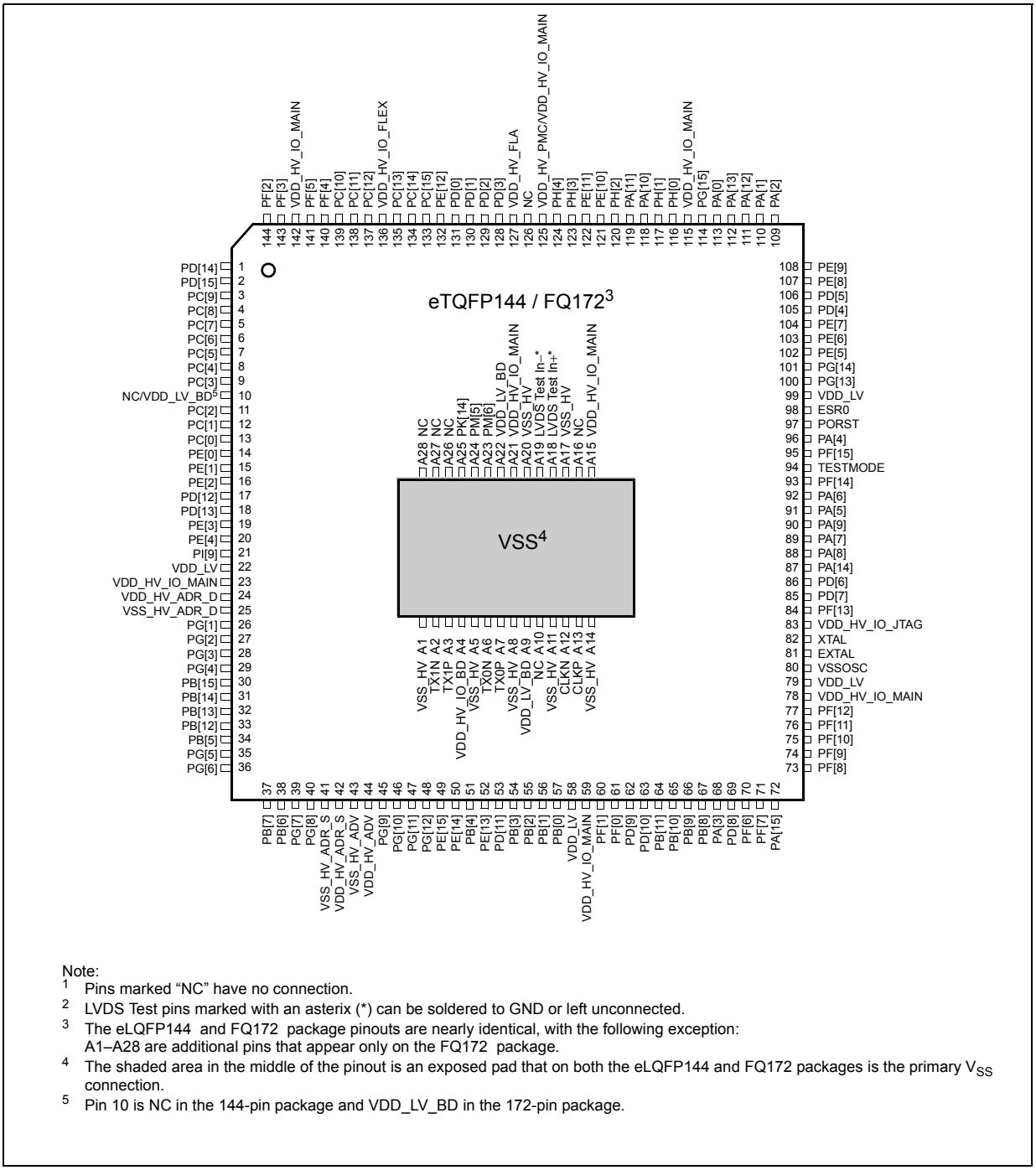


2 Package pinouts and signal descriptions

2.1 Package pinouts

The QFP and FusionQuad® package pinouts are shown in *Figure 3* and *Figure 4*.

Figure 3. 144-pin QFP and 172-pin FQ configuration (top view)



Note:
1 Pins marked “NC” have no connection.
2 LVDS Test pins marked with an asterix (*) can be soldered to GND or left unconnected.
3 The eLQFP144 and FQ172 package pinouts are nearly identical, with the following exception: A1–A28 are additional pins that appear only on the FQ172 package.
4 The shaded area in the middle of the pinout is an exposed pad that on both the eLQFP144 and FQ172 packages is the primary V_{SS} connection.
5 Pin 10 is NC in the 144-pin package and VDD_LV_BD in the 172-pin package.

Table 4. LVDSM pin descriptions(Continued)

Functional block	Port pin	Signal	Signal description	Direction	Package pin number	
					eTQFP144, FQ172	eLQFP176, FQ216
Differential DSPI 2	PD[3]	SCK_N	Differential DSPI 2 Clock, LVDS Negative Terminal	O	128	156
	PD[2]	SCK_P	Differential DSPI 2 Clock, LVDS Positive Terminal	O	129	157
	PD[1]	SOUT_N	Differential DSPI 2 Serial Output, LVDS Negative Terminal	O	130	158
	PD[0]	SOUT_P	Differential DSPI 2 Serial Output, LVDS Positive Terminal	O	131	159
	PF[13]	SIN_N	Differential DSPI 2 Serial Input, LVDS Negative Terminal	I	84	107
	PD[7]	SIN_P	Differential DSPI 2 Serial Input, LVDS Positive Terminal	I	85	108
Differential DSPI 5	PF[9]	SCK_N	Differential DSPI 5 Clock, LVDS Negative Terminal	O	74	95
	PF[10]	SCK_P	Differential DSPI 5 Clock, LVDS Positive Terminal	O	75	96
	PF[11]	SOUT_N	Differential DSPI 5 Serial Output, LVDS Negative Terminal	O	76	97
	PF[12]	SOUT_P	Differential DSPI 5 Serial Output, LVDS Positive Terminal	O	77	98
	PF[13]	SIN_N	Differential DSPI 5 Serial Input, LVDS Negative Terminal	I	84	107
	PD[7]	SIN_P	Differential DSPI 5 Serial Input, LVDS Positive Terminal	I	85	108

1. DRCLK and TCK/DRCLK usage for SIPI LFAST and Debug LFAST are described in the SPC574Kxx reference manual, refer to SIPI LFAST and Debug LFAST chapters.
2. Pads use special enable signal from DCI block: DCI driven enable for Debug LFAST pads is transparent to user.

3.12 Oscillator and FMPLL

3.12.1 FMPLL

Two frequency-modulated phase-locked loop (FMPLL) modules, the Reference PLL (PLL0) and the System PLL (PLL1) generate the system and auxiliary clocks from the main oscillator driver.

Figure 12. PLL integration

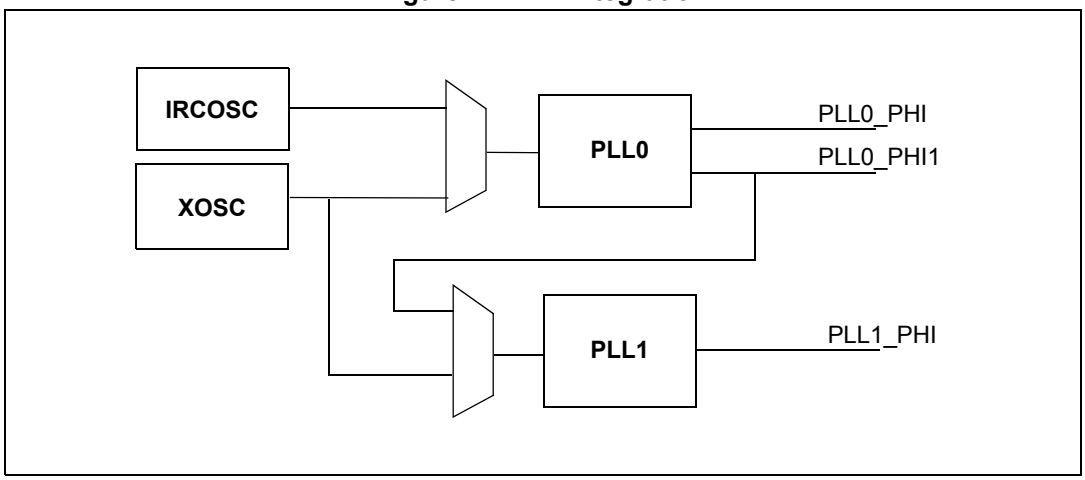


Table 26. PLL0 electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{PLL0IN}	SR	—	PLL0 input clock[1],[2]	—	8	—	44	MHz
Δ_{PLL0IN}	SR	—	PLL0 input clock duty cycle[1]	—	40	—	60	%
$f_{PLL0VCO}$	CC	P	PLL0 VCO frequency	—	600	—	1250	MHz
$f_{PLL0PHI}$	CC	D	PLL0 clock output frequency on PHI	—	—	—	400	MHz
$f_{PLL0PHI1}$	CC	D	PLL0 clock output frequency on PHI1	—	—	—	78	MHz
$t_{PLL0LOCK}$	CC	P	PLL0 lock time	—	—	—	110	µs
$\lvert\Delta_{PLL0PHI0SPJIT}\rvert$	CC	T	PLL0_PHI0 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI0}$ = 400 MHz, 6-sigma pk-pk	—	—	200	ps
$\lvert\Delta_{PLL0PHI1SPJIT}\rvert$	CC	T	PLL0_PHI1 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI1}$ = 40MHz, 6-sigma pk-pk	—	—	300[3]	ps

1. The typical user trim step size δf_{TRIM} = 0.35 %.

3.13 ADC specifications

3.13.1 ADC input description

Figure 15 shows the input equivalent circuit for fast SARn channels.

Figure 15. Input equivalent circuit (Fast SARn channels)

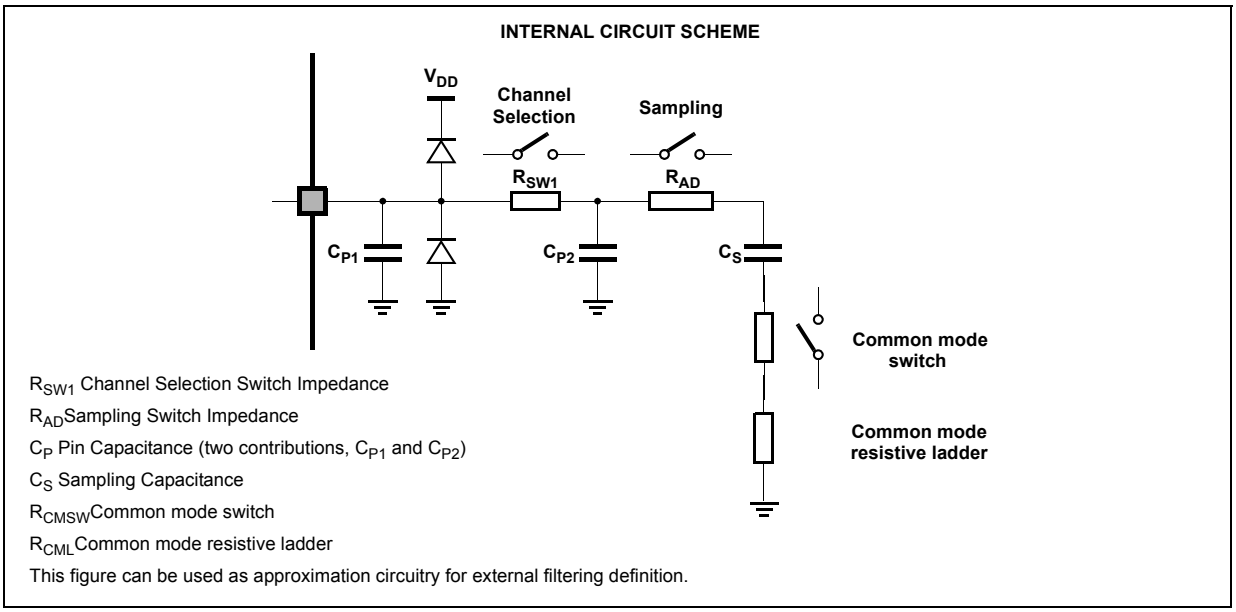


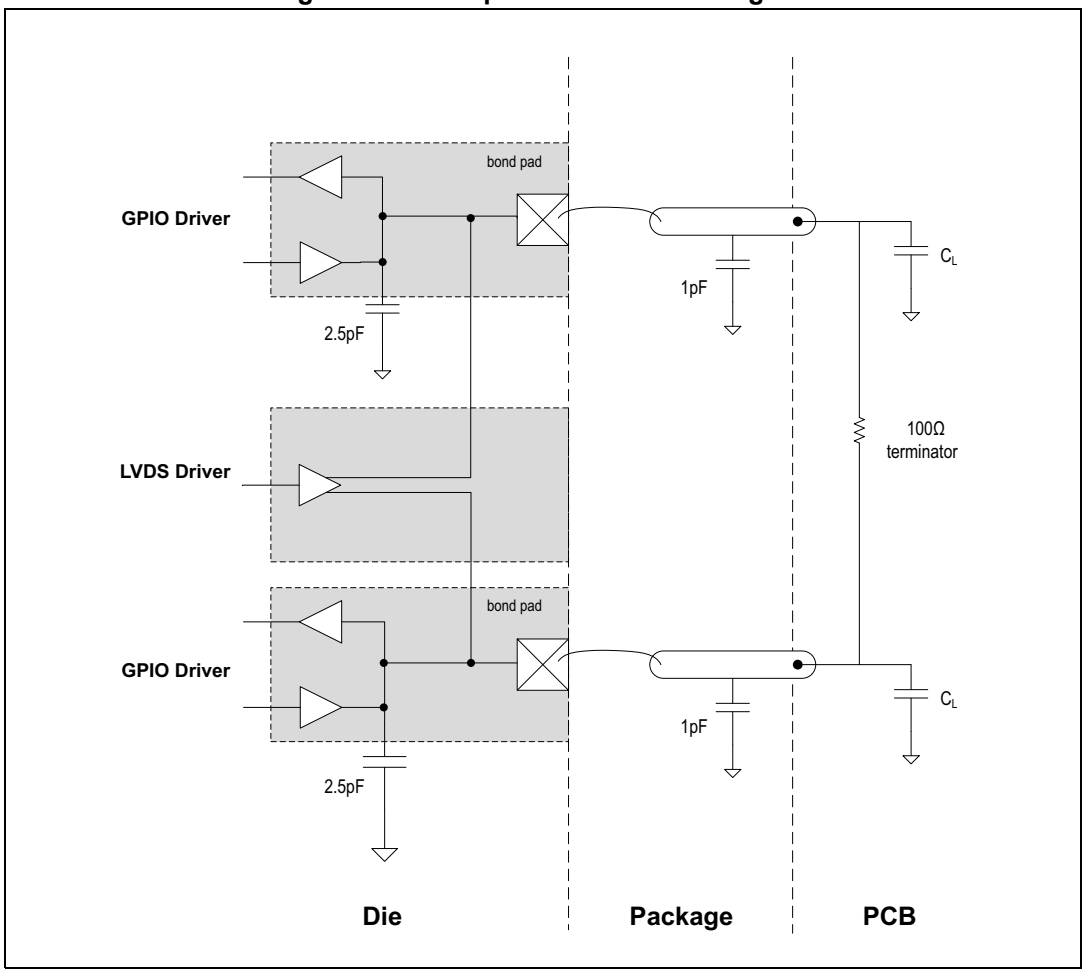
Figure 16 shows the input equivalent circuit for SARB channels.

Table 34. SDn ADC electrical specification[1](Continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
R_{BIAS}	CC	D	bias resistance	—	110	144	180	kΩ
ΔV_{INTCM}	CC	D	Common mode input reference voltage	—	–12		12	%
V_{BIAS}	CC	D	Bias voltage	—	—	$V_{DD\_HV\_ADR}/2$	—	V
δV_{BIAS}	CC	D	Bias voltage accuracy	—	–2.5	—	+2.5	%
CMRR	SR	D	Common mode rejection ratio	—	54	—	—	dB
R_{Caaf}	SR	D	Anti-aliasing filter	External series resistance	—	—	20	kΩ
	CC	D		Filter capacitances	180	—	—	pF
$f_{PASSBAND}$	CC	D	Pass band[16]	—	0.01	—	0.333 * f_{ADCD_S}	KHz
δ_{RIPPLE}	CC	D	Pass band ripple[17]	0.333 * f_{ADCD_S}	–1	—	1	%
$F_{rolloff}$	CC	D	Stop band attenuation	[0.5 * f_{ADCD_S}, 1.0 * f_{ADCD_S}]	40	—	—	dB
				[1.0 * f_{ADCD_S}, 1.5 * f_{ADCD_S}]	45	—	—	
				[1.5 * f_{ADCD_S}, 2.0 * f_{ADCD_S}]	50	—	—	
				[2.0 * f_{ADCD_S}, 2.5 * f_{ADCD_S}]	55	—	—	
				[2.5 * f_{ADCD_S}, f_{ADCD_M}/2]	60	—	—	

3. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in *Figure 21*.
4. Valid for maximum external load C_L.

Figure 21. LVDS pad external load diagram



3.15.3 LFAST PLL electrical characteristics

The following table contains the electrical characteristics for the LFAST PLL.

Table 39. LFAST PLL electrical characteristics(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Nominal	Max	
f_{RF_REF}	SR	D	PLL reference clock frequency	—	10	—	26	MHz
ERR_{REF}	CC	D	PLL input reference clock frequency error	—	–1	—	1	%
DC_{REF}	CC	D	PLL input reference clock duty cycle	—	45	—	55	%

3. Startup time is defined as the time taken by LVDS receiver for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.

3.19.1.4 Aurora debug port timing

Table 51. Aurora debug port timing

#	Symbol		C	Characteristic		Value		Unit
						Min	Max	
1	t_{REFCLK}	CC	T	Reference clock frequency		625	1250	MHz
1a	t_{MCYC}	CC	T	Reference clock rise/fall time		—	400	ps
2	t_{RCDC}	CC	D	Reference clock duty cycle		45	55	%
3	J_{RC}	CC	D	Reference clock jitter		—	40	ps
4	$t_{STABILITY}$	CC	D	Reference clock stability		50	—	PPM
5	BER	CC	D	Bit error rate		—	10^{-12}	—
6	J_D	SR	D	Transmit lane deterministic jitter		—	0.17	OUI
7	J_T	SR	D	Transmit lane total jitter		—	0.35	OUI
8	S_O	CC	T	Differential output skew		—	20	ps
9	S_{MO}	CC	T	Lane to lane output skew		—	1000	ps
10	OUI	CC	D	Aurora lane unit interval(1)	625 Mbps	1600	1600	ps
			D		1.25 Gbps	800	800	

1. ± 100 PPM

Table 52. DSPI channel frequency support(Continued)

DSPI use mode		Max usable frequency (MHz)[1],[2]
LVDS (Master mode)	Full duplex – Modified timing (*Table 55*)	33
	Output only mode TSB mode (SCK/SOUT/PCS) (*Table 56*)	40
CMOS Slave mode	Full duplex (*Table 58*)	16

1. Maximum usable frequency can be achieved if used with fastest configuration of the highest drive pads.
2. Maximum usable frequency does not take into account external device propagation delay.

3.19.2.1 DSPI master mode full duplex timing with CMOS and LVDS pads

3.19.2.1.1 DSPI CMOS Master Mode – Classic Timing

Table 53. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1]

#	Symbol		C	Characteristic	Condition		Value[2]		Unit
					Pad drive[3]	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	33.0	—	ns
					Strong	50 pF	80.0	—	
					Medium	50 pF	200.0	—	
2	t_{CSC}	CC	D	PCS to SCK delay	SCK and PCS drive strength				
					Very strong	25 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 16$	—	ns
					Strong	50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 16$	—	
					Medium	50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 16$	—	
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	$(N^{(4)} \times t_{SYS}^{(5)}) - 29$	—	
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	
					Medium	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	$(M^{(6)} \times t_{SYS}^{(5)}) - 35$	—	

4. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
5. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
6. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
7. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
8. PCSx and PCSS using same pad configuration.
9. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.
10. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Figure 31. DSPI CMOS master mode – classic timing, CPHA = 0

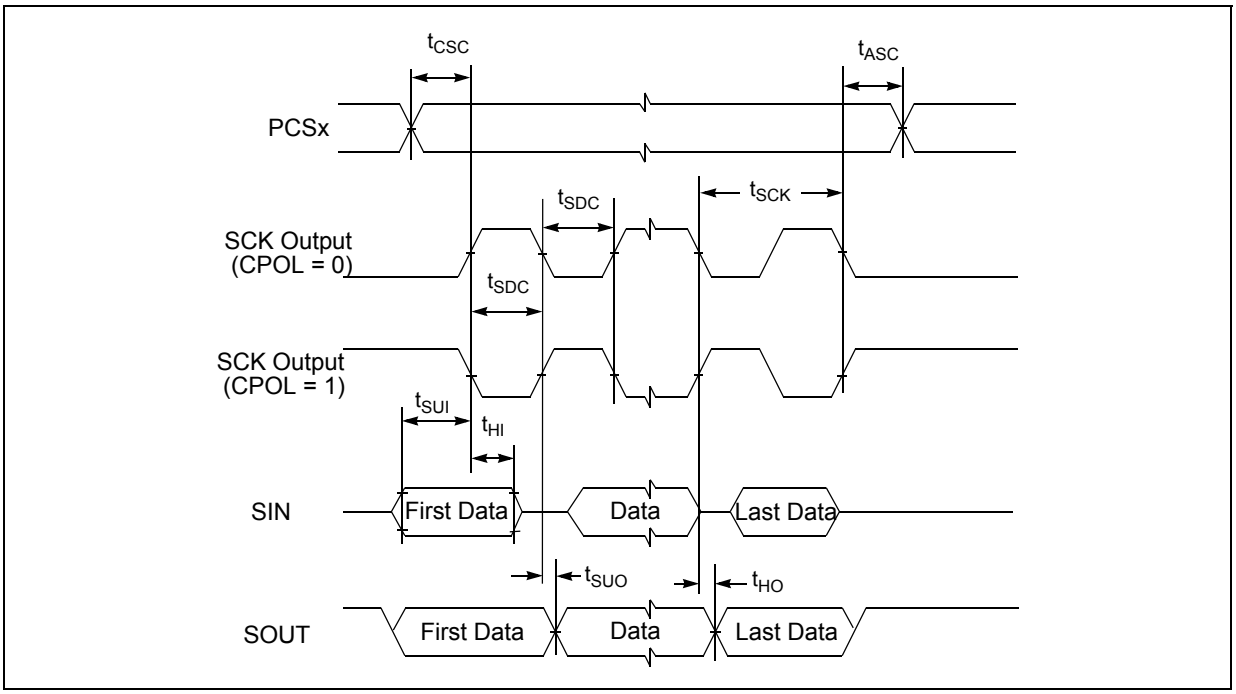
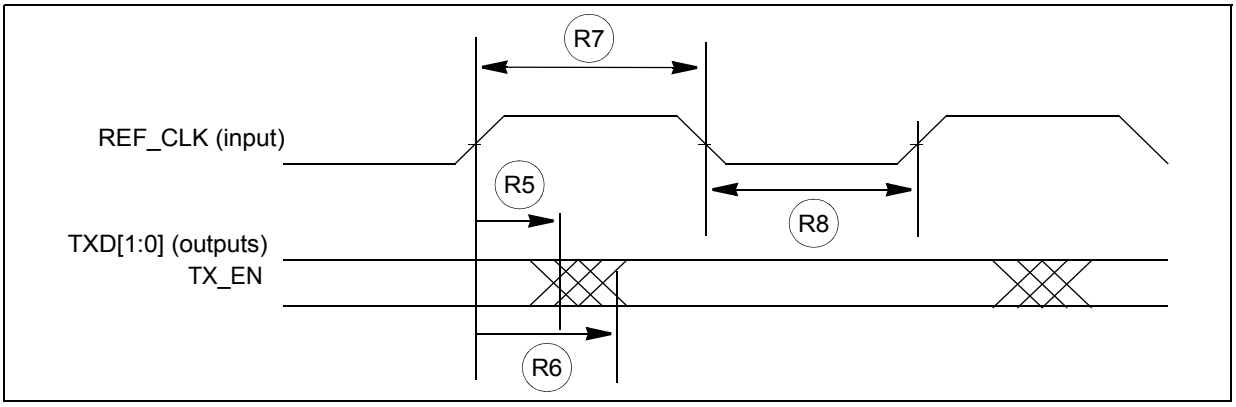


Figure 44. RMII transmit signal timing diagram



3.19.4 FlexRay timing

This section provides the FlexRay Interface timing characteristics for the input and output signals.

These are recommended numbers as per the FlexRay EPL v3.0 specification, and subject to change per the final timing analysis of the device.

3.19.4.1 TxEN

Figure 45. TxEN signal

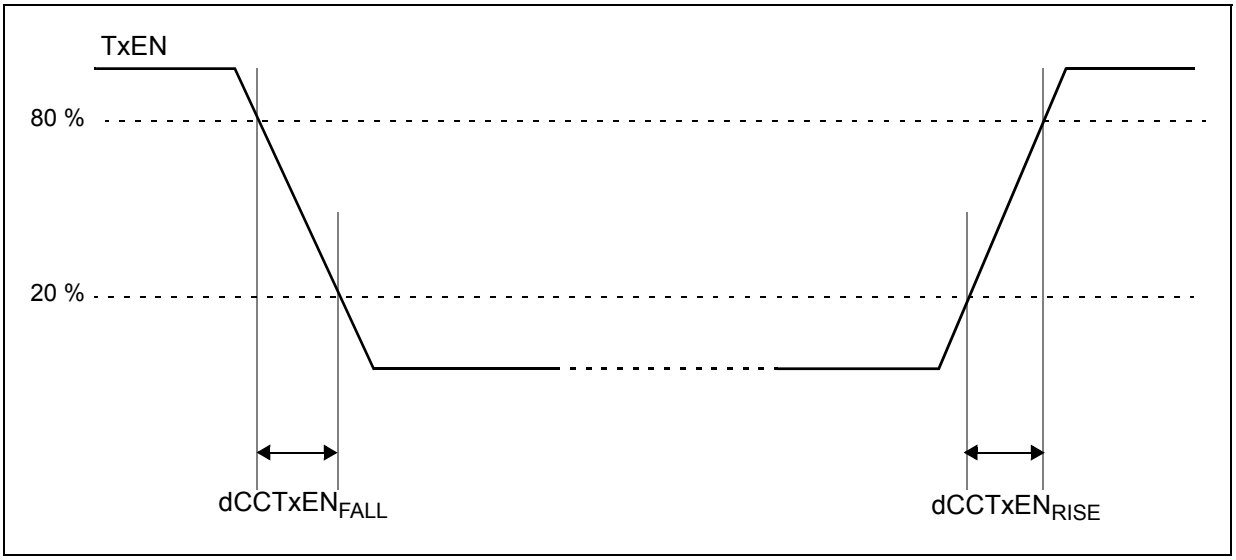


Table 62. TxEN output characteristics(1)

Symbol		C	Characteristic	Value		Unit
				Min	Max	
dCCTxEN$_{RISE25}$	CC	D	Rise time of TxEN signal at CC	—	9	ns
dCCTxEN$_{FALL25}$	CC	D	Fall time of TxEN signal at CC	—	9	ns

Table 65. PSI5 timing

Symbol		C	Parameter	Value		Unit
				Min	Max	
t_{MSG_DLY}	CC	D	Delay from last bit of frame (CRC0) to assertion of new message received interrupt	—	3	µs
t_{SYNC_DLY}	CC	D	Delay from internal sync pulse to sync pulse trigger at the SDOUT_PSI5_n pin	—	2	µs
t_{MSG_JIT}	CC	D	Delay jitter from last bit of frame (CRC0) to assertion of new message received interrupt	—	1	cycles(1)
t_{SYNC_JIT}	CC	D	Delay jitter from internal sync pulse to sync pulse trigger at the SDOUT_PSI5_n pin	—	±(1 PSI5_1µs_CLK + 1 PBRIDGEn_CLK)	cycles

1. Measured in PSI5 clock cycles (PBRIDGEn_CLK on the device). Minimum PSI5 clock period is 20 ns.

3.19.6 UART timing

UART channel frequency support is shown in the following table.

Table 66. UART frequency support

LINFlexD clock frequency LIN_CLK (MHz)	Oversampling rate	Voting scheme	Max usable frequency (Mbaud)
80	16	3:1 majority voting	5
	8		10
	6	Limited voting on one sample with configurable sampling point	13.33
	5		16
	4		20
100	16	3:1 majority voting	6.25
	8		12.5
	6	Limited voting on one sample with configurable sampling point	16.67
	5		20
	4		25

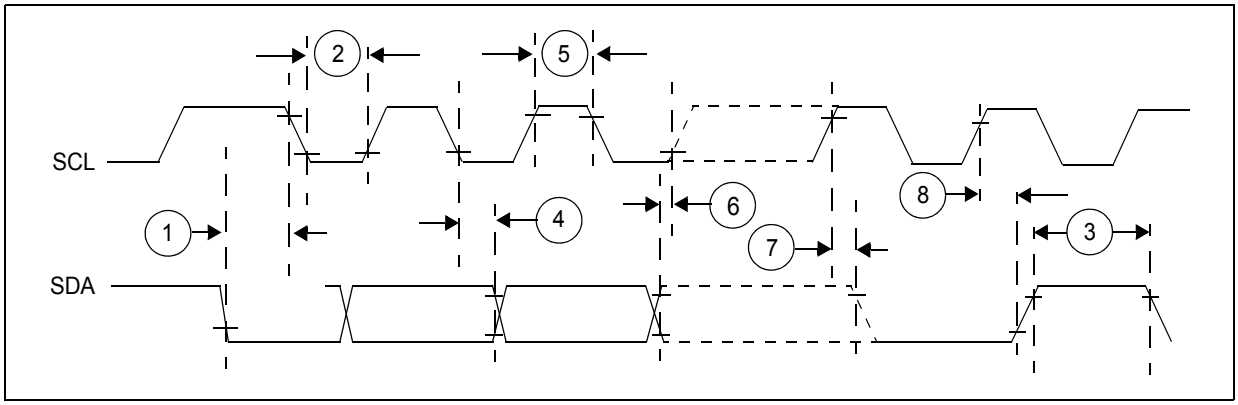
3.19.7 I²C timing

The I²C AC timing specifications are provided in the following tables.

Table 67. I²C input timing specifications — SCL and SDA(1)

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	—	CC	D	Start condition hold time	2	—	PER_CLK Cycle(2)
2	—	CC	D	Clock low time	8	—	PER_CLK Cycle

Figure 49. I²C input/output timing



3.19.8 GPIO delay timing

The GPIO delay timing specification is provided in the following table.

Table 69. GPIO delay timing

Symbol		C	Parameter	Value		Unit
				Min	Max	
IO_delay	CC	D	Delay from MSCR bit update to pad function enable	5	25	ns

4.2 eTQFP144 case drawing

Figure 50. eTQFP144 – STMicroelectronics package mechanical drawing (1 of 2)

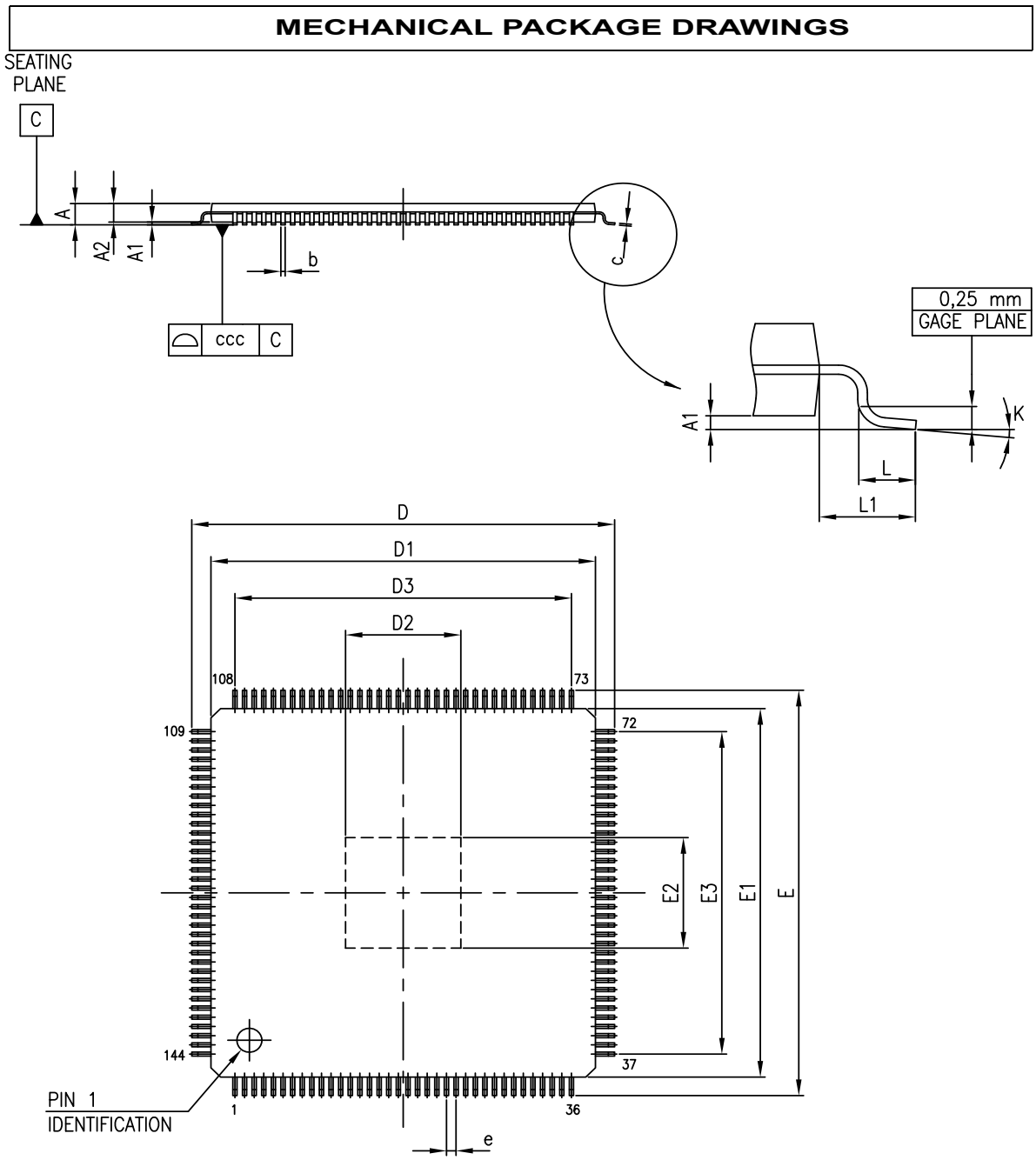


Figure 55. FusionQuad® QFP172 package mechanical drawing (2 of 2)

MECHANICAL OUTLINE ASSEMBLY

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE H LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUMS A–B AND D TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC BODY AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
6. 'N' IS THE NUMBER OF TERMINALS FOR PERIPHERAL LEADS, AND 'M' IS THE NUMBER OF TERMINALS FOR BOTTOM LANDS ON BOTTOM SURFACE OF PACKAGE BODY. THE BOTTOM LANDS ARE IDENTIFIED BY ALPHANUMERICS | A1~A#.
7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE H.
8. THE TOP OF PACKAGE MAY BE SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MM.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
10. CONTROLLING DIMENSION | MILLIMETERS.
11. MAXIMUM ALLOWABLE DIE THICKNESS TO BE ASSEMBLED IN THIS PACKAGE FAMILY IS 0.38 MM.
12. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
13. DIMENSIONS D2 AND E2 REPRESENT THE SIZE OF THE EXPOSED PAD. THE ACTUAL DIMENSIONS ARE DETERMINED BY EACH INDIVIDUAL LEADFRAME DRAWING. THE EXPOSED PAD SIZE TOLERANCE IS 0.10 MAX.
14. EXPOSED PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 0.05 MM.
15. UNILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
16. MECHANICAL CONNECT TABS ARE COUNTED FOR GROUND (VSS) SIGNAL PINS. THOSE ARE INCLUDED INTO PACKAGE TOTAL PIN COUNTS.
17. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.
18. THESE DIMENSIONS APPLY TO ALL 4 SYMMETRIC LOCATIONS.
19. GATE PROTRUSION HEIGHT OR CHIP OUT DEPTH | 0.049 MM MAX

ALL DIMENSIONS IN MILLIMETERS

VARIATIONS				
SYMBOL	FUSION			NOTE
	MIN	NOM	MAX	
A	—	—	1.20	
A1	0.05	0.10	0.15	
A2	0.95	1.00	1.05	
A3	–0.05	0.00	0.05	
A4		0.152 REF		
D		22.00 BSC		4
D1		20.00 BSC		5
D2		17.50 BSC		
D3	8.32	8.42	8.52	
E		22.00 BSC		4
E1		20.00 BSC		5
E2		17.50 BSC		
E3	8.20	8.30	9.40	
E4		10.00 REF		
L	0.45	0.60	0.75	
N		144		6
e		0.50 BSC		
b	0.17	0.22	0.27	
c.c.c		0.08		
d.d.d		0.08		

PITCH VARIATIONS				
SYMBOL	FUSION			NOTE
	MIN	NOM	MAX	
eT		0.50 BSC		
eC		0.39 BSC		18
M		28		6
La	0.30	0.40	0.50	
f	0.17	0.22	0.27	
999	—	0.08	—	

THE FusionQuad PACKAGE IS A REGISTERED TRADEMARK OF AMKOR TECHNOLOGIES.

THE FusionQuad PACKAGE IS ASSEMBLED BY AMKOR TECHNOLOGIES.

Table 72. Thermal characteristics for eLQFP176[1]

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection[2]	Four layer board—2s2p	25	28	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-moving-air, ambient[2]	At 200 ft./min., four layer board—2s2p	18	22	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board[3]	—	12	16	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-case top[4]	—	12	15	°C/W
$R_{\theta JCbottom}$	CC	D	Junction-to-case bottom[5]	—	1.5	3.5	°C/W
Ψ_{JT}	CC	D	Junction-to-package top[6]	Natural convection	3	4.5	°C/W
P_d	CC	D	Device power dissipation	Maximum power and voltage condition	—	2	W

1. The lower number in the ranges specified in the 'Value' column are based on simulation; actual data may vary in the given range. The specified characteristics are subject to change per final device design and characterization. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.5.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

Equation 3 $T_J = T_A + (R_{\theta JA} * P_D)$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Table 74. Revision history(Continued)

Revision	Date	Description of changes
3 (cont'd)	31 Jan 2014	*Table 42 (Voltage monitor electrical characteristics)*: – V_{LVD108} specification, changed Min value from "1080" to "1120" – V_{LVD108} specification, changed Max value from "1140" to "1170" – V_{LVD108}Changed Parameter name "LV internal supply low voltage monitoring" to "Core LV internal supply low voltage monitoring" and added note to conditions "This is combination of LVD108_C, P, and F. Min is from min value of LVD108_F, and P which is the lowest one. Max is the max value of LVD108_C which is the highest one of three." – V_{PORUP_LV} Falling voltage (power down) condition, added footnote "assume all of LVDs on LV supplies disabled". – Added "HVD140 does not cause reset" at end of footnote "HVD is released after $t_{VDRELEASE}$ temporization when lower threshold is crossed, HVD is asserted tVDASSERT after detection when upper threshold is crossed." – V_{LVD295} Rising voltage condition changed Max value "3100" to "3120". – V_{LVD295} Falling voltage condition changed Min value "2950" to "2920" and Max value "3080" to "3100". – V_{HVD360} Rising voltage condition changed Min value "3420" to "3435" and Max value "3610" to "3650". – V_{HVD360} Falling voltage condition changed Min value "3400" to "3415". *Table 44 (Functional terminals state during power-up and reset)*: – Replaced "Weak pull-down" with "Weak pull-up" for ESR1 in Power-up, reset, and default states – Replaced "ERROR" with "ERROR[0]" – Updated note 6 – ESR1 POWER-UP Pad State changed to *Weak pull-down.* *Table 45 (Flash memory program and erase specifications)*: Updated the values. *Table 46 (Flash memory Life Specification)*: Replaced "K" with "k" in the unit column *Section 3.18.1, Flash read wait state and address pipeline control settings*: Added this section Moved I^2C AC timing specification after section "UART timing" Moved "UART timing" section after "PSI5 timing" Table 48 (K2 Flash memory program and erase specifications(pending silicon characterization)) – Complete rework of table and contents. – In row $t_{dwprogram}$: • removed Initial max parameter classification • Lifetime max changed to 650 – In row $t_{pprogra}$: • Initial max parameter classification removed – Added row $t_{pprogrameep}$ [KGD] – In row $t_{qprogram}$: • Typical end of life changed to 396 – Added row $t_{qprogrameep}$ [KGD]

Table 74. Revision history(Continued)

Revision	Date	Description of changes
5 (cont'd)	30 March 2015	*Table 39 (LFAST PLL electrical characteristics)*: Replaced "P" with "T" in the classification column of f_{VCO} parameter and updated note 2. *Table 38 (MSC/DSPI LVDS transmitter electrical characteristics)*: Replaced "C" with "T" in the classification column of I_{LVDS_TX} parameter. *Table 40 (Aurora LVDS electrical characteristics)*: For $\|\Delta V_{OD\_LVDS}\|$ parameter, removed the "$\pm$" from the values. *Table 41 (Device Power Supply Integration)*: Replaced maximum value of "300" with "350" for IDD_{MREG} parameter. *Table 59 (RMII serial management channel timing)*: For M10 parameter, replaced the minimum value of "0" with "-10". For M13 parameter, replaced the minimum value of "-10" with "10". Updated the third footnote. *Table 64 (RxD input characteristics)*: Removed "Automotive and" from table footnote. *Table 71 (Thermal characteristics for eTQFP144)*: Added P_d parameter. *Table 72 (Thermal characteristics for eLQFP176)*: Added P_d parameter.