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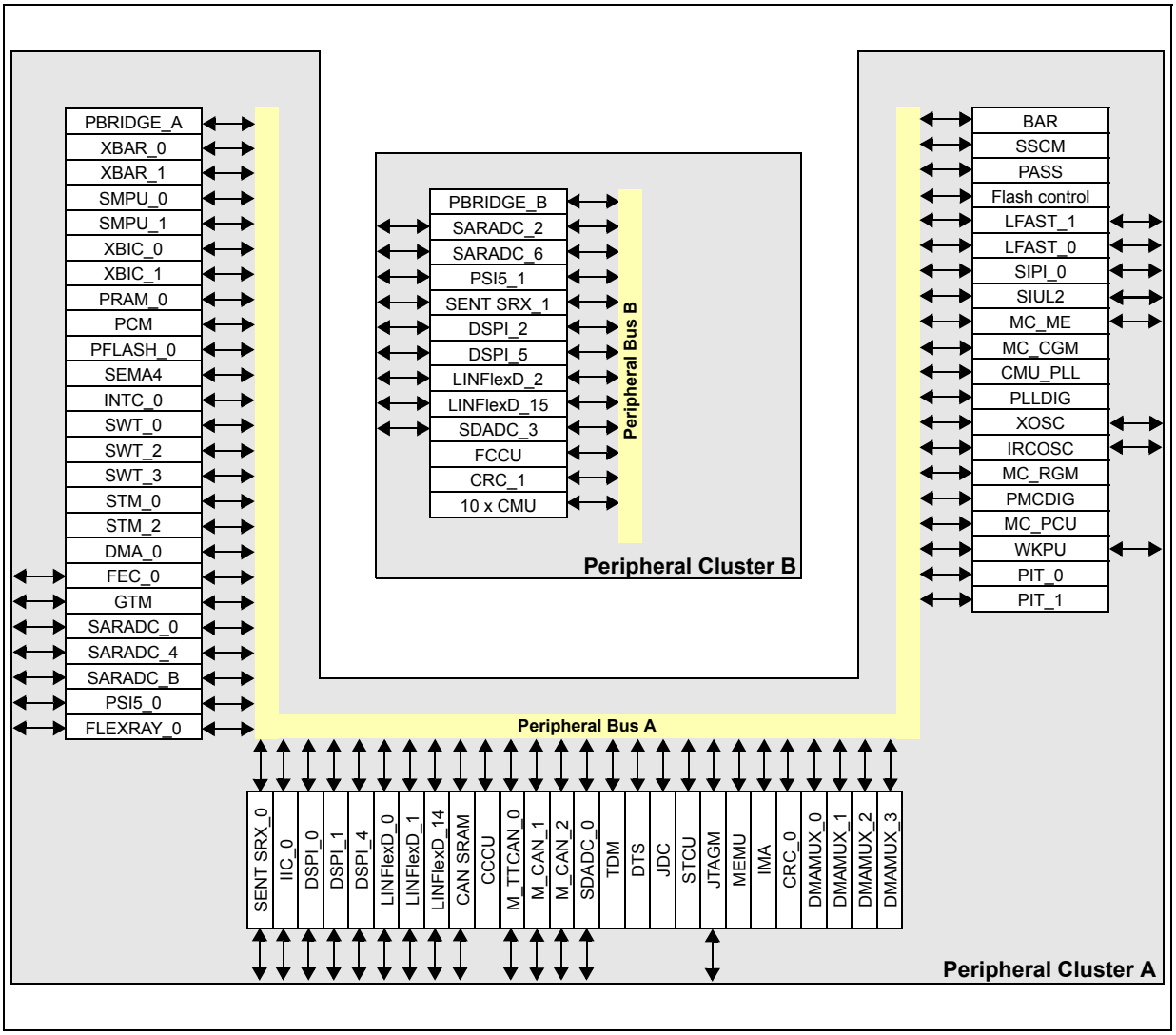
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z2, e200z4, e200z4
Core Size	32-Bit Tri-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, FlexRay, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12b SAR, 16b Sigma-Delta
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-eLQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc574k72e7c6fay

Figure 2. Periphery allocation



3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” (Controller Characteristics) is included in the “Symbol” column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” (System Requirement) is included in the “Symbol” column.

Note: Parameters given to junction temperature T_J = 150 °C are for packaged parts .

Note: Within this document, $V_{DD\_HV\_IO}$ refers to supply pins $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_JTAG}$, $V_{DD\_HV\_IO\_FLEX}$, $V_{DD\_HV\_OSC}$ and $V_{DD\_HV\_FLA}$.

3.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 6* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 6. Parameter classifications

Classification tag	Tag description
P	Parameters are guaranteed by production testing on each individual device.
C	Parameters are guaranteed by the design characterization by measuring a statistically relevant sample size across process variations.
T	Parameters are guaranteed by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Parameters are derived mainly from simulations.

3.3 Absolute maximum ratings

Table 7 describes the maximum ratings of the device.

Table 7. Absolute maximum ratings(1)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
Cycle	T	Lifetime power cycles	—	—	1000 k	—
V_{SS_HV}	D	Ground voltage	—	—	—	—
V_{DD_LV}	D	1.2 V core supply voltage(2),(3),(4)	—	–0.3	1.5	V

Table 14. Temperature profile – Packaged parts(Continued)

Vehicle category	Operation	Temperature	Cumulated duration (hours)
Passenger cars – low end	Active operation	T_A = 120 to 125 °C	100
		T_A = 115 to 120 °C	100
		T_A = 110 to 115 °C	100
		T_A = 105 to 110 °C	100
		T_A = 100 to 105 °C	100
		T_A = 95 to 100 °C	100
		T_A = 90 to 95 °C	100
		T_A = 85 to 90 °C	150
		T_A = 80 to 85 °C	300
		T_A = 50 to 80 °C	800
		T_A = 40 to 50 °C	1600
		T_A = 25 to 40 °C	2200
		T_A = –10 to 25 °C	1500
		T_A = –40 to –10 °C	500
		Total operation time	7750
Commercial vehicles	Active operation	T_J = 150 °C	360
		T_J = 140 °C	1200
		T_J = 130 °C	2100
		T_J = 120 °C	29000
		T_J = 110 °C	3600
		T_J = 85 °C	2740
		T_J = 40 °C	500
		T_J = –40 °C	500
		Total operation time	40000

Table 15. Unbiased temperature profile – Packaged parts

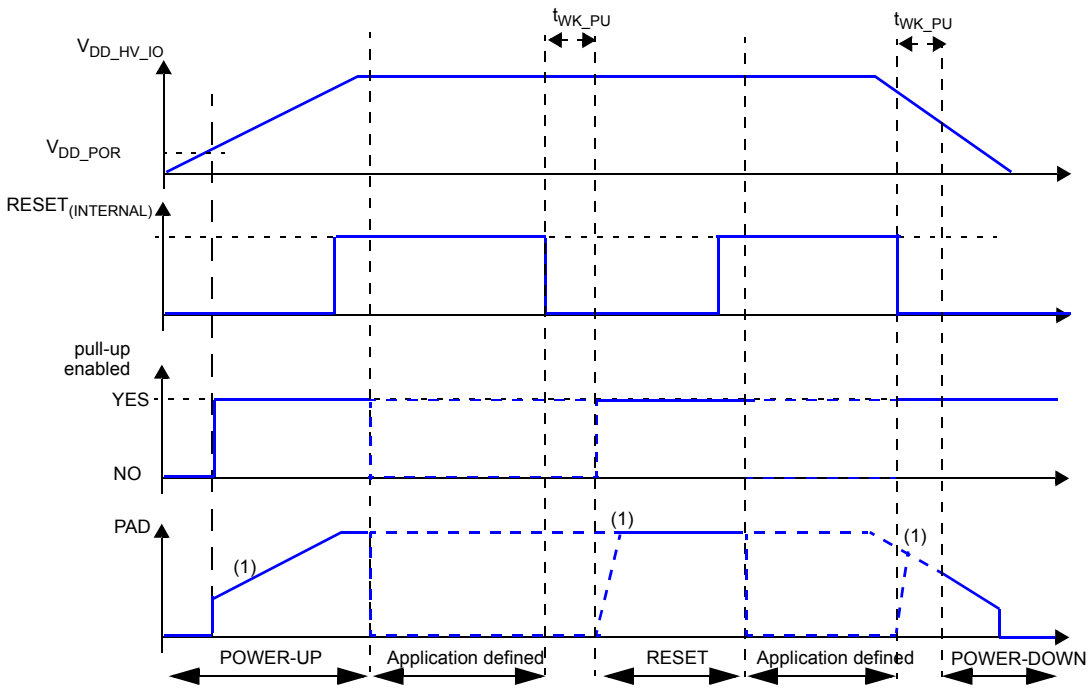
Operation	Temperature	Cumulated duration (years)
Unbiased	T_J > 60 °C	0(1)
	T_J = –40 to 60 °C	20

1. Temperatures above 60 °C are accumulated against active operation biased condition.

3.8 DC electrical specifications

The following table describes the DC electrical specifications.

Figure 8. Weak pull-up electrical characteristics definition



1. Actual PAD slopes will depend on external capacitances and VDD_HV_IO supply.

3.9.2 I/O output DC characteristics

The figure below provides description of output DC electrical characteristics.

Table 20. WEAK configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
R_{OH_W}	CC	P	PMOS output impedance weak configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OH} < 0.5 mA	—	—	1040	Ω
R_{OL_W}	CC	P	NMOS output impedance weak configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OL} < 0.5 mA	—	—	1040	Ω
f_{MAX_W}	CC	T	Output frequency weak configuration	C_L = 25 pF[3]	—	—	2	MHz
				C_L = 50 pF[3]	—	—	1	
		D		C_L = 200 pF[3]	—	—	0.25	
t_{TR_W}	CC	T	Transition time output pin weak configuration[4]	C_L = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	40	—	120	ns
				C_L = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	80	—	240	
		D		C_L = 200 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	320	—	820	
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	50	—	150	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	100	—	300	
				C_L = 200 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	350	—	1050	
$\lvert t_{SKEW\_W} \rvert$	CC	T	Difference between rise and fall time	—	—	—	25	%
I_{DCMAX_W}	CC	D	Maximum DC current	—	—	—	4	mA
$T_{PHL/PLH}$	CC	D	Propagation delay	C_L = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	120	ns
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	150	
				C_L = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	240	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	—	—	300	

1. All VDD_HV_IO conditions for 4.5V to 5.5V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0V to 3.6V are valid for VSIO[VSIO_xx] = 0
2. All values need to be confirmed during device validation.
3. C_L is the sum of external capacitance. Device and package capacitances (C_{IN}, defined in *Table 18*) are to be added to calculate total signal capacitance (C_{TOT} = C_L + C_{IN}).
4. Transition time maximum value is approximated by the following formula:

   0 pF < C_L < 50 pFt_{TR_W}(ns) = 22 ns + C_L(pF) × 4.4 ns/pF

   50 pF < C_L < 200 pFt_{TR_W}(ns) = 50 ns + C_L(pF) × 3.85 ns/pF
5. Only for $V_{DD\_HV\_IO\_JTAG}$ segment when VSIO[VSIO_IJ] = 0 or $V_{DD\_HV\_IO\_FLEX}$ segment when VSIO[VSIO_IF] = 0.

Table 21 shows the MEDIUM configuration output buffer electrical characteristics.

Table 25. Reset electrical characteristics

Symbol			Parameter	Conditions	Value(1)			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input high level TTL (Schmitt trigger)	—	2.0	—	$V_{DD\_HV\_IO}$ +0.4	V
V_{IL}	SR	P	Input low level TTL (Schmitt trigger)	—	–0.4	—	0.8	V
V_{HYS}	CC	C	Input hysteresis TTL (Schmitt trigger)	—	275	—	—	mV
V_{DD_POR}	CC	D	Minimum supply for strong pull-down activation	—	—	—	1.2	V
I_{OL_R}	CC	P	Strong pull-down current(2)	Device under power-on reset $V_{DD\_HV\_IO} = V_{DD\_POR}$, $V_{OL} = 0.35 * V_{DD\_HV\_IO}$	0.2	—	—	mA
				Device under power-on reset 3.0 V < $V_{DD\_HV\_IO}$ < 5.5 V, V_{OL} > 1.0 V	8	—	—	
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	$\overline{ESR0}$ pin $V_{IN} = 0.69 * V_{DD\_HV\_IO}$	23	—	65	µA
		C		$\overline{ESR0}$ pin $V_{IN} = 0.49 * V_{DD\_HV\_IO}$	—	—	82	
$\lvert I_{WPD} \rvert$	CC	P	Weak pull-down current absolute value	$\overline{PORST}$ pin $V_{IN} = 0.69 * V_{DD\_HV\_IO}$	50	—	130	µA
		C		$\overline{PORST}$ pin $V_{IN} = 0.49 * V_{DD\_HV\_IO}$	40	—	—	
W_{FRST}	SR	P	$\overline{PORST}$ and $\overline{ESR0}$ input filtered pulse	—	—	—	500	ns
W_{NFRST}	SR	P	$\overline{PORST}$ and $\overline{ESR0}$ input not filtered pulse	—	2000	—	—	ns
W_{FNMI}	SR	P	ESR1 input filtered pulse	—	—	—	15	ns
W_{NFNMI}	SR	P	ESR1 input not filtered pulse	—	400	—	—	ns

1. An external 4.7 KOhm pull-up resistor is recommended to be used with the PORST and ESR0 pins for fast negation of the signals.
2. I_{OL_R} applies to both PORST and ESR0: Strong pull-down is active on PHASE0 for PORST. Strong pull-down is active on PHASE0, PHASE1, PHASE2, and the beginning of PHASE3 for ESR0.

$\overline{PORST}$ must be connected to an external power-on supply circuitry. Minimum requested circuitry is external pull-up to ensure device can exit reset.

Note: No restrictions exist on reset signal slew rate apart from absolute maximum rating compliance.

Figure 13. Crystal/Resonator Connections

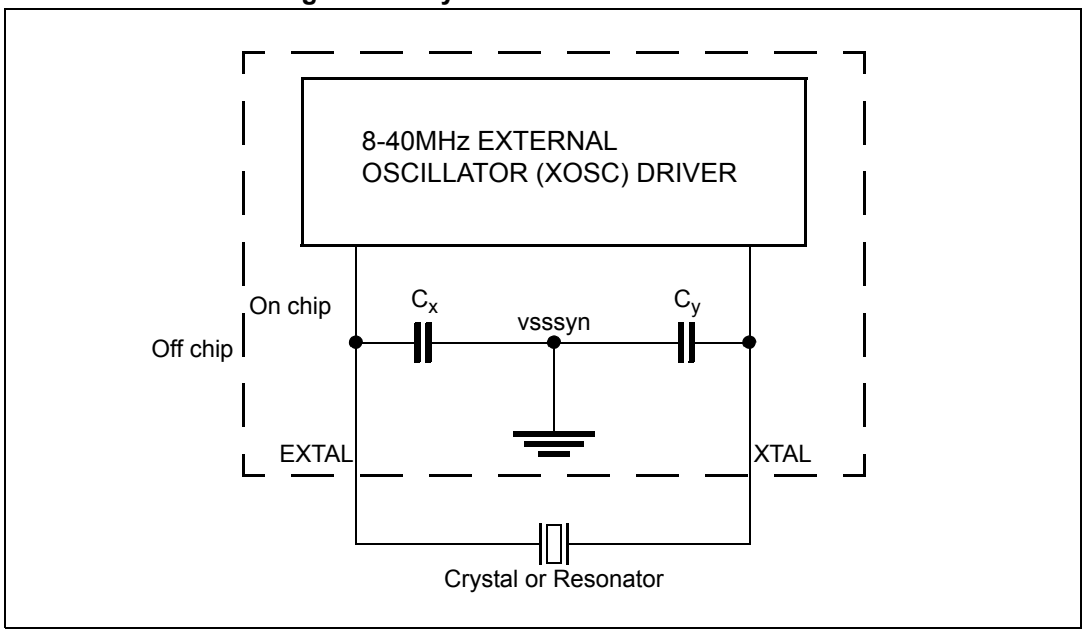


Table 29. Selectable load capacitance

load_cap_sel[4:0] from DCF record	Capacitance offered on EXTAL/XTAL (Cx and Cy)(1),(2) (pF)
00000	1.0
00001	2.0
00010	2.9
00011	3.8
00100	4.8
00101	5.7
00110	6.6
00111	7.5
01000	8.5
01001	9.4
01010	10.3
01011	11.2
01100	12.2
01101	13.1
01110	14.0
01111	15.0
10000–11111(3)	Reserved

1. Values are determined from simulation across process corners and voltage and temperature variation. Capacitance values vary ±12% across process, 0.25% across voltage, and no variation across temperature.

1. All specifications in this table valid for the full input voltage range for the analog inputs.
2. For noise filtering, add a high frequency bypass capacitance of 0.1 µF between $V_{DD\_HV\_ADV}$ and $V_{SS\_HV\_ADV}$.
3. Safety pull-down is available for port pin PB[5] and PE[14]. It enables discharge of up to 100 nF from 5 V every 300 ms.

The SARn ADCs are 12-bit Successive Approximation Register analog-to-digital converters with full capacitive DAC. The SARn architecture allows input channel multiplexing.

Table 33. SARn ADC electrical specification(1)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{ALTREF}	SR	C	ADC alternate reference voltage	$V_{ALTREF} < V_{DD\_HV\_IO\_MAIN}$ $V_{ALTREF} < V_{DD\_HV\_ADV}$	4.5	5.5	V
		C			4.0	5.9	
		P		Extended range with reduce TUE $V_{ALTREF} < V_{DD\_HV\_IO\_MAIN}$ $V_{ALTREF} < V_{DD\_HV\_ADV}$	2.0	5.9	
V_{IN}	SR	D	ADC input signal	$0 < V_{IN} < V_{DD\_HV\_IO\_MAIN}$	$V_{SS\_HV\_ADR}$	$V_{DD\_HV\_ADR}$	V
f_{ADCK}	SR	P	Clock frequency	$T_J < 150$ °C	7.5	14.6	MHz
$t_{ADCPRECH}$	SR	T	ADC precharge time	Fast SAR—fast precharge	135	—	ns
				Fast SAR—full precharge	270	—	
				Slow SAR (SARADC_B)—fast precharge	270	—	
				Slow SAR (SARADC_B)—full precharge	540	—	
ΔV_{PRECH}	SR	D	ADC Precharge voltage	Full precharge $V_{PRECH} = V_{DD\_HV\_ADR}/2$ $T_J < 150$ °C	–0.25	0.25	V
		D		Fast precharge $V_{PRECH} = V_{DD\_HV\_ADR}/2$ $T_J < 150$ °C	–0.5	0.5	V
ΔV_{INTREF}	CC	P	Internal reference voltage precision	Applies to all internal reference points ($V_{SS\_HV\_ADR}$, 1/3 * $V_{DD\_HV\_ADR}$, 2/3 * $V_{DD\_HV\_ADR}$, $V_{DD\_HV\_ADR}$)	–0.20	0.20	V
$t_{ADCSAMPLE}$	SR	P	ADC sample time(2)	Fast SAR – 12-bit configuration	0.750	—	µs
		D		Fast SAR – 10-bit configuration	0.555	—	
		P		Slow SAR (SARADC_B) – 12-bit configuration	1.500	—	
		D		Slow SAR (SARADC_B) – 10-bit configuration	0.833	—	

Table 34. SDn ADC electrical specification(1)(Continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$SNR_{DIFF150}$(9)	CC	T	Signal to noise ratio in differential mode 150 ksps output rate	$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 1 $T_J < 150$ °C	80	—	—	dBFS
		T		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11), $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 2 $T_J < 150$ °C	77	—	—	
		T		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11), $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 4 $T_J < 150$ °C	74	—	—	
		T		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 8 $T_J < 150$ °C	71	—	—	
		D		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 16 $T_J < 150$ °C	68	—	—	
$SNR_{DIFF333}$ (12)	CC	P	Signal to noise ratio in differential mode 333 ksps output rate	$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 1 $T_J < 150$ °C	74	—	—	dBFS
		T		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 2 $T_J < 150$ °C	71	—	—	
		T		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 4 $T_J < 150$ °C	68	—	—	
		T		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 8 $T_J < 150$ °C	65	—	—	
		D		$4.5 < V_{DD\_HV\_ADV} < 5.5$(10),(11) $V_{DD\_HV\_ADR} = V_{DD\_HV\_ADV}$ GAIN = 16 $T_J < 150$ °C	62	—	—	

Table 36. LVDS pad startup and receiver electrical characteristics[1][2](Continued)

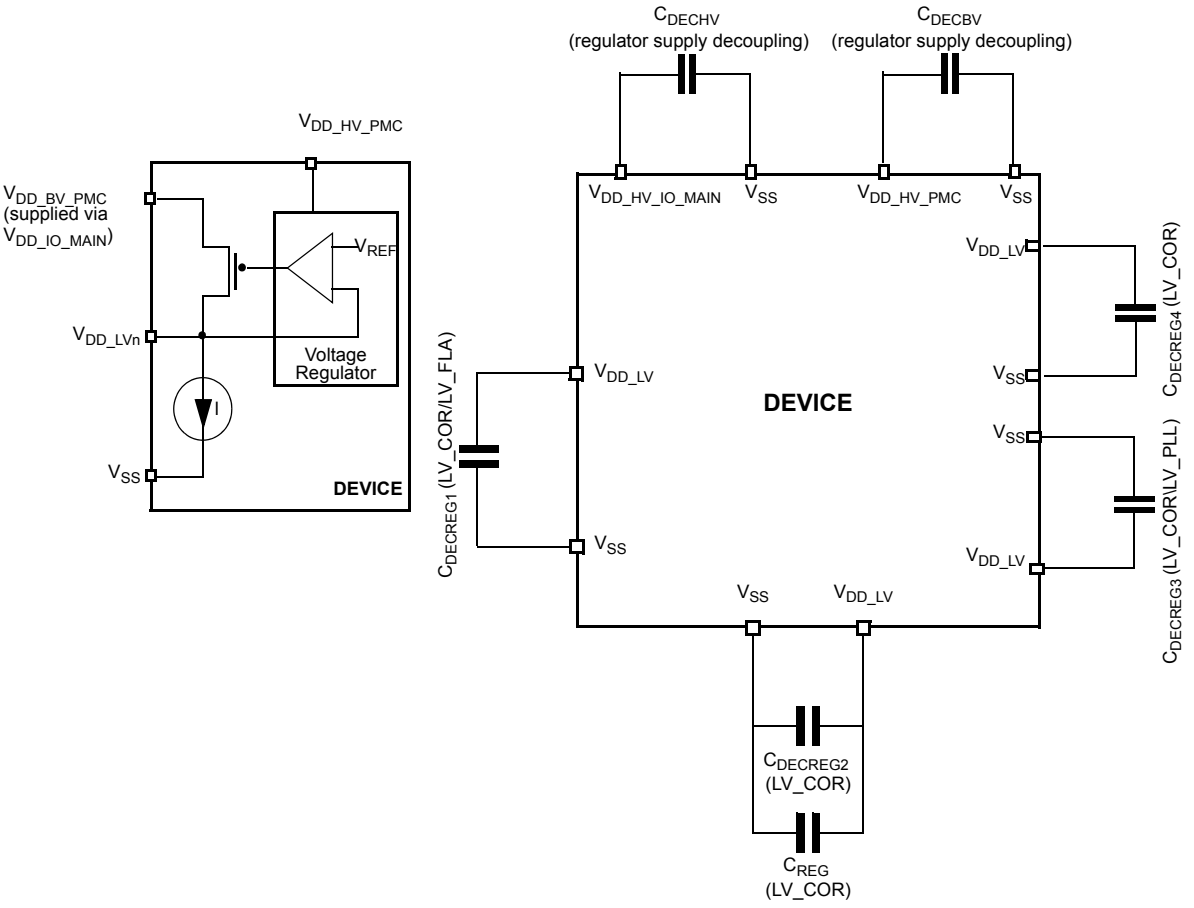
Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
t_{SM2NM_TX}	CC	T	Transmitter startup time (sleep mode to normal mode)[7]	Not applicable to the MSC/DSPI LVDS pad	—	0.2	0.5	µs
t_{PD2NM_RX}	CC	T	Receiver startup time (power down to normal mode)[8]	—	—	20	40	ns
t_{PD2SM_RX}	CC	T	Receiver startup time (power down to sleep mode)[9]	Not applicable to the MSC/DSPI LVDS pad	—	20	50	ns
I_{LVDS_BIAS}	CC	C	LVDS bias current consumption	Tx or Rx enabled	—	—	0.95	mA
TRANSMISSION LINE CHARACTERISTICS (PCB Track)								
Z_0	SR	D	Transmission line characteristic impedance	—	47.5	50	52.5	Ω
Z_{DIFF}	SR	D	Transmission line differential impedance	—	95	100	105	Ω
RECEIVER								
V_{ICOM}	SR	T	Common mode voltage	—	0.15 (10)	—	1.6[11]	V
$\|\Delta_{VI}\|$	SR	T	Differential input voltage[12]	—	100	—	—	mV
R_{IN}	CC	D	Terminating resistance	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%	80	125	150	Ω
		D		$V_{DD\_HV\_IO}$ = 3.3 V ± 10%	80	115	150	Ω
C_{IN}	CC	D	Differential input capacitance[13]	—	—	3.5	6.0	pF
I_{LVDS_RX}	CC	C	Receiver DC current consumption	Enabled	—	—	0.5	mA

1. The LVDS pad startup and receiver electrical characteristics in this table apply to both the LFAST & High-speed Debug (HSD) LVDS pad, and the MSC/DSPI LVDS pad except where noted in the conditions.
2. All LVDS pad electrical characteristics are valid from –40 °C to 150 °C.
3. All startup times are defined after a 2 peripheral bridge clock delay from writing to the corresponding enable bit in the LVDS control registers (LCR) of the LFAST and High-Speed Debug modules. The value of the LCR bits for the LFAST/HSD modules don't take effect until the corresponding SIUL2 MSCR ODC bits are set to LFAST LVDS mode. Startup times for MSC/DSPI LVDS are defined after 2 peripheral bridge clock delay after selecting MSC/DSPI LVDS in the corresponding SIUL2 MSCR ODC field.
4. Startup times are valid for the maximum external loads CL defined in both the LFAST/HSD and MSC/DSPI transmitter electrical characteristic tables.
5. Bias startup time is defined as the time taken by the current reference block to reach the settling bias current after being enabled.
6. Total transmitter startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_TX} + 2 peripheral bridge clock periods.
7. Total transmitter startup time from sleep mode to normal mode is t_{SM2NM_TX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
8. Total receiver startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_RX} + 2 peripheral bridge clock periods.
9. Total receiver startup time from power down to sleep mode is t_{PD2SM_RX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
10. Absolute min = 0.15 V – (285 mV/2) = 0 V

3.17.1 Power management integration

Use the integration scheme provided below to ensure proper device function.

Figure 22. Voltage regulator capacitance connection



Note: The pins positions correspond to the pins positions in the pins package.

The internal voltage regulator requires external capacitance (C_{REGn}) to be connected to the device to provide a stable low voltage digital supply to the device. Placed capacitances on the board as near as possible to the associated pins and limit the serial inductance of the board to less than 5 nH.

Place a decoupling capacitor between each V_{DD_LV} supply pin and V_{SS} ground plane to ensure stable voltage. Place the capacitor as near as possible to the V_{DD_LV} supply pin.

3.17.2 Main voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage ballast supply $V_{DD\_BV\_PMC}$, internally connected to $V_{DD\_HV\_IO\_MAIN}$ supply. The regulator itself is supplied by $V_{DD\_HV\_PMC}$. Both high voltage supplies are common with $V_{DD\_HV\_IO}$.

Note: Refer to SPC574Kx_IO_Signal_Table.xls table for details regarding power connectivity.

Table 42. Voltage monitor electrical characteristics(1)(Continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$t_{VDASSERT}$	CC	D	Voltage detector threshold crossing assertion	—	0.1	—	2	µs
$t_{VDRELEASE}$	CC	D	Voltage detector threshold crossing de-assertion	—	5	—	20	µs

1. For V_{DD_LV} levels, a maximum of 30 mV IR drop is incurred from the pin to all sinks on the die. For other LVD, the IR drop is estimated by multiplying the supply current by 0.5 Ω.
2. V_{PORUP_LV} and V_{PORUP_HV} threshold are untrimmed values before completion of the power-up sequence. All other LVD/HVD thresholds are provided after trimming.
3. Assume all of LVDs on LV supplies disabled.
4. LV internal supply levels are measured on device internal supply grid after internal voltage drop.
5. LVD is released after $t_{VDRELEASE}$ temporization when *upper* threshold is crossed, LVD is asserted $t_{VDASSERT}$ after detection when *lower* threshold is crossed.
6. This is combination of LVD108_C, P, and F. Min is from min value of LVD108_F, and P which is the lowest one. Max is the max value of LVD108_C which is the highest one of three.
7. LV external supply levels are measured on the die side of the package bond wire after package voltage drop.
8. HVD is released after $t_{VDRELEASE}$ temporization when *lower* threshold is crossed, HVD is asserted $t_{VDASSERT}$ after detection when *upper* threshold is crossed. HVD140 does not cause reset.
9. This supply also needs to be below 5472 mV (untrimmed HVD600 min).
10. Untrimmed LVD300_A will be asserted first on power down.
11. Hysteresis is implemented only between the VDD_HV_IO_MAIN High voltage Supplies and the ADC high voltage supply. When these two supplies are shorted together, the hysteresis is as is shown in *Table 42*. If the supplies are not shorted (VDD_IO_MAIN and ADC high voltage supply), then there will be no hysteresis on the high voltage supplies.

3.17.4 Power up/down sequencing

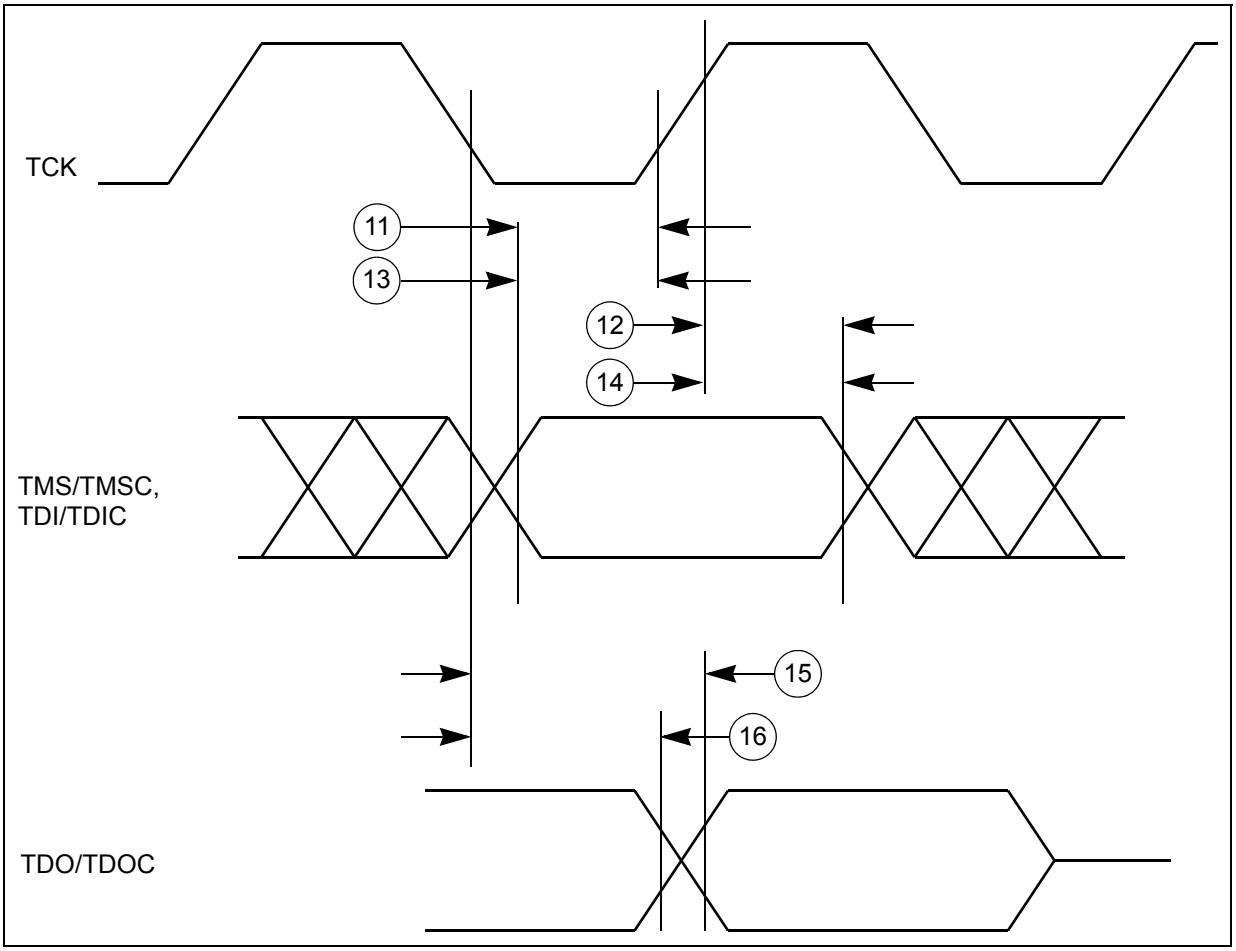
The following table shows the constraints and relationships for the different power supplies.

Table 43. Device supply relation during power-up/power-down sequence

		Supply 2(1)					
		V_{DD_LV}	$V_{DD\_HV\_IO\_JTAG}$/ $V_{DD\_HV\_IO\_FLEX}$	$V_{DD\_HV\_IO}$	$V_{DD\_HV\_ADV}$	$V_{DD\_HV\_ADR}$	ALTREFn(2)
Supply 1(1)	V_{DD_LV}						
	$V_{DD\_HV\_IO\_JTAG}$/ $V_{DD\_HV\_IO\_FLEX}$						
	$V_{DD\_HV\_IO}$						
	$V_{DD\_HV\_ADV}$						
	$V_{DD\_HV\_ADR}$				5 mA		
	ALTREFn			10 mA(3)	10 mA(3)		

1. Red cells: Supply 1 (row) can exceed Supply 2 (column), granted that external circuitry ensures current flowing from supply1 is less than absolute maximum rating current value provided.
2. ALTREFn are the alternate references for the ADC that can be used in place of the default reference ($V_{DD\_HV\_ADR\_*}$). They are SARB.ALTREF and SAR2.ALTREF.

Figure 29. Nexus TDI/TDIC, TMS/TMSC, TDO/TDOC timing



3.19.1.3 Aurora LVDS interface timing

Table 50. Aurora LVDS interface timing specifications

Symbol		C	Parameter	Value			Unit
				Min	Typ	Max	
Data Rate							
—	SR	T	Data rate	—	—	1250	Mbps
STARTUP							
t_{STRT_BIAS}	CC	T	Bias startup time(1)	—	—	5	µs
t_{STRT_TX}	CC	T	Transmitter startup time(2)	—	—	5	µs
t_{STRT_RX}	CC	T	Receiver startup time(3)	—	—	4	µs

1. Startup time is defined as the time taken by LVDS current reference block for settling bias current after its pwr_down (power down) has been deasserted. LVDS functionality is guaranteed only after the startup time.
2. Startup time is defined as the time taken by LVDS transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.

Table 58. DSPI CMOS Slave timing - Modified Transfer Format (MTFE = 0/1)(1)(Continued)

#	Symbol		C	Characteristic	Condition		Min	Max	Unit
					Pad Drive	Load			
9	t_{SUI}	CC	D	Data Setup Time for Inputs(2)	—	—	10	—	ns
10	t_{HI}	CC	D	Data Hold Time for Inputs(2)	—	—	10	—	ns
11	t_{SUO}	CC	D	SOUT Valid Time(2),(3),(4) (after SCK edge)	Very Strong	25 pF	—	30	ns
					Strong	50 pF	—	30	ns
					Medium	50 pF	—	50	ns
12	t_{HO}	CC	D	SOUT Hold Time(2),(3),(4) (after SCK edge)	Very Strong	25 pF	2.5	—	ns
					Strong	50 pF	2.5	—	ns
					Medium	50 pF	2.5	—	ns

1. DSPI slave operation is only supported for a single master and single slave on the device. Timing is valid for that case only.
2. Input timing assumes an input slew rate of 1 ns (10% - 90%) and uses TTL / Automotive voltage thresholds.
3. All timing values for output signals in this table, are measured to 50% of the output voltage.
4. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

Figure 40. DSPI Slave Mode - Modified transfer format timing (MFTE = 0/1)—CPHA = 0

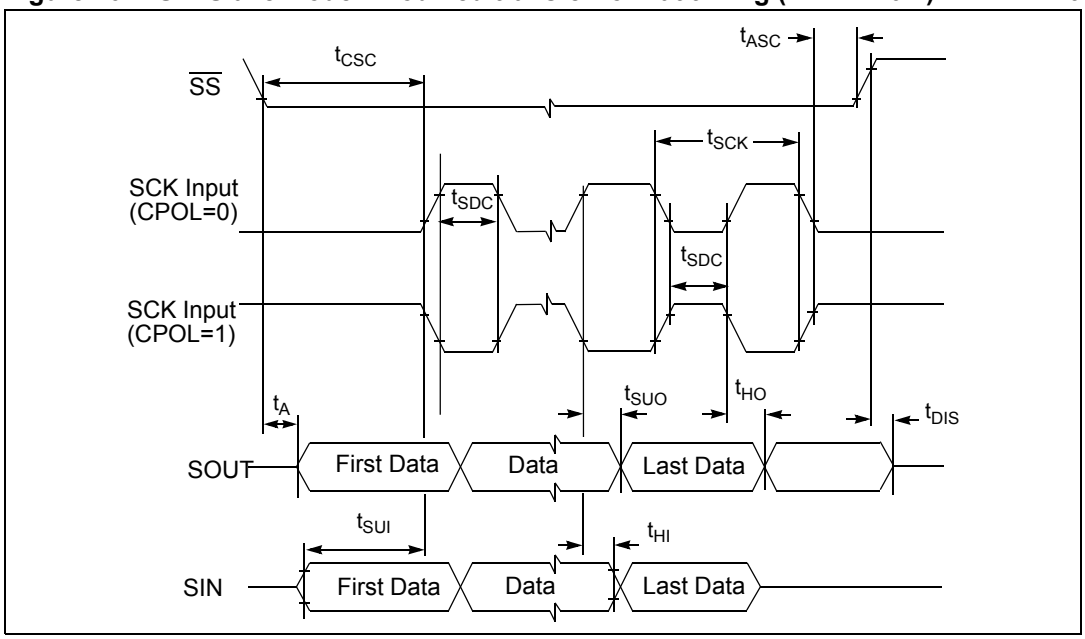


Table 74. Revision history(Continued)

Revision	Date	Description of changes
2 (cont'd)	30 Aug 2012	Updated *Table 28 (External Oscillator electrical specifications)* Updated *Table 29 (Selectable load capacitance)* Updated Table 26 (SARn ADC electrical specification) Updated *Table 34 (SDn ADC electrical specification)* Revised Section 3.13, ADC specifications *Figure 19 (Power-down exit time)*: replaced symbol "Tsu" with "t_{PD2NM_TX}" *Table 35 (Temperature sensor electrical characteristics)*: – Following symbols added: T_{SENS}, T_{ACC}, I_{TEMP_SENS} – Following sentence removed from footnote: "All values above are comprehended in the IP test plan for 100% testing, except Power." – Footnote deleted: "Temperature sensor continues to function between 150 °C and 165 °C but accuracy is degraded" Table 37 (LFAST interface electrical characteristics): removed redundant footnote Replaced section "DigRF electrical characteristics" with *Section 3.15, LVDS Fast Asynchronous Serial Transmission (LFAST) pad electrical characteristics* Updated *Table 39 (LFAST PLL electrical characteristics)* Updated *Table 40 (Aurora LVDS electrical characteristics)* – Specification change: R_{V_L} (Terminating resistance): min value is 81 ohm (was 90); max value is 120 ohm (was 110). – Footnote added to $\lvert\Delta V_{OD\_LVDS}\rvert$ (Differential output voltage swing (terminated)): "The minimum value of 400 mV is only valid for differential terminating resistance (R_{V_L}) = 99 ohm to 101 ohm. The differential output voltage swing tracks with the value of R_{V_L}." – Updated and renamed specification f_{RX} Receive Clock Rate (was Receive Data Rate) – Specification description changed from "$\lvert\Delta V_{I\_L}\rvert$ (Differential input voltage)" to "Differential input voltage (peak to peak)". – Clarification: The maximum value of T_{Loss} (Transmission Line Loss due to loading effects) is specified for the maximum drive level of the Aurora transmit pad. – Note added: "The Aurora interface is AC coupled, so there is no common-mode voltage specification." – Footnote (applies to entire table) updated: "All Aurora electrical characteristics are valid from –40 °C to 165 °C, except where noted" Reorganized subsections of Section 3.17, Power management: PMC, POR/LVD, sequencing *Table 41 (Device Power Supply Integration)*: – Replaced "TBD" with "—" in Typ column – Removed V_{SREG}, I_{SREG}, $I_{LPREGINT}$ Updated *Table 42 (Voltage monitor electrical characteristics)* *Table 43 (Device supply relation during power-up/power-down sequence)*: – Replaced "$V_{DD\_HV\_PMC}$" with $V_{DD\_HV\_IO\_JTAG}$/$V_{DD\_HV\_IO\_FLEX}$ – Replaced "$V_{DD\_HV\_PMU}$" with $V_{DD\_HV\_IO\_JTAG}$/$V_{DD\_HV\_IO\_FLEX}$ – Replaced $V_{DD\_HV\_ADR}$ row value from 2 mA to 5 mA Changed instance of "Supply 1" to "Supply 2" in column header row *Table 44 (Functional terminals state during power-up and reset)*: – Changed "Power-up pad state" column value from "High impedance" to "weak pull-up" in TDI row – Updated pad states in TMS row *Section 3.17.3, Device voltage monitoring*: added introductory text Updated Table 44 (Flash memory program and erase specifications (pending silicon characterization)) Revised Section 3.19.2, DSPI Timing with CMOS and LVDS Pads *Table 48 (JTAG pin AC electrical characteristics)*: – Changed all parameters from "C" to "D" – Specification change: t_{TCYC} (TCK cycle time) is 100 ns (was 40 ns). Boundary scan frequency is limited to 10 MHz or less.

Table 74. Revision history(Continued)

Revision	Date	Description of changes
3 (cont'd)	31 Jan 2014	*Table 19 (I/O pull-up/pull-down DC electrical characteristics)*: – $\|I_{WPU}\|$ Parameter is *Weak pull-up current absolute value* – $\|I_{WPU}\|$ (P) condition is $V_{IN} < V_{IH} = 0.69*V_{DD\_HV\_IO}$, 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V – $\|I_{WPU}\|$ (P) min is 23 µA, max is — – Removed: $\|I_{WPU}\|$ (T) at V_{IN} = 0 V, 3.0 V < $V_{DD\_HV\_IO}$ < 4.0 V – Added: $\|I_{WPU}\|$ (T) at $V_{IN} > V_{IL} = 0.49*V_{DDE}$, 4.5 V < V_{DD} < 5.5 V – Added: $\|I_{WPU}\|$ (T) at $V_{IN} > V_{IL}$ = 1.1 V (TTL), 4.5 V < V_{DD} < 5.5 V – Added: R_{WPU} (Weak pull-up resistance) – $\|I_{WPD}\|$ (P) condition is $V_{IN} > V_{IH} = 0.69*V_{DDE}$, 4.5 V < V_{DD} < 5.5 V – $\|I_{WPD}\|$ (P) min. is —, max is 130 µA – Removed: $\|I_{WPD}\|$ (T) at $V_{IN} = V_{DD\_HV\_IO}$, 3.0 V < $V_{DD\_HV\_IO}$ < 4.0 V – Added: $\|I_{WPD}\|$ (T) at $V_{IN} < V_{IL} = 0.49*V_{DDE}$, 4.5 V < V_{DD} < 5.5 V – Added: $\|I_{WPD}\|$ (T) at $V_{IN} < V_{IL}$ = 0.9 V (TTL), 4.5 V < V_{DD} < 5.5 V – Added: R_{WPD} (Weak pull-down resistance) – Replaced "$V_{IN} > V_{IH}$" with "$V_{IN} < V_{IH}$" and "$V_{IN} < V_{IH}$" with "$V_{IN} > V_{IH}$" in the first two rows of $\|I_{WPD}\|$ – Replaced V_{DD} with $V_{DD\_HV\_IO}$ in the conditions column of I_{WPU} and I_{WPD} *Section 3.9.2, I/O output DC characteristics*: – Removed references to EBI in document. *Table 20 (WEAK configuration output buffer electrical characteristics)*: – Added footnote *All VDD_HV_IO conditions for 4.5V to 5.9V...* – Added footnote *Only for VDD_HV_IO_JTAG segment...* – Added new parameter "Propagation delay". *Table 21 (MEDIUM configuration output buffer electrical characteristics)*: – R_{OH_M} condition is 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V, Push pull, I_{OH} < 2 mA – R_{OL_M} condition is 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V, Push pull, I_{OH} < 2 mA – t_{TR_M} condition is C_L = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V – t_{TR_M} condition is C_L = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V – t_{TR_M} condition is C_L = 200 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V – Added footnotes: *All VDD_HV_IO...* and *Only for VDD_HV_IO_JTAG...* – Added new parameter "Propagation delay". *Table 22 (STRONG configuration output buffer electrical characteristics)*: – R_{OH_S} condition is 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V, Push pull, I_{OH} < 8 mA; – R_{OL_S} condition is 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V, Push pull – I_{OH} < 8 mA; t_{TR_S} condition changed to C_L = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V – t_{TR_S} condition changed to C_L = 200 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V – t_{TR_S} condition C_L = 25 pF, 4.0 V < $V_{DD\_HV\_IO}$ < 5.9 V changed to C_L = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V – Added footnotes: *All VDD_HV_IO conditions for 4.5V to 5.9V...* and *Only for VDD_HV_IO_JTAG segment...* – Added new parameter "Propagation delay" *Table 23 (VERY STRONG configuration output buffer electrical characteristics)*: – In rows R_{OH_V} and R_{OL_V}: Conditions for C Parameter changed to *VSIO[VSIO_xx] = 1, Push pull, I_{OH} < 7 mA*, Value Min is 30, TYP is 50, Max is 75. – In row f_{SYS}: Conditions for C Parameter changed to *VSIO[VSIO_xx] = 1, C_L = 15 pF* – Added footnote: *All VDD_HV_IO conditions for 4.5V to 5.9V...*

Table 74. Revision history(Continued)

Revision	Date	Description of changes
3 (cont'd)	31 Jan 2014	– Updated footnote *The 640 MHz frequency is achieved...* – f_{ADCD_M} specification, removed footnote "V_{INM} is the input voltage applied to the negative terminal of the SDADC." – f_{ADCD_M} specification, changed parameter from "S/D clock" to "S/D modulator input clock" – Changed f_{ADCD_M} Min from "—" to "4". – RESOLUTION specification, added footnote "When using a GAIN setting of 16, the conversion result will always have a value of zero in the least significant bit. The gives an effective resolution of 15 bits." – $\|\delta_{GAIN}\|$ specification, changed Max value from "0.1" % to "5" mV, "0.25" % to "7.5" mV, and "0.5" % to "10" mV. – Common mode rejection ratio parameter change symbol from "—" to "V_{cmrr}" – Anti-aliasing filter parameter, changed symbol "—" to "R_{Caaf}" – Stop band attenuation parameter, changed "symbol "—" to "$F_{rolloff}$". – For tLATENCY, tSETTLING, and tODRECOVERY specifications, changed max from 2 * &GROUP to "2 * &$_{GROUP}$ + 7 * f_{ADCD_S}". – Changed footnote 9 in "full input range (specified by Vin)" to "full input frequency range." – Changed footnote 11 "0.873" dB to "0.087" dB. – Changed footnote from "The ±1% passband ripple specification is equivalent to 20 * $\log_{10}$ (0.99) = 0.87 dB." to "The ±1% passband ripple specification is equivalent to 20 * $\log_{10}$ (0.99) = 0.087 dB. – $t_{STARTUP}$ renamed as $t_{POWERUP}$ – $t_{LATENCY}$ renamed as $t_{STARTUP}$ – A new parameter $t_{LATENCY}$ added – Max value of δ_{GROUP} modified for all values of OSR – new condition and max value added for $t_{STARTUP}$, $t_{LATENCY}$, $t_{SETTLING}$ and $t_{ODRECOVERY}$. – $t_{POWERUP}$ renamed as $t_{STARTUP}$. – $t_{STARTUP}$ row removed. – Description of $t_{LATENCY}$ changed from "Latency between input data and converted data" to "Latency between input data and converted data when input mux does not change". – Max value of $t_{LATENCY}$ changed from "2*δ_{GROUP} + f_{ADCD_S}" to "δ_{GROUP} + f_{ADCD_S}". – Maximum value of parameter "GAIN" changed from 16 to 15. – Replaced the "—" in the conditions column of f_{ADCD_S} with "T_J < 150 °C" – Replaced "2*δ_{GROUP}" with "δ_{GROUP}" in the max column of $t_{LATENCY}$ – For max value of $\|\delta_{GAIN}\|$ row, replaced "1" with "1.5" – Added one new table: Table 34 (Electrical specifications) *Table 35 (Temperature sensor electrical characteristics)*: – In row I_{TEMP_SENS} max value changed to 700 µA – In row T_{SENS} changed Parameter classification to *P* – In row T_{ACC} added condition $T_J < 165$ °C – The minimum value of "T_{ACC}" changed from 7 to "-7". *Table 36 (LVDS pad startup and receiver electrical characteristics)*: – $\|\Delta_{VI}\|$ specification, Differential input voltage parameter, added footnote 12 "The LXRXOP[0] bit in the LFAST LVDS Control Register (LCR) must be set to one to ensure proper LFAST receive timing." – max value of t_{STRT_BIAS} changed from 0.8 µs to 4 µs – max value of t_{PD2NM_TX} changed from 0.55 µs to 2.75 µs

Table 74. Revision history(Continued)

Revision	Date	Description of changes
3 (cont'd)	31 Jan 2014	*Table 42 (Voltage monitor electrical characteristics)*: – V_{LVD108} specification, changed Min value from "1080" to "1120" – V_{LVD108} specification, changed Max value from "1140" to "1170" – V_{LVD108}Changed Parameter name "LV internal supply low voltage monitoring" to "Core LV internal supply low voltage monitoring" and added note to conditions "This is combination of LVD108_C, P, and F. Min is from min value of LVD108_F, and P which is the lowest one. Max is the max value of LVD108_C which is the highest one of three." – V_{PORUP_LV} Falling voltage (power down) condition, added footnote "assume all of LVDs on LV supplies disabled". – Added "HVD140 does not cause reset" at end of footnote "HVD is released after $t_{VDRELEASE}$ temporization when lower threshold is crossed, HVD is asserted tVDASSERT after detection when upper threshold is crossed." – V_{LVD295} Rising voltage condition changed Max value "3100" to "3120". – V_{LVD295} Falling voltage condition changed Min value "2950" to "2920" and Max value "3080" to "3100". – V_{HVD360} Rising voltage condition changed Min value "3420" to "3435" and Max value "3610" to "3650". – V_{HVD360} Falling voltage condition changed Min value "3400" to "3415". *Table 44 (Functional terminals state during power-up and reset)*: – Replaced "Weak pull-down" with "Weak pull-up" for ESR1 in Power-up, reset, and default states – Replaced "ERROR" with "ERROR[0]" – Updated note 6 – ESR1 POWER-UP Pad State changed to *Weak pull-down.* *Table 45 (Flash memory program and erase specifications)*: Updated the values. *Table 46 (Flash memory Life Specification)*: Replaced "K" with "k" in the unit column *Section 3.18.1, Flash read wait state and address pipeline control settings*: Added this section Moved I^2C AC timing specification after section "UART timing" Moved "UART timing" section after "PSI5 timing" Table 48 (K2 Flash memory program and erase specifications(pending silicon characterization)) – Complete rework of table and contents. – In row $t_{dwprogram}$: • removed Initial max parameter classification • Lifetime max changed to 650 – In row $t_{pprogra}$: • Initial max parameter classification removed – Added row $t_{pprogrameep}$ [KGD] – In row $t_{qprogram}$: • Typical end of life changed to 396 – Added row $t_{qprogrameep}$ [KGD]

Table 74. Revision history(Continued)

Revision	Date	Description of changes
3 (cont'd)	31 Jan 2014	– Differentiated rows $t_{16kprogrameep}$ with [KGD] and [Packaged part] – In row $t_{16kprogrameep}$ [Packaged part]: • Typ value changed to 31 • Initial max 25 °C changed to 40 • Initial max All temp changed to 58 • Typical end of life changed to 64 – In row $t_{16kprogrameep}$ [KGD]: • Typ value changed to 40.5 • Initial max 25 °C changed to 52.5 – In row t_{pr}: • Characteristics footnote changed to *Rate computed based on 256K sectors.* – In row $t_{fferase}$: – Characteristics footnote changed to *Only code sectors, not including EEPROM* – In row t_{PSRT}: • Characteristics footnote changed to *Time between suspend resume and...* – In row t_{PSUS}: • Initial max 25 °C value removed – In row t_{ESUS}: • characteristics footnote changed to *Timings guaranteed by design.* • Initial max 25 °C value removed – Added row t_{AICOP} – Footnote: *For memory sizes > 1 MB and...* changed to *Actual hardware programming times...* Added new Section 3.19.2, DSPI timing with CMOS and LVDS pads *Table 48 (JTAG pin AC electrical characteristics)*: Added footnote "JTAG timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 4.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the data sheet." *Table 49 (Nexus debug port timing)*: – t_{TCYC} (TCK cycle time) min value changed to 2 – Header "1K cycles" modified to "1k cycles". – Footnote 1 changed to "Nexus timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 4.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the data sheet." – Added (TDO sampled on posedge of TCK) to t_{TCYC} in the characteristics column and changed the min value from "36" to "40" Section 3.19.4, FlexRay timing: Added new section that includes "DSPI CMOS Slave timing - Modified Transfer Format (MTFE = 1)" table and timing diagrams "DSPI Slave Mode - Modified transfer format timing (MFTE = 1) — CPHA = 0" and "DSPI Slave Mode - Modified transfer format timing (MFTE = 1) — CPHA = 1". *Table 58 (DSPI CMOS Slave timing - Modified Transfer Format (MTFE = 0/1))*: – Changed table title "(MTFE = 1)" to "(MTFE = 0/1)" – Added footnote 1 to table title "DSPI slave operation is only supported for a single master and single slave on the device. Timing is valid for that case only." *Figure 40 (DSPI Slave Mode - Modified transfer format timing (MFTE = 0/1)—CPHA = 0)*: Changed figure title "(DSPI Slave Mode - Modified transfer format timing (MFTE = 1) — CPHA = 0) to "(DSPI Slave Mode - Modified transfer format timing (MFTE = 0/1) — CPHA = 0)".

Table 74. Revision history(Continued)

Revision	Date	Description of changes
4 (cont'd)	19 Dec 2014	– The maximum value changed from "15" to "16" for the maximum value for GAIN. – Added note to $t_{LATENCY}$ and $t_{SETTLING}$. – SNR_{SE150} specification: changed footnote to "This parameter is guaranteed by bench validation with a small sample of typical devices, and tested in production to a value of 6 dB less" (was 2 dB less). Removed the Table : Electrical specifications. *Table 42 (Voltage monitor electrical characteristics)*: – Changed the minimum and maximum value of V_{LVD108}. – Updated the minimum and maximum value of V_{PORUP_HV}. *Table 47 (Flash memory RWSC configuration)*: – Replaced "40 – 160 MHz" with "140 – 160 MHz" in the Platform Frequency column. *Table 52 (DSPI channel frequency support)*: – Added CMOS Slave mode. *Table 64 (RxD input characteristics)*: – Revised footnote ("FlexRay RxD timing is valid. . ."). *Section 3.19.8, GPIO delay timing*: – Added this section. Table 65 (Order codes): – Replaced EMU574K72K5-AA, EMU574K72K7-AA with EMU574K72K5-BB and EMU574K72K7-BB respectively. – Removed figure "Emulation device code structure EMU574M72K5-AA".