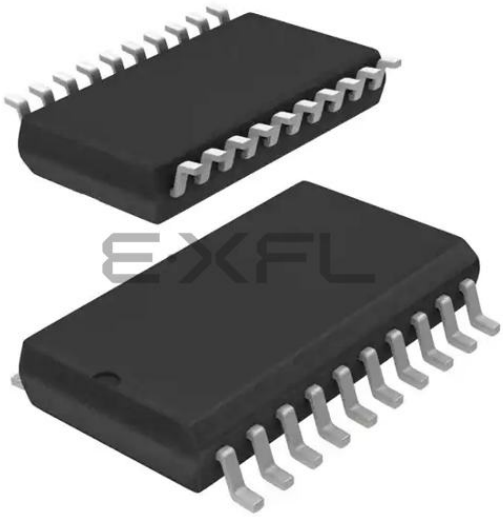

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Details	
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Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SO
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p87lpc767bd-512

Low power, low price, low pin count (20 pin) microcontroller with 4-kbyte OTP and 8-bit A/D converter

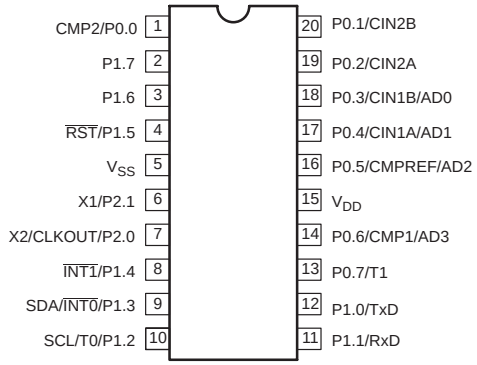
P87LPC767

GENERAL DESCRIPTION **1**
FEATURES **1**
ORDERING INFORMATION **2**
PIN CONFIGURATION, 20-PIN DIP AND SO PACKAGES **2**
LOGIC SYMBOL **2**
BLOCK DIAGRAM **3**
PIN DESCRIPTIONS **5**
SPECIAL FUNCTION REGISTERS **6**
FUNCTIONAL DESCRIPTION **8**
Enhanced CPU 8
Analog Functions 8
Analog to Digital Converter 8
A/D Timing 9
The A/D in Power Down and Idle Modes 10
Code Examples for the A/D 11
Analog Comparators 12
Comparator Configuration 12
Internal Reference Voltage 14
Comparator Interrupt 14
Comparators and Power Reduction Modes 14
Comparator Configuration Example 14
I^2C Serial Interface 15
I^2C Interrupts 15
Reading I2CON 15
Checking ATN and DRDY 17
Writing I2CON 17
Regarding Transmit Active 17
Regarding Software Response Time 18
Interrupts 19
External Interrupt Inputs 20
I/O Ports 21
Quasi-Bidirectional Output Configuration 21
Open Drain Output Configuration 22
Push-Pull Output Configuration 22
Keyboard Interrupt (KBI) 23
Oscillator 25
Low Frequency Oscillator Option 25
Medium Frequency Oscillator Option 25
High Frequency Oscillator Option 25
On-Chip RC Oscillator Option 25
External Clock Input Option 25
Clock Output 25
CPU Clock Modification: CLKR and DIVM 27
Power Monitoring Functions 27
Brownout Detection 27
Power On Detection 28
Power Reduction Modes 28
Idle Mode 28
Power Down Mode 28
Low Voltage EPROM Operation 30
Reset 30
Timer/Counters 31
Mode 0 32
Mode 1 33

ORDERING INFORMATION

Type number	Package			Temperature Range (°C)
	Name	Description	Version	
P87LPC767BN	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1	0 to +70
P87LPC767BD	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1	0 to +70
P87LPC767FN	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1	–40 to +85
P87LPC767FD	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1	–40 to +85
P87LPC767HD	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1	–40 to +125

PIN CONFIGURATION, 20-PIN DIP AND SO PACKAGES



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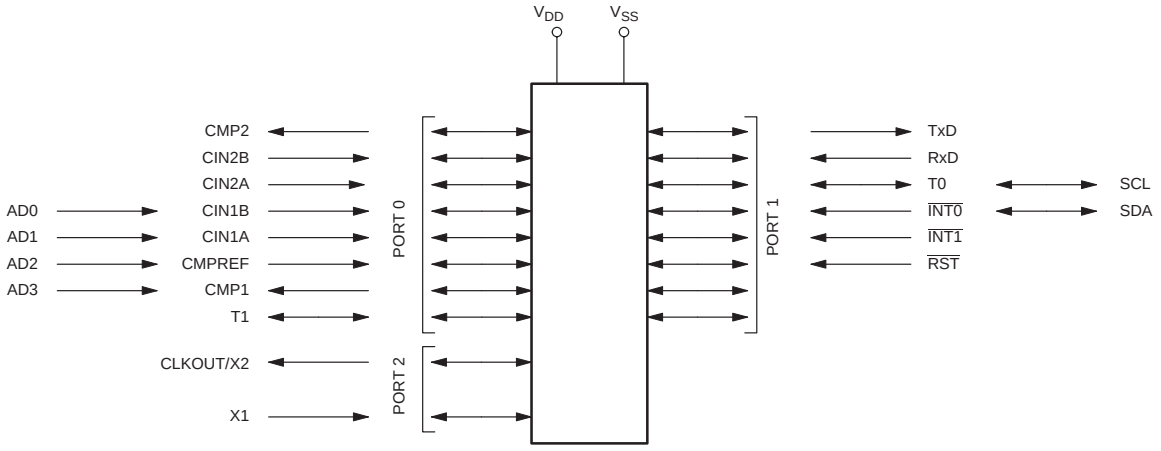
LOGIC SYMBOL



SU01350

FUNCTIONAL DESCRIPTION

Details of P87LPC767 functions will be described in the following sections.

Enhanced CPU

The P87LPC767 uses an enhanced 80C51 CPU which runs at twice the speed of standard 80C51 devices. This means that the performance of the P87LPC767 running at 5 MHz is exactly the same as that of a standard 80C51 running at 10 MHz. A machine cycle consists of 6 oscillator cycles, and most instructions execute in 6 or 12 clocks. A user configurable option allows restoring standard 80C51 execution timing. In that case, a machine cycle becomes 12 oscillator cycles.

In the following sections, the term “CPU clock” is used to refer to the clock that controls internal instruction execution. This may sometimes be different from the externally applied clock, as in the case where the part is configured for standard 80C51 timing by means of the CLKR configuration bit or in the case where the clock is divided down via the setting of the DIVM register. These features are described in the Oscillator section.

Analog Functions

The P87LPC767 incorporates analog peripheral functions: an Analog to Digital Converter and two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and inputs disabled.

Digital outputs are disabled by putting the port output into the Input Only (high impedance) mode as described in the I/O Ports section.

Digital inputs on port 0 may be disabled through the use of the PT0AD register. Each bit in this register corresponds to one pin of Port 0. Setting the corresponding bit in PT0AD disables that pin’s digital input. Port bits that have their digital inputs disabled will be read as 0 by any instruction that accesses the port.

Analog to Digital Converter

The P87LPC767 incorporates a four channel, 8-bit A/D converter. The A/D inputs are alternate functions on four port 0 pins. Because the device has a very limited number of pins, the A/D power supply and references are shared with the processor power pins, V_{DD} and V_{SS}. The A/D converter operates down to a V_{DD} supply of 3.0 V.

The A/D converter circuitry consists of a 4-input analog multiplexer and an 8-bit successive approximation ADC. The A/D employs a ratiometric potentiometer which guarantees DAC monotonicity.

The A/D converter is controlled by the special function register ADCON. Details of ADCON are shown in Figure 2. The A/D must be enabled by setting the ENADC bit at least 10 microseconds before a conversion is started, to allow time for the A/D to stabilize. Prior to the beginning of an A/D conversion, one analog input pin must be selected for conversion via the AADR1 and AADR0 bits. These bits cannot be changed while the A/D is performing a conversion.

An A/D conversion is started by setting the ADCS bit, which remains set while the conversion is in progress. When the conversion is complete, the ADCS bit is cleared and the ADCI bit is set. When ADCI is set, it will generate an interrupt if the interrupt system is enabled, the A/D interrupt is enabled (via the EAD bit in the IE1 register), and the A/D interrupt is the highest priority pending interrupt.

When a conversion is complete, the result is contained in the register DAC0. This value will not change until another conversion is started. Before another A/D conversion may be started, the ADCI bit must be cleared by software. The A/D channel selection may be changed by the same instruction that sets ADCS to start a new conversion, but not by the same instruction that clears ADCI.

The connections of the A/D converter are shown in Figure 3.

The ideal A/D result may be calculated as follows:

$$\text{Result} = (V_{IN} - V_{SS}) \times \frac{256}{V_{DD} - V_{SS}} \quad \text{(round result to the nearest integer)}$$

Table 1. Example A/D Conversion Times

CPU Clock Rate	RCCLK = 0	RCCLK = 1		
		minimum	nominal	maximum
32 kHz	NA	563.4 µs	659 µs	757 µs
1 MHz	186 µs	32.4 µs	39.3 µs	48.9 µs
4 MHz	46.5 µs	18.9 µs	23.6 µs	30.1 µs
11.0592 MHz	16.8 µs	16 µs	20.2 µs	27.1 µs
12 MHz	15.5 µs			
16 MHz	11.6 µs			
20 MHz	9.3 µs			

Note: Do not clock ADC from the RC oscillator when MCU clock is greater than 4 MHz.

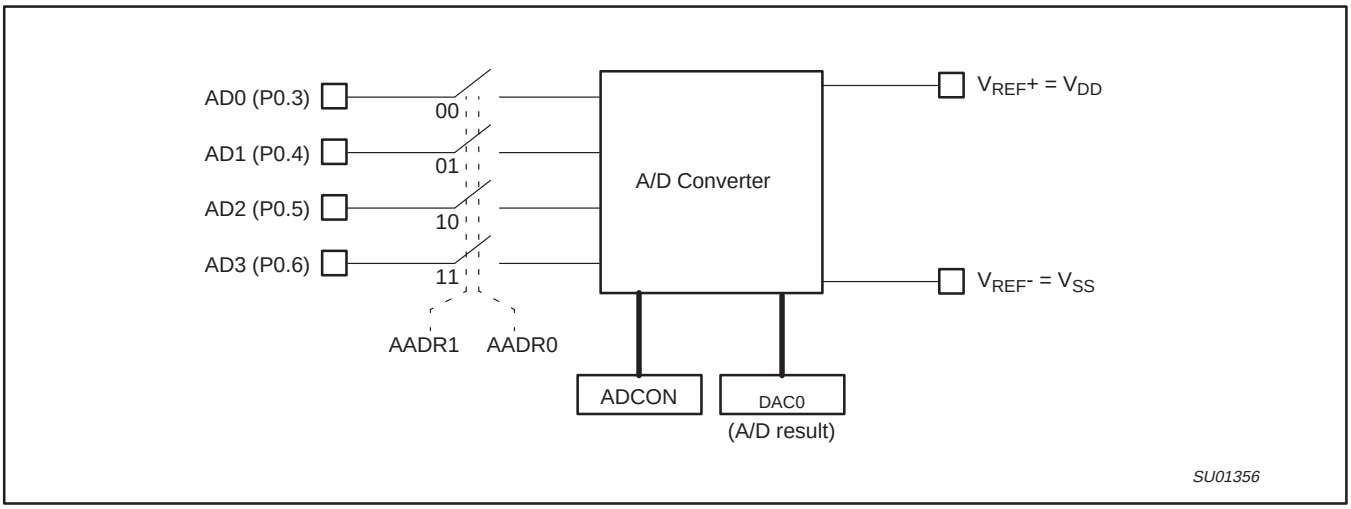


Figure 3. A/D Converter Connections

The A/D in Power Down and Idle Modes

While using the CPU clock as the A/D clock source, the Idle mode may be used to conserve power and/or to minimize system noise during the conversion. CPU operation will resume and Idle mode terminate automatically when a conversion is complete if the A/D interrupt is active. In Idle mode, noise from the CPU itself is eliminated, but noise from the oscillator and any other on-chip peripherals that are running will remain.

The CPU may be put into Power Down mode when the A/D is clocked by the on-chip RC oscillator (RCCLK = 1). This mode gives the best possible A/D accuracy by eliminating most on-chip noise sources.

If the Power Down mode is entered while the A/D is running from the CPU clock (RCCLK = 0), the A/D will abort operation and will not wake up the CPU. The contents of DAC0 will be invalid when operation does resume.

When an A/D conversion is started, Power Down or Idle mode must be activated within two machine cycles in order to have the most accurate A/D result. These two machine cycles are counted at the CPU clock rate. When using the A/D with either Power Down or Idle mode, care must be taken to insure that the CPU is not restarted by another interrupt until the A/D conversion is complete. The possible causes of wakeup are different in Power Down and Idle modes.

A/D accuracy is also affected by noise generated elsewhere in the application, power supply noise, and power supply regulation. Since the P87LPC767 power pins are also used as the A/D reference and supply, the power supply has a very direct affect on the accuracy of A/D readings. Using the A/D without Power Down mode while the clock is divided through the use of CLKR or DIVM has an adverse effect on A/D accuracy.

Analog Comparators

Two analog comparators are provided on the P87LPC767. Input and output options allow use of the comparators in a number of different configurations. Comparator operation is such that the output is a logical one (which may be read in a register and/or routed to a pin) when the positive input (one of two selectable pins) is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be configured to cause an interrupt when the output value changes.

Comparator Configuration

Each comparator has a control register, CMP1 for comparator 1 and CMP2 for comparator 2. The control registers are identical and are shown in Figure 4.

The overall connections to both comparators are shown in Figure 5. There are eight possible configurations for each comparator, as determined by the control bits in the corresponding CMPn register: CPn, CNn, and OEn. These configurations are shown in Figure 6. The comparators function down to a V_{DD} of 3.0 V.

When each comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 microseconds. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

CMPn Address: ACh for CMP1, ADh for CMP2 Reset Value: 00h

Not Bit Addressable

7	6	5	4	3	2	1	0
—	—	CEn	CPn	CNn	OEn	COn	CMFn

BIT	SYMBOL	FUNCTION
CMPn.7, 6	—	Reserved for future use. Should not be set to 1 by user programs.
CMPn.5	CEn	Comparator enable. When set by software, the corresponding comparator function is enabled. Comparator output is stable 10 microseconds after CEn is first set.
CMPn.4	CPn	Comparator positive input select. When 0, CINnA is selected as the positive comparator input. When 1, CINnB is selected as the positive comparator input.
CMPn.3	CNn	Comparator negative input select. When 0, the comparator reference pin CMPREF is selected as the negative comparator input. When 1, the internal comparator reference V_{ref} is selected as the negative comparator input.
CMPn.2	OEn	Output enable. When 1, the comparator output is connected to the CMPn pin if the comparator is enabled (CEn = 1). This output is asynchronous to the CPU clock.
CMPn.1	COn	Comparator output, synchronized to the CPU clock to allow reading by software. Cleared when the comparator is disabled (CEn = 0).
CMPn.0	CMFn	Comparator interrupt flag. This bit is set by hardware whenever the comparator output COn changes state. This bit will cause a hardware interrupt if enabled and of sufficient priority. Cleared by software and when the comparator is disabled (CEn = 0).

SU01152

Figure 4. Comparator Control Registers (CMP1 and CMP2)

I2CFG Address: C8h Reset Value: 00h

Bit Addressable

7	6	5	4	3	2	1	0
SLAVEN	MASTRQ	CLRTI	TIRUN	—	—	CT1	CT0

BIT	SYMBOL	FUNCTION
I2CFG.7	SLAVEN	Slave Enable. Writing a 1 this bit enables the slave functions of the I^2C subsystem. If SLAVEN and MASTRQ are 0, the I^2C hardware is disabled. This bit is cleared to 0 by reset and by an I^2C time-out.
I2CFG.6	MASTRQ	Master Request. Writing a 1 to this bit requests mastership of the I^2C bus. If a transmission is in progress when this bit is changed from 0 to 1, action is delayed until a stop condition is detected. A start condition is sent and DRDY is set (thus making ATN = 1 and generating an I^2C interrupt). When a master wishes to release mastership status of the I^2C, it writes a 1 to XSTP in I2CON. MASTRQ is cleared by an I^2C time-out.
I2CFG.5	CLRTI	Writing a 1 to this bit clears the Timer I overflow flag. This bit position always reads as a 0.
I2CFG.4	TIRUN	Writing a 1 to this bit lets Timer I run; a zero stops and clears it. Together with SLAVEN, MASTRQ, and MASTER, this bit determines operational modes as shown in Table 1.
I2CFG.2, 3	—	Reserved for future use. Should not be set to 1 by user programs.
I2CFG.1, 0	CT1, CT0	These two bits are programmed as a function of the CPU clock rate, to optimize the MIN HI and LO time of SCL when this device is a master on the I^2C. The time value determined by these bits controls both of these parameters, and also the timing for stop and start conditions.

SU01157

Figure 10. I^2C Configuration Register (I2CFG)

Regarding Software Response Time

Because the P87LPC767 can run at 20 MHz, and because the I^2C interface is optimized for high-speed operation, it is quite likely that an I^2C service routine will sometimes respond to DRDY (which is set at a rising edge of SCL) and write I2DAT before SCL has gone low again. If XDAT were applied directly to SDA, this situation would produce an I^2C protocol violation. The programmer need not worry about this possibility because XDAT is applied to SDA only when SCL is low.

Conversely, a program that includes an I^2C service routine may take a long time to respond to DRDY. Typically, an I^2C routine operates on a flag-polling basis during a message, with interrupts from other peripheral functions enabled. If an interrupt occurs, it will delay the response of the I^2C service routine. The programmer need not worry about this very much either, because the I^2C hardware stretches the SCL low time until the service routine responds. The only constraint on the response is that it must not exceed the Timer I time-out.

Values to be used in the CT1 and CT0 bits are shown in Table 2. To allow the I^2C bus to run at the maximum rate for a particular oscillator frequency, compare the actual oscillator rate to the f_{OSC} max column in the table. The value for CT1 and CT0 is found in the first line of the table where CPU clock max is greater than or equal to the actual frequency.

Table 2 also shows the machine cycle count for various settings of CT1/CT0. This allows calculation of the actual minimum high and low times for SCL as follows:

$$\text{SCL min high/low time (in microseconds)} = \frac{6 * \text{Min Time Count}}{\text{CPU clock (in MHz)}}$$

For instance, at an 8 MHz frequency, with CT1/CT0 set to 1 0, the minimum SCL high and low times will be 5.25 μs.

Table 2 also shows the Timer I timeout period (given in machine cycles) for each CT1/CT0 combination. The timeout period varies because of the way in which minimum SCL high and low times are measured. When the I^2C interface is operating, Timer I is pre-loaded at every SCL transition with a value dependent upon CT1/CT0. The pre-load value is chosen such that a minimum SCL high or low time has elapsed when Timer I reaches a count of 008 (the actual value pre-loaded into Timer I is 8 minus the machine cycle count).

Table 2. Interaction of TIRUN with SLAVEN, MASTRQ, and MASTER

SLAVEN, MASTRQ, MASTER	TIRUN	OPERATING MODE
All 0	0	The I^2C interface is disabled. Timer I is cleared and does not run. This is the state assumed after a reset. If an I^2C application wants to ignore the I^2C at certain times, it should write SLAVEN, MASTRQ, and TIRUN all to zero.
All 0	1	The I^2C interface is disabled.
Any or all 1	0	The I^2C interface is enabled. The 3 low-order bits of Timer I run for min-time generation, but the hi-order bits do not, so that there is no checking for I^2C being “hung.” This configuration can be used for very slow I^2C operation.
Any or all 1	1	The I^2C interface is enabled. Timer I runs during frames on the I^2C, and is cleared by transitions on SCL, and by Start and Stop conditions. This is the normal state for I^2C operation.

Table 3. CT1, CT0 Values

CT1, CT0	Min Time Count (Machine Cycles)	CPU Clock Max (for 100 kHz I^2C)	Timeout Period (Machine Cycles)
1 0	7	8.4 MHz	1023
0 1	6	7.2 MHz	1022
0 0	5	6.0 MHz	1021
1 1	4	4.8 MHz	1020

Interrupts

The P87LPC767 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the P87LPC767’s many interrupt sources. The P87LPC767 supports up to 13 interrupt sources.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts at once.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the IP0, IP0H, IP1, and IP1H registers. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. So, if two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve simultaneous requests of the same priority level.

Table 3 summarizes the interrupt sources, flag bits, vector addresses, enable bits, priority bits, arbitration ranking, and whether each interrupt may wake up the CPU from Power Down mode.

Table 4. Summary of Interrupts

Description	Interrupt Flag Bit(s)	Vector Address	Interrupt Enable Bit(s)	Interrupt Priority	Arbitration Ranking	Power Down Wakeup
External Interrupt 0	IE0	0003h	EX0 (IEN0.0)	IP0H.0, IP0.0	1 (highest)	Yes
Timer 0 Interrupt	TF0	000Bh	ET0 (IEN0.1)	IP0H.1, IP0.1	4	No
External Interrupt 1	IE1	0013h	EX1 (IEN0.2)	IP0H.2, IP0.2	7	Yes
Timer 1 Interrupt	TF1	001Bh	ET1 (IEN0.3)	IP0H.3, IP0.3	10	No
Serial Port Tx and Rx	TI & RI	0023h	ES (IEN0.4)	IP0H.4, IP0.4	12	No
Brownout Detect	BOF	002Bh	EBO (IEN0.5)	IP0H.5, IP0.5	2	Yes
I^2C Interrupt	ATN	0033h	EI2 (IEN1.0)	IP1H.0, IP1.0	5	No
KBI Interrupt	KBF	003Bh	EKB (IEN1.1)	IP1H.1, IP1.1	8	Yes
Comparator 2 interrupt	CMF2	0043h	EC2 (IEN1.2)	IP1H.2, IP1.2	11	Yes
Watchdog Timer	WDOVF	0053h	EWD (IEN0.6)	IP0H.6, IP0.6	3	Yes
A/D Converter	ADCI	005Bh	EAD (IEN1.4)	IP1H.4, IP1.4	6	Yes
Comparator 1 interrupt	CMF1	0063h	EC1 (IEN1.5)	IP1H.5, IP1.5	9	Yes
Timer I	–	0073h	ETI (IEN1.7)	IP1H.7, IP1.7	13 (lowest)	No

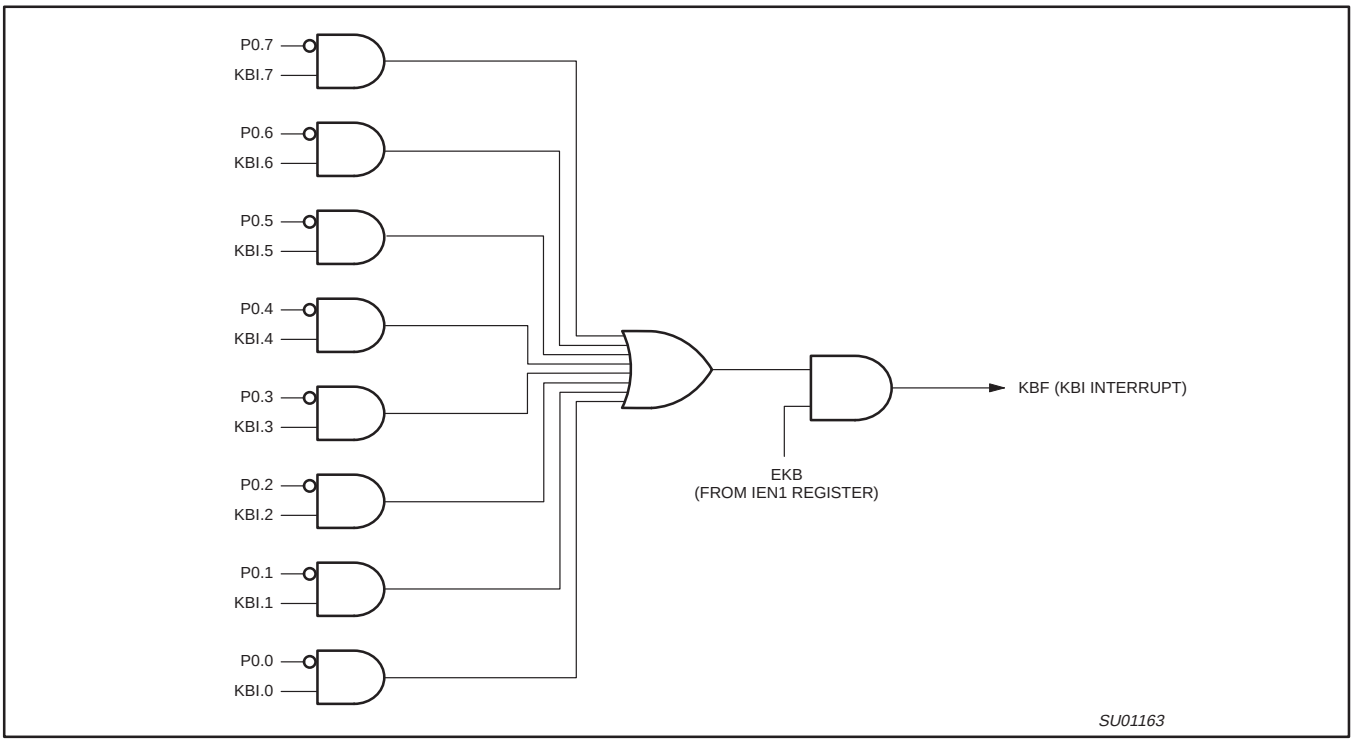


Figure 16. Keyboard Interrupt

KBI Address: 86h Reset Value: 00h

Not Bit Addressable

7	6	5	4	3	2	1	0
KBI.7	KBI.6	KBI.5	KBI.4	KBI.3	KBI.2	KBI.1	KBI.0

BIT	SYMBOL	FUNCTION
KBI.7	KBI.7	When set, enables P0.7 as a cause of a Keyboard Interrupt.
KBI.6	KBI.6	When set, enables P0.6 as a cause of a Keyboard Interrupt.
KBI.5	KBI.5	When set, enables P0.5 as a cause of a Keyboard Interrupt.
KBI.4	KBI.4	When set, enables P0.4 as a cause of a Keyboard Interrupt.
KBI.3	KBI.3	When set, enables P0.3 as a cause of a Keyboard Interrupt.
KBI.2	KBI.2	When set, enables P0.2 as a cause of a Keyboard Interrupt.
KBI.1	KBI.1	When set, enables P0.1 as a cause of a Keyboard Interrupt.
KBI.0	KBI.0	When set, enables P0.0 as a cause of a Keyboard Interrupt.

Note: the Keyboard Interrupt must be enabled in order for the settings of the KBI register to be effective. The interrupt flag (KBF) is located at bit 7 of AUXR1.

SU01164

Figure 17. Keyboard Interrupt Register (KBI)

Oscillator

The P87LPC767 provides several user selectable oscillator options, allowing optimization for a range of needs from high precision to lowest possible cost. These are configured when the EPROM is programmed. Basic oscillator types that are supported include: low, medium, and high speed crystals, covering a range from 20 kHz to 20 MHz; ceramic resonators; and on-chip RC oscillator.

Low Frequency Oscillator Option

This option supports an external crystal in the range of 20 kHz to 100 kHz.

Table 6 shows capacitor values that may be used with a quartz crystal in this mode.

Table 6. Recommended oscillator capacitors for use with the low frequency oscillator option

Oscillator Frequency	V_{DD} = 2.7 to 4.5 V			V_{DD} = 4.5 to 6.0 V		
	Lower Limit	Optimal Value	Upper Limit	Lower Limit	Optimal Value	Upper Limit
20 kHz	15 pF	15 pF	33 pF	33 pF	33 pF	47 pF
32 kHz	15 pF	15 pF	33 pF	33 pF	33 pF	47 pF
100 kHz	15 pF	15 pF	33 pF	15 pF	15 pF	33 pF

Medium Frequency Oscillator Option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

Table 7 shows capacitor values that may be used with a quartz crystal in this mode.

Table 7. Recommended oscillator capacitors for use with the medium frequency oscillator option

Oscillator Frequency	V_{DD} = 2.7 to 4.5 V		
	Lower Limit	Optimal Value	Upper Limit
100 kHz	33 pF	33 pF	47 pF
1 MHz	15 pF	15 pF	33 pF
4 MHz	15 pF	15 pF	33 pF

High Frequency Oscillator Option

This option supports an external crystal in the range of 4 to 20 MHz. Ceramic resonators are also supported in this configuration.

Table 8 shows capacitor values that may be used with a quartz crystal in this mode.

Table 8. Recommended oscillator capacitors for use with the high frequency oscillator option

Oscillator Frequency	V_{DD} = 2.7 to 4.5 V			V_{DD} = 4.5 to 6.0 V		
	Lower Limit	Optimal Value	Upper Limit	Lower Limit	Optimal Value	Upper Limit
4 MHz	15 pF	33 pF	47 pF	15 pF	33 pF	68 pF
8 MHz	15 pF	15 pF	33 pF	15 pF	33 pF	47 pF
16 MHz	–	–	–	15 pF	15 pF	33 pF
20 MHz	–	–	–	15 pF	15 pF	33 pF

On-Chip RC Oscillator Option

The on-chip RC oscillator option has a typical frequency of 6 MHz and can be divided down for slower operation through the use of the DIVM register. Note that the on-chip oscillator has a ±25% frequency tolerance and for that reason may not be suitable for use in some applications. A clock output on the X2/P2.0 pin may be enabled when the on-chip RC oscillator is used.

External Clock Input Option

In this configuration, the processor clock is input from an external source driving the X1/P2.1 pin. The rate may be from 0 Hz up to 20 MHz when V_{DD} is above 4.5 V and up to 10 MHz when V_{DD} is below 4.5 V. When the external clock input mode is used, the X2/P2.0 pin may be used as a standard port pin. A clock output on the X2/P2.0 pin may be enabled when the external clock input is used.

Clock Output

The P87LPC767 supports a clock output function when either the on-chip RC oscillator or external clock input options are selected. This allows external devices to synchronize to the P87LPC767. When enabled, via the ENCLK bit in the P2M1 register, the clock output appears on the X2/CLKOUT pin whenever the on-chip oscillator is running, including in Idle mode. The frequency of the clock output is 1/6 of the CPU clock rate. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power. The clock output may also be enabled when the external clock input option is selected.

Table 9. Sources of Wakeup from Power Down Mode

Wakeup Source	Conditions
External Interrupt 0 or 1	The corresponding interrupt must be enabled.
Keyboard Interrupt	The keyboard interrupt feature must be enabled and properly set up. The corresponding interrupt must be enabled.
Comparator 1 or 2	The comparator(s) must be enabled and properly set up. The corresponding interrupt must be enabled.
Watchdog Timer Reset	The watchdog timer must be enabled via the WDTE bit in the UCFG1 EPROM configuration byte.
Watchdog Timer Interrupt	The WDTE bit in the UCFG1 EPROM configuration byte must not be set. The corresponding interrupt must be enabled.
Brownout Detect Reset	The BOD bit in AUXR1 must not be set (brownout detect not disabled). The BOI bit in AUXR1 must not be set (brownout interrupt disabled).
Brownout Detect Interrupt	The BOD bit in AUXR1 must not be set (brownout detect not disabled). The BOI bit in AUXR1 must be set (brownout interrupt enabled). The corresponding interrupt must be enabled.
Reset Input	The external reset input must be enabled.
A/D converter	Must use internal RC clock (RCCLK = 1) for A/D converter to work in Power Down mode. The A/D must be enabled and properly set up. The corresponding interrupt must be enabled.

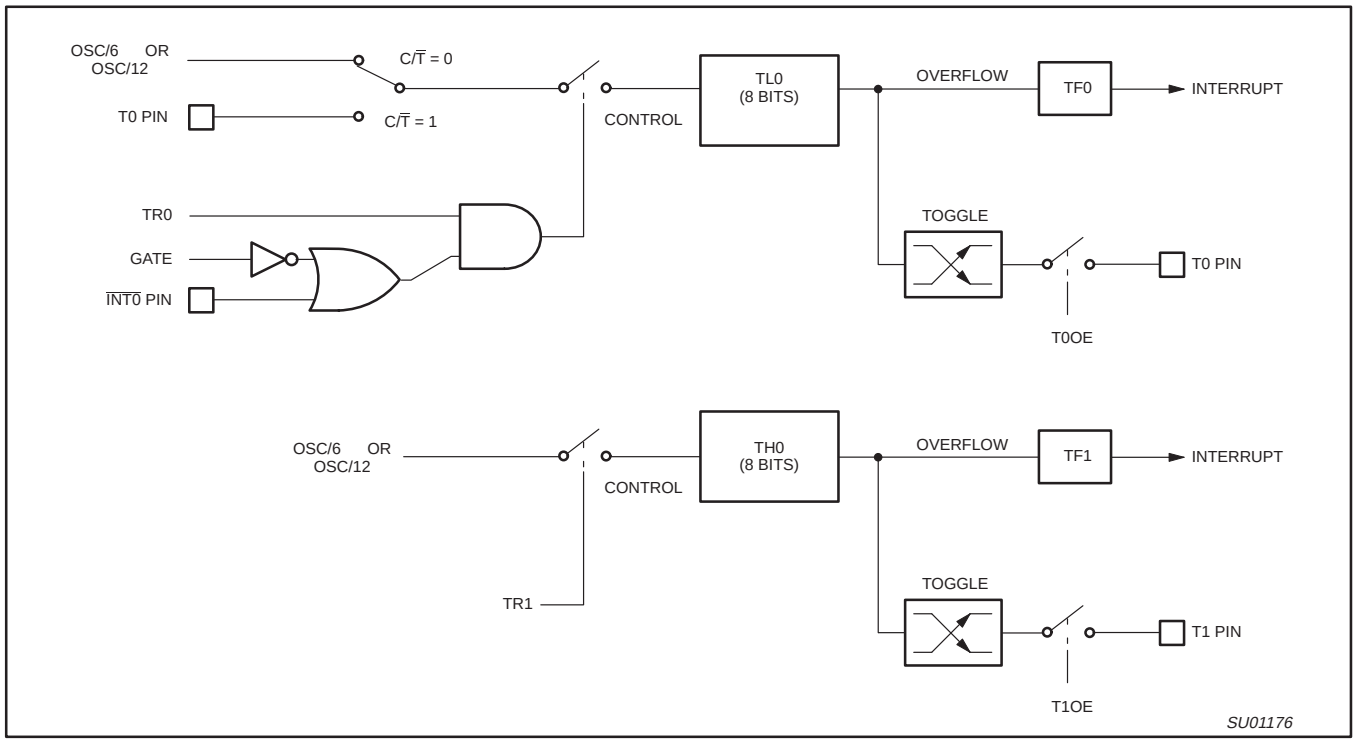


Figure 29. Timer/Counter 0 Mode 3 (Two 8-Bit Counters)

Timer Overflow Toggle Output
Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. This function is enabled by control bits T0OE and T1OE in the P2M1 register, and apply to Timer 0 and Timer 1 respectively. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

UART

The P87LPC767 includes an enhanced 80C51 UART. The baud rate source for the UART is timer 1 for modes 1 and 3, while the rate is fixed in modes 0 and 2. Because CPU clocking is different on the P87LPC767 than on the standard 80C51, baud rate calculation is somewhat different. Enhancements over the standard 80C51 UART include Framing Error detection and automatic address recognition.

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the SBUF register. However, if the first byte still hasn't been read by the time reception of the second byte is complete, the first byte will be lost. The serial port receive and transmit registers are both accessed through Special Function Register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

The serial port can be operated in 4 modes:

Mode 0
Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at 1/6 of the CPU clock frequency.

Mode 1
10 bits are transmitted (through TxD) or received (through RxD): a start bit (logical 0), 8 data bits (LSB first), and a stop bit (logical 1). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate.

Mode 2
11 bits are transmitted (through TxD) or received (through RxD): start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/16 or 1/32 of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

Mode 3
11 bits are transmitted (through TxD) or received (through RxD): a start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

Baud Rates

The baud rate in Mode 0 is fixed: Mode 0 Baud Rate = CPU clock/6. The baud rate in Mode 2 depends on the value of bit SMOD1 in Special Function Register PCON. If SMOD1 = 0 (which is the value on reset), the baud rate is 1/32 of the CPU clock frequency. If SMOD1 = 1, the baud rate is 1/16 of the CPU clock frequency.

$$\text{Mode 2 Baud Rate} = \frac{1 + \text{SMOD1}}{32} \times \text{CPU clock frequency}$$

Using Timer 1 to Generate Baud Rates

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD1. The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either “timer” or “counter” operation, and in any of its 3 running modes. In the most typical applications, it is configured for “timer” operation, in the auto-reload mode (high nibble of TMOD = 0010b). In that case the baud rate is given by the formula:

$$\text{Mode 1, 3 Baud Rate} = \frac{\text{CPU clock frequency}/\text{192 (or 96 if SMOD1 = 1)}}{256 - \text{(TH1)}}$$

Tables 6 and 7 list various commonly used baud rates and how they can be obtained using Timer 1 as the baud rate generator.

Table 10. Baud Rates, Timer Values, and CPU Clock Frequencies for SMOD1 = 0

Timer Count	Baud Rate					
	2400	4800	9600	19.2k	38.4k	57.6k
–1	0.4608	0.9216	* 1.8432	* 3.6864	* 7.3728	* 11.0592
–2	0.9216	1.8432	* 3.6864	* 7.3728	* 14.7456	
–3	1.3824	2.7648	5.5296	* 11.0592	–	–
–4	* 1.8432	* 3.6864	* 7.3728	* 14.7456	–	–
–5	2.3040	4.6080	9.2160	* 18.4320	–	–
–6	2.7648	5.5296	* 11.0592	–	–	–
–7	3.2256	6.4512	12.9024	–	–	–
–8	* 3.6864	* 7.3728	* 14.7456	–	–	–
–9	4.1472	8.2944	16.5888	–	–	–
–10	4.6080	9.2160	* 18.4320	–	–	–

More About UART Mode 0

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/6 the CPU clock frequency. Figure 31 shows a simplified functional diagram of the serial port in Mode 0, and associated timing.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal at S6P2 also loads a 1 into the 9th position of the transmit shift register and tells the TX Control block to commence a transmission. The internal timing is such that one full machine cycle will elapse between “write to SBUF” and activation of SEND.

SEND enables the output of the shift register to the alternate output function line of P1.1 and also enable SHIFT CLOCK to the alternate output function line of P1.0. SHIFT CLOCK is low during S3, S4, and S5 of every machine cycle, and high during S6, S1, and S2. At S6P2 of every machine cycle in which SEND is active, the contents of the transmit shift are shifted to the right one position.

As data bits shift out to the right, zeros come in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position, is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control block to do one last shift and then deactivate SEND and set T1. Both of these actions occur at S1P1 of the 10th machine cycle after “write to SBUF.” Reception is initiated by the condition REN = 1 and R1 = 0. At S6P2 of the next machine cycle, the RX Control unit writes the bits 11111110 t o the receive shift register, and in the next clock phase activates RECEIVE.

RECEIVE enable SHIFT CLOCK to the alternate output function line of P1.0. SHIFT CLOCK makes transitions at S3P1 and S6P1 of every machine cycle. At S6P2 of every machine cycle in which RECEIVE is active, the contents of the receive shift register are shifted to the left one position. The value that comes in from the right is the value that was sampled at the P1.1 pin at S5P2 of the same machine cycle.

As data bits come in from the right, 1s shift out to the left. When the 0 that was initially loaded into the rightmost position arrives at the leftmost position in the shift register, it flags the RX Control block to do one last shift and load SBUF. At S1P1 of the 10th machine cycle after the write to SCON that cleared RI, RECEIVE is cleared as RI is set.

More About UART Mode 1

Ten bits are transmitted (through TxD), or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in SCON. In the P87LPC767 the baud rate is determined by the Timer 1 overflow rate. Figure 32 shows a simplified functional diagram of the serial port in Mode 1, and associated timings for transmit receive.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads a 1 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission actually commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SBUF” signal.)

The transmission begins with activation of SEND which puts the start bit at TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that.

As data bits shift out to the right, zeros are clocked in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 10th divide-by-16 rollover after “write to SBUF.”

Reception is initiated by a detected 1-to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written into the input shift register. Resetting the divide-by-16 counter aligns its rollovers with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RxD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in mode 1 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated.: 1. R1 = 0, and 2. Either SM2 = 0, or the received stop bit = 1.

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated. At this time, whether the above conditions are met or not, the unit goes back to looking for a 1-to-0 transition in RxD.

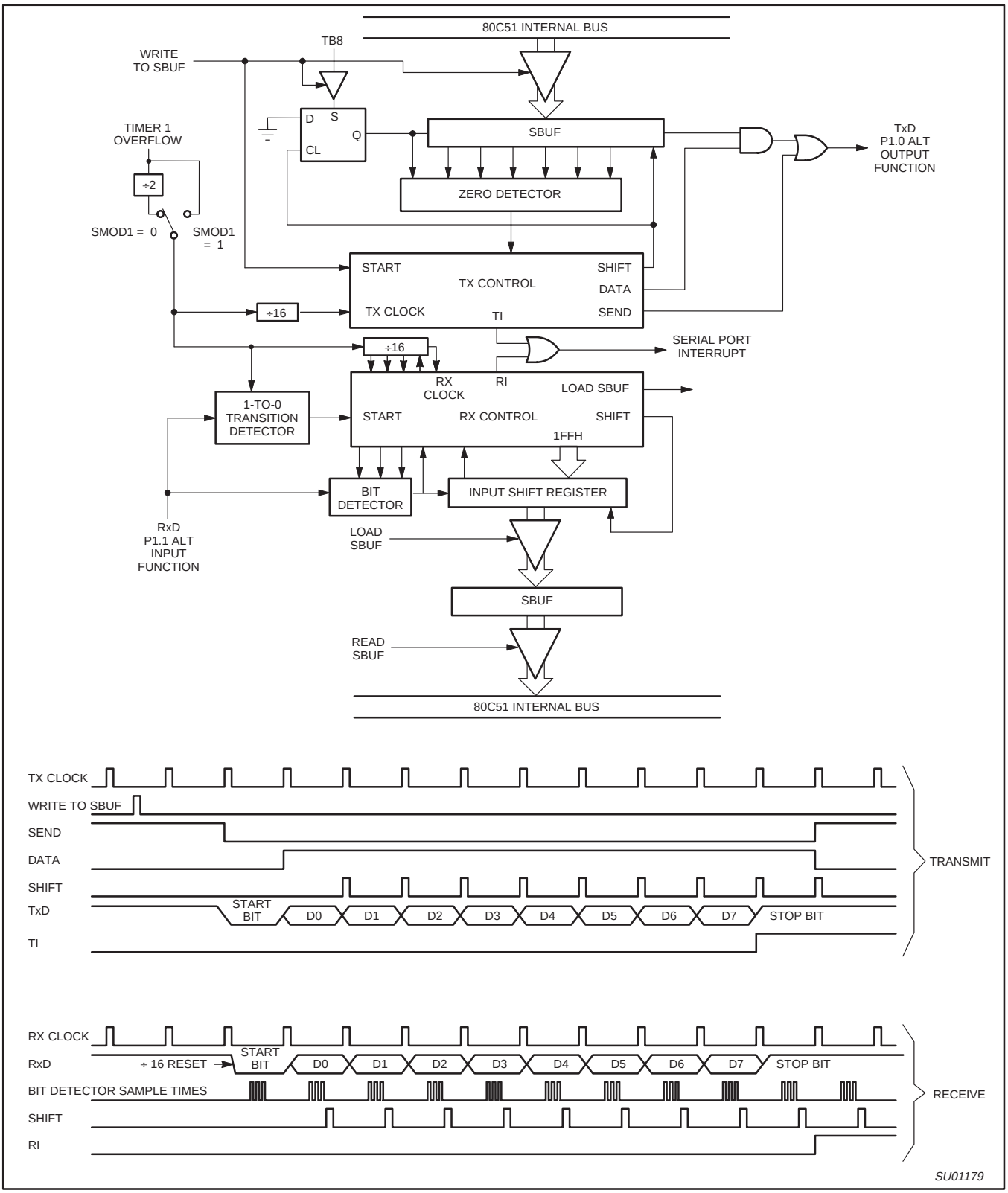


Figure 32. Serial Port Mode 1

More About UART Modes 2 and 3

Eleven bits are transmitted (through TxD), or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8) can be assigned the value of 0 or 1. On receive, the 9the data bit goes into RB8 in SCON. The baud rate is programmable to either 1/16 or 1/32 of the CPU clock frequency in Mode 2. Mode 3 may have a variable baud rate generated from Timer 1.

Figures 33 and 34 show a functional diagram of the serial port in Modes 2 and 3. The receive portion is exactly the same as in Mode 1. The transmit portion differs from Mode 1 only in the 9th bit of the transmit shift register.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads TB8 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SBUF” signal.)

The transmission begins with activation of SEND, which puts the start bit at TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that. The first shift clocks a 1 (the stop bit) into the 9th bit position of the shift register. Thereafter, only zeros are clocked in. Thus, as data bits shift out to the right, zeros are clocked in from the left. When TB8 is at the output position of the shift register, then the stop bit is just to the left of TB8, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 11th divide-by-16 rollover after “write to SBUF.”

Reception is initiated by a detected 1-to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written to the input shift register.

At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of R–D. The value accepted is the value that was seen in at least 2 of the 3 samples. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in Modes 2 and 3 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI.

The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated. 1. RI = 0, and 2. Either SM2 = 0, or the received 9th data bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits go into SBUF. One bit time later, whether the above conditions were met or not, the unit goes back to looking for a 1-to-0 transition at the RxD input.

Multiprocessor Communications

UART modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received or transmitted. When data is received, the 9th bit is stored in RB8. The UART can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. One way to use this feature in multiprocessor systems is as follows:

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that follow. The slaves that weren’t being addressed leave their SM2 bits set and go on about their business, ignoring the subsequent data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit, although this is better done with the Framing Error flag. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

UCFG2 Address: FD01h Unprogrammed Value: FFh

7	6	5	4	3	2	1	0
SB2	SB1	—	—	—	—	—	—

BIT	SYMBOL	FUNCTION
UCFG2.7, 6	SB2, SB1	EPROM security bits. See table entitled, “EPROM Security Bits” for details.
UCFG2.5–0	—	Reserved for future use.

SU01186

Figure 39. EPROM System Configuration Byte 2 (UCFG2)

Security Bits
When neither of the security bits are programmed, the code in the EPROM can be verified. When only security bit 1 is programmed, all further programming of the EPROM is disabled. At that point, only security bit 2 may still be programmed. When both security bits are programmed, EPROM verify is also disabled.

Table 12. EPROM Security Bits

SB2	SB1	Protection Description
1	1	Both security bits unprogrammed. No program security features enabled. EPROM is programmable and verifiable.
1	0	Only security bit 1 programmed. Further EPROM programming is disabled. Security bit 2 may still be programmed.
0	1	Only security bit 2 programmed. This combination is not supported.
0	0	Both security bits programmed. All EPROM verification and programming are disabled.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Operating temperature under bias	–55 to +125	°C
Storage temperature range	–65 to +150	°C
Voltage on $\overline{RST}/V_{PP}$ pin to V_{SS}	0 to +11.0	V
Voltage on any other pin to V_{SS}	–0.5 to V_{DD}+0.5 V	V
Maximum I_{OL} per I/O pin	20	mA
Power dissipation (based on package heat transfer, not device power consumption)	1.5	W

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification are not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 2.7 V to 6.0 V unless otherwise specified; T_{amb} = 0 °C to +70 °C, –40 °C to +85 °C, or –40 °C to +125 °C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1,2]	MAX	
I_{DD}	Power supply current, operating	5.0 V, 20 MHz[11]		15	25	mA
		3.0 V, 10 MHz[11]		4	7	mA
I_{ID}	Power supply current, Idle mode	5.0 V, 20 MHz[11]		6	10	mA
		3.0 V, 10 MHz[11]		2	4	mA
I_{PD}	Power supply current, Power Down mode	5.0 V[11]		1	10	µA
		3.0 V[11]		1	5	µA
V_{RAM}	RAM keep-alive voltage		1.5			V
V_{IL}	Input low voltage (TTL input)	4.0 V < V_{DD} < 6.0 V	–0.5		0.2 V_{DD}–0.1	V
		2.7 V < V_{DD} < 4.0 V	–0.5		0.7	V
V_{IL1}	Negative going threshold (Schmitt input)		–0.5 V_{DD}	0.4 V_{DD}	0.3 V_{DD}	V
V_{IH}	Input high voltage (TTL input)		0.2 V_{DD}+0.9		V_{DD}+0.5	V
V_{IH1}	Positive going threshold (Schmitt input)		0.7 V_{DD}	0.6 V_{DD}	V_{DD}+0.5	V
HYS	Hysteresis voltage			0.2 V_{DD}		V
V_{OL}	Output low voltage all ports[5, 9]	I_{OL} = 3.2 mA, V_{DD} = 2.7 V			0.4	V
V_{OL1}	Output low voltage all ports[5, 9]	I_{OL} = 20 mA, V_{DD} = 2.7 V			1.0	V
V_{OH}	Output high voltage, all ports[3]	I_{OH} = –20 µA, V_{DD} = 2.7 V	V_{DD}–0.7			V
		I_{OH} = –30 µA, V_{DD} = 4.5 V	V_{DD}–0.7			V
V_{OH1}	Output high voltage, all ports[4]	I_{OH} = –1.0 mA, V_{DD} = 2.7 V	V_{DD}–0.7			V
C_{IO}	Input/Output pin capacitance[10]				15	pF
I_{IL}	Logical 0 input current, all ports[8]	V_{IN} = 0.4 V			–50	µA
I_{LI}	Input leakage current, all ports[7]	V_{IN} = V_{IL} or V_{IH}			±2	µA
I_{TL}	Logical 1 to 0 transition current, all ports[3, 6]	V_{IN} = 1.5 V at V_{DD} = 3.0 V	–30		–250	µA
		V_{IN} = 2.0 V at V_{DD} = 5.5 V	–150		–650	µA
R_{RST}	Internal reset pull-up resistor		40		225	kΩ
$V_{BO2.5}$	Brownout trip voltage with BOV = 1[12]	T_{amb} = 0 °C to +70 °C	2.45	2.5	2.65	V
$V_{BO3.8}$	Brownout trip voltage with BOV = 0		3.45	3.8	3.90	V
V_{REF}	Reference voltage		1.11	1.26	1.41	V

NOTES:

1. Typical ratings are not guaranteed. The values listed are at room temperature, 5 V.
2. See other Figures for details.
3. Ports in quasi-bidirectional mode with weak pull-up (applies to all port pins with pull-ups). Does not apply to open drain pins.
4. Ports in PUSH-PULL mode. Does not apply to open drain pins.
5. In all output modes except high impedance mode.
6. Port pins source a transition current when used in quasi-bidirectional mode and externally driven from 1 to 0. This current is highest when V_{IN} is approximately 2 V.
7. Measured with port in high impedance mode. Parameter is guaranteed but not tested at cold temperature.
8. Measured with port in quasi-bidirectional mode.
9. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 20 mA
   Maximum total I_{OL} for all outputs: 80 mA
   Maximum total I_{OH} for all outputs: 5 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
10. Pin capacitance is characterized but not tested.
11. The I_{DD}, I_{ID}, and I_{PD} specifications are measured using an external clock with the following functions disabled: comparators, brownout detect, and watchdog timer. For V_{DD} = 3 V, LPEP = 1. Refer to the appropriate figures on the following pages for additional current drawn by each of these functions and detailed graphs for other frequency and voltage combinations.
12. Devices initially operating at V_{DD} = 2.7 V or above and at f_{OSC} = 10 MHz or less are guaranteed to continue to execute instructions correctly at the brownout trip point. Initial power-on operation below V_{DD} = 2.7 V is not guaranteed.

COMPARATOR ELECTRICAL CHARACTERISTICS

V_{DD} = 3.0 V to 6.0 V unless otherwise specified; T_{amb} = 0 °C to +70 °C, –40 °C to +85 °C, or –40 °C to +125 °C, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{IO}	Offset voltage comparator inputs[1]				±10	mV
V_{CR}	Common mode range comparator inputs		0		V_{DD}–0.3	V
CMRR	Common mode rejection ratio[1]				–50	dB
	Response time			250	500	ns
	Comparator enable to output valid				10	µs
I_{IL}	Input leakage current, comparator	$0 < V_{IN} < V_{DD}$			±10	µA

NOTE:
1. This parameter is guaranteed by characterization, but not tested in production.

A/D CONVERTER DC ELECTRICAL CHARACTERISTICS

Vdd = 3.0 V to 6.0 V unless otherwise specified;
Tamb = 0 to +70 °C for commercial, -40 °C to +85 °C for industrial, or –40 °C to +125 °C for extended industrial, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
AV_{IN}	Analog input voltage		V_{SS} - 0.2	V_{DD} + 0.2	V
R_{REF}	Resistance between V_{DD} and V_{SS}	A/D enabled	tbd	tbd	kΩ
C_{IA}	Analog input capacitance			15	pF
DL_e	Differential non-linearity[1,2,3]			±1	LSB
IL_e	Integral non-linearity[1,4]			±1	LSB
OS_e	Offset error[1,5]			±1	LSB
G_e	Gain error[1,6]			±1	%
A_e	Absolute voltage error[1,7]			±1	LSB
M_{CTC}	Channel-to-channel matching			±1	LSB
C_t	Crosstalk between inputs of port[8]	0 to 100 kHz		-60	dB
-	Input slew rate			100	V/ms
-	Input source impedance			10	kΩ

NOTES:
1. Conditions: V_{SS} = 0 V; V_{DD} = 5.12 V.
2. The A/D is monotonic, there are no missing codes
3. The differential non-linearity (DL_e) is the difference between the actual step width and the ideal step width. See Figure 40.
4. The integral non-linearity (IL_e) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 40.
5. The offset error (OS_e) is the absolute difference between the straight line which fits the actual transfer curve (after removing gain error), and the straight line which fits the ideal transfer curve. See Figure 40.
6. The gain error (G_e) is the relative difference in percent between the straight line fitting the actual transfer curve (after removing offset error), and the straight line which fits the ideal transfer curve. Gain error is constant at every point on the transfer curve. See Figure 40.
7. The absolute voltage error (A_e) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve.
8. This should be considered when both analog and digital signals are input simultaneously to A/D pins.
9. Changing the input voltage faster than this may cause erroneous readings.
10. A source impedance higher than this driving an A/D input may result in loss of precision and erroneous readings.

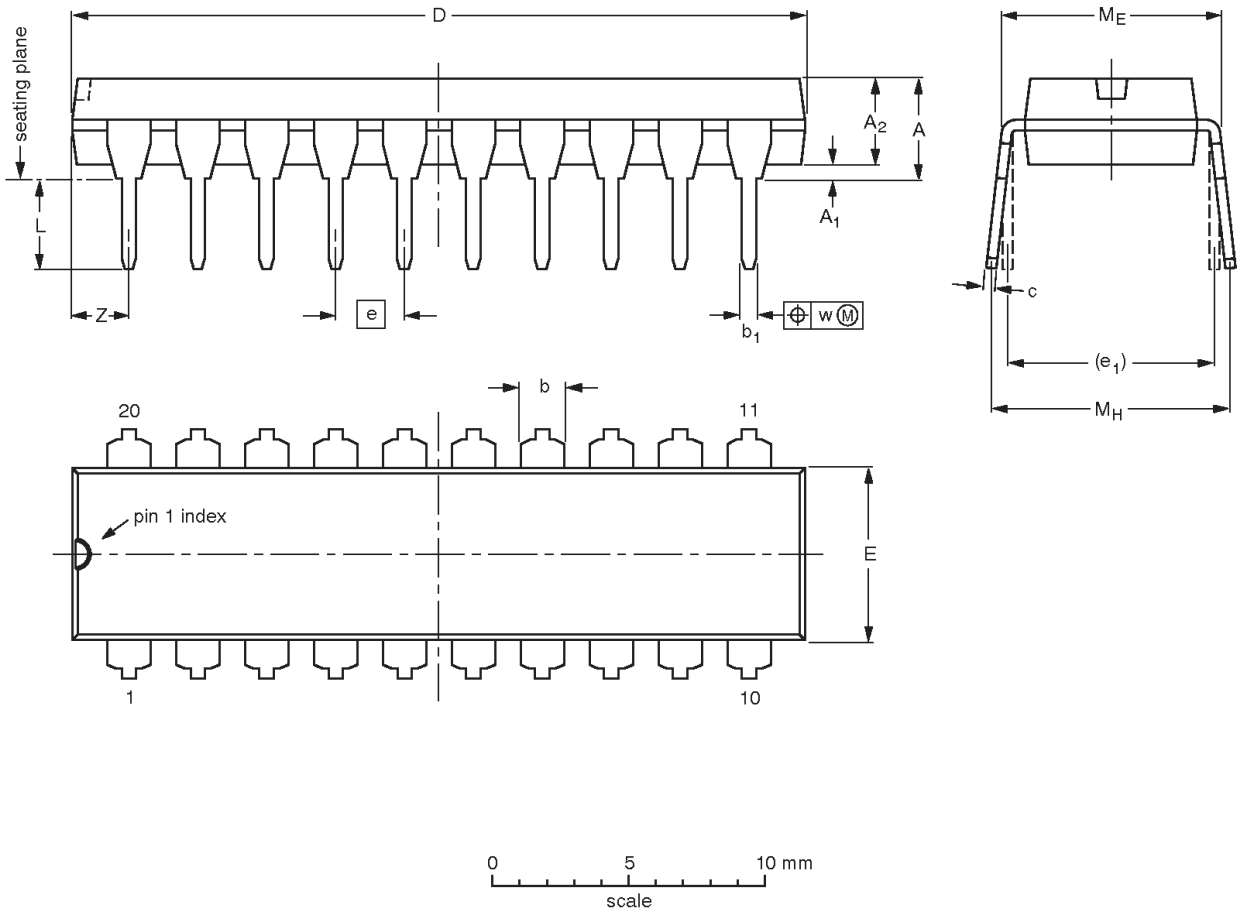
AC ELECTRICAL CHARACTERISTICS

T_{amb} = 0 °C to +70 °C, –40 °C to +85 °C, or –40 °C to +125 °C; V_{DD} = 2.7 V to 6.0 V unless otherwise specified, V_{SS} = 0 V[1, 2, 3]

SYMBOL	FIGURE	PARAMETER	LIMITS		UNIT
			MIN	MAX	
External Clock					
f_C	42	Oscillator frequency (V_{DD} = 4.5 V to 6.0 V)	0	20	MHz
f_C	42	Oscillator frequency (V_{DD} = 2.7 V to 6.0 V)	0	10	MHz
t_C	42	Clock period and CPU timing cycle	$1/f_C$		ns
t_{CHCX}	42	Clock high-time[4]	20		ns
t_{CLCX}	42	Clock low time[4]	20		ns
Shift Register					
t_{XLXL}	41	Serial port clock cycle time	$6t_C$		ns
t_{QVXH}	41	Output data setup to clock rising edge	$5t_C$ – 133		ns
t_{XHQX}	41	Output data hold after clock rising edge	$1t_C$ – 80		ns
t_{XHDV}	41	Input data setup to clock rising edge		$5t_C$ – 133	ns
t_{XHDX}	41	Input data hold after clock rising edge	0		ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for all outputs = 80 pF.
3. Parts are guaranteed to operate down to 0 Hz.
4. Applies only to an external clock source, not when a crystal is connected to the X1 and X2 pins.

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1		MS-001	SC-603			~~95-05-24~~ 99-12-27