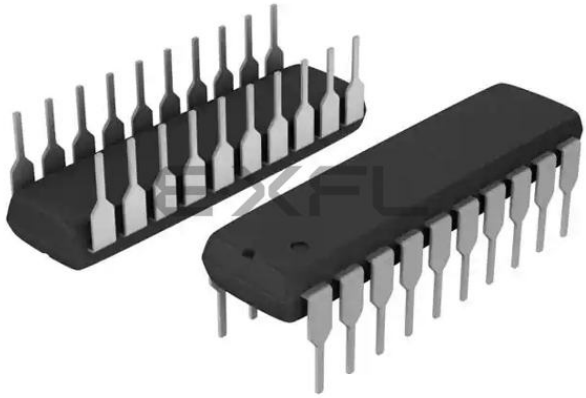

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-DIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p87lpc767bn-112

Low power, low price, low pin count (20 pin) microcontroller with 4-kbyte OTP and 8-bit A/D converter

P87LPC767

GENERAL DESCRIPTION

The P87LPC767 is a 20-pin single-chip microcontroller designed for low pin count applications demanding high-integration, low cost solutions over a wide range of performance requirements. A member of the Philips low pin count family, the P87LPC767 offers programmable oscillator configurations for high and low speed crystals or RC operation, wide operating voltage range, programmable port output configurations, selectable Schmitt trigger inputs, LED drive outputs, and a built-in watchdog timer. The P87LPC767 is based on an accelerated 80C51 processor architecture that executes instructions at twice the rate of standard 80C51 devices.

FEATURES

- An accelerated 80C51 CPU provides instruction cycle times of 300–600 ns for all instructions except multiply and divide when executing at 20 MHz. Execution at up to 20 MHz when V_{DD} = 4.5 V to 6.0 V, 10 MHz when V_{DD} = 2.7 V to 6.0 V.
- Four-channel multiplexed 8-bit A/D converter. Conversion time of 9.3 μS at f_{OSC} = 20 MHz.
- 2.7 V to 6.0 V operating range for digital functions.
- 4 K bytes EPROM code memory.
- 128 byte RAM data memory.
- 32-byte customer code EPROM allows serialization of devices, storage of setup parameters, etc.
- Two 16-bit counter/timers. Each timer may be configured to toggle a port output upon timer overflow.
- Two analog comparators.
- Full duplex UART.
- I^2C communication port.
- Eight keypad interrupt inputs, plus two additional external interrupt inputs.
- Four interrupt priority levels.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog timeout time is selectable from 8 values.
- Active low reset. On-chip power-on reset allows operation with no external reset components.
- Low voltage reset. One of two preset low voltage levels may be selected to allow a graceful system shutdown when power fails. May optionally be configured as an interrupt.
- Oscillator Fail Detect. The watchdog timer has a separate fully on-chip oscillator, allowing it to perform an oscillator fail detect function.
- Configurable on-chip oscillator with frequency range and RC oscillator options (selected by user programmed EPROM bits). The RC oscillator option allows operation with no external oscillator components.
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.
- Selectable Schmitt trigger port inputs.
- LED drive capability (20 mA) on all port pins.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- 15 I/O pins minimum. Up to 18 I/O pins using on-chip oscillator and reset options.
- Only power and ground connections are required to operate the P87LPC767 when fully on-chip oscillator and reset options are selected.
- Serial EPROM programming allows simple in-circuit production coding. Two EPROM security bits prevent reading of sensitive application programs.
- Idle and Power Down reduced power modes. Improved wakeup from Power Down mode (a low interrupt input starts execution). Typical Power Down current is 1 μA.
- 20-pin DIP and SO packages.

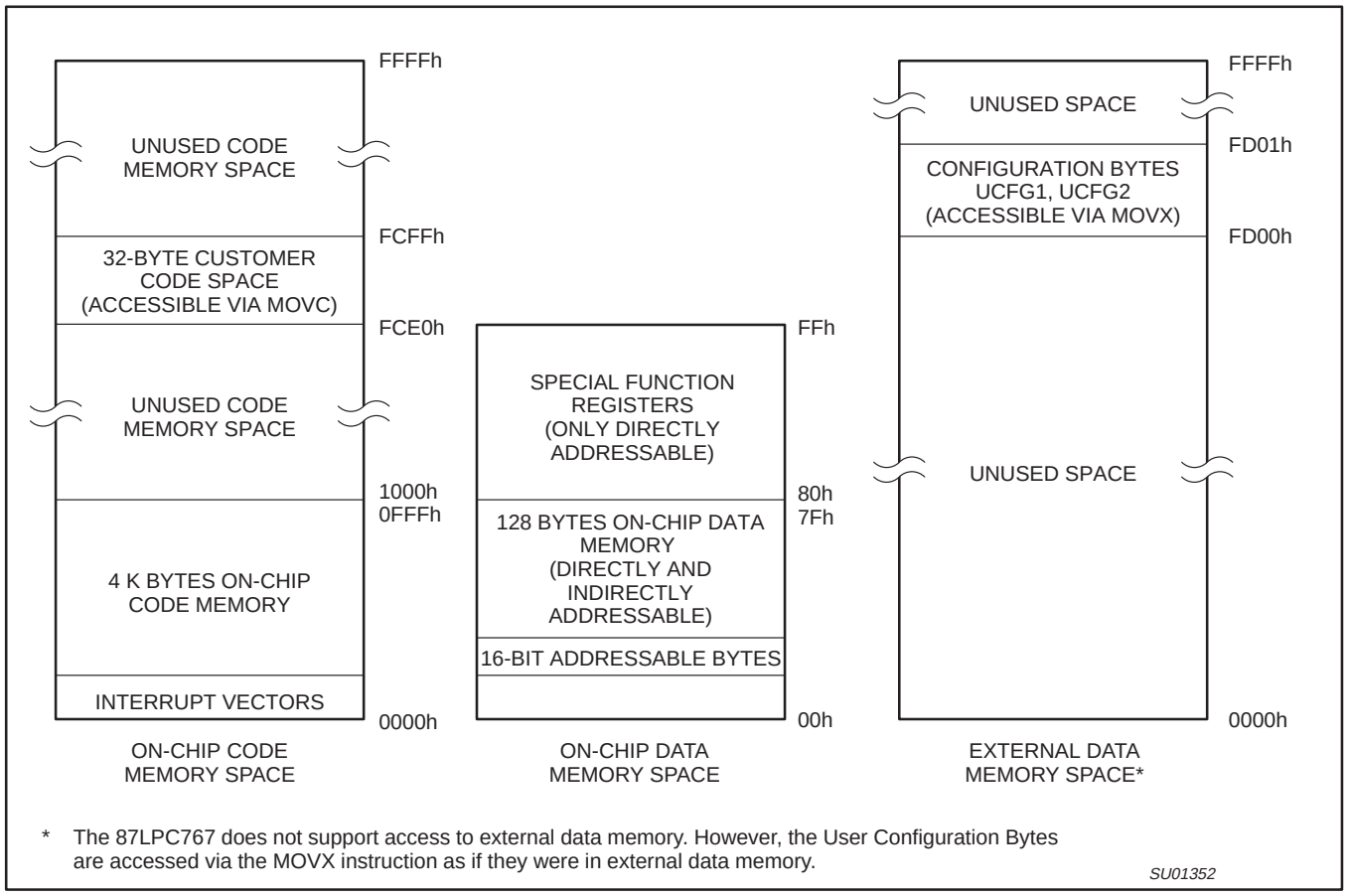


Figure 1. P87LPC767 Program and Data Memory Map

Code Examples for the A/D

The first piece of sample code shows an example of port configuration for use with the A/D. This example sets up the pins so that all four A/D channels may be used. Port configuration for analog functions is described in the section Analog Functions.

```
; Set up port pins for A/D conversion, without affecting other pins.
   mov    PT0AD,#78h          ; Disable digital inputs on A/D input pins.
   anl    P0M2,#87h           ; Disable digital outputs on A/D input pins.
   orl    P0M1,#78h           ; Disable digital outputs on A/D input pins.
```

Following is an example of using the A/D with interrupts. The routine ADStart begins an A/D conversion using the A/D channel number supplied in the accumulator. The channel number is not checked for validity. The A/D must previously have been enabled with sufficient time to allow for stabilization.

The interrupt handler routine reads the conversion value and returns it in memory address ADResult. The interrupt should be enabled prior to starting the conversion.

```
; Start A/D conversion.
ADStart:
   orl    ADCON,A             ; Add in the new channel number.
   setb   ADCS                ; Start an A/D conversion.
;  orl    PCON,#01h           ; The CPU could be put into Idle mode here.
;  orl    PCON,#02h           ; The CPU could be put into Power Down mode here if RCCLK = 1.
   ret

; A/D interrupt handler.
ADInt:
   push   ACC                 ; Save accumulator.
   mov    A,DAC0              ; Get A/D result,
   mov    ADResult,A          ;   and save it in memory.
   clr    ADCI                ; Clear the A/D completion flag.
   anl    ADCON,#0fch         ; Clear the A/D channel number.
   pop    ACC                 ; Restore accumulator.
   reti
```

Following is an example of using the A/D with polling. An A/D conversion is started using the channel number supplied in the accumulator. The channel number is not checked for validity. The A/D must previously have been enabled with sufficient time to allow for stabilization. The conversion result is returned in the accumulator.

```
ADRead:
   orl    ADCON,A             ; Add in the new channel number.
   setb   ADCS                ; Start A/D conversion.
ADChk:
   jnb    ADCI,ADChk          ; Wait for ADCI to be set.
   mov    A,DAC0              ; Get A/D result.
   clr    ADCI                ; Clear the A/D completion flag.
   anl    ADCON,#0fch         ; Clear the A/D channel number.
   ret
```

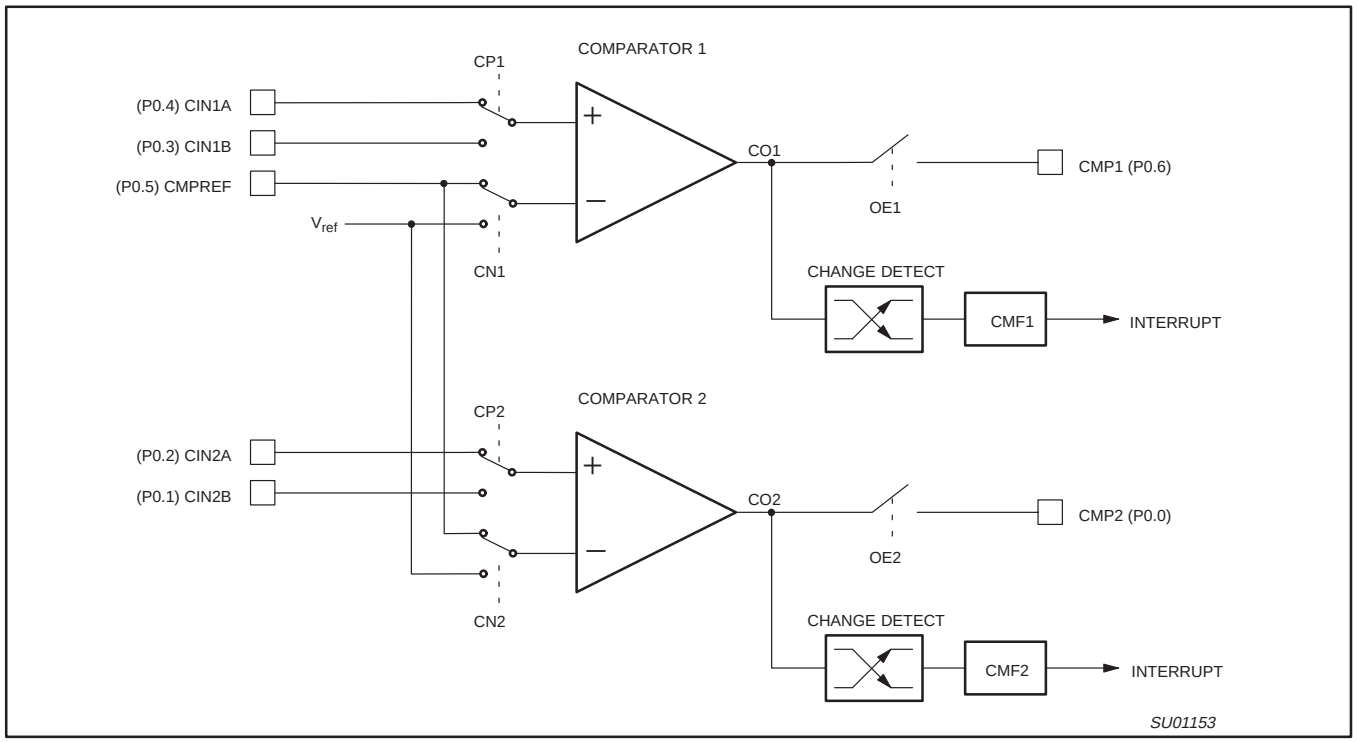


Figure 5. Comparator Input and Output Connections

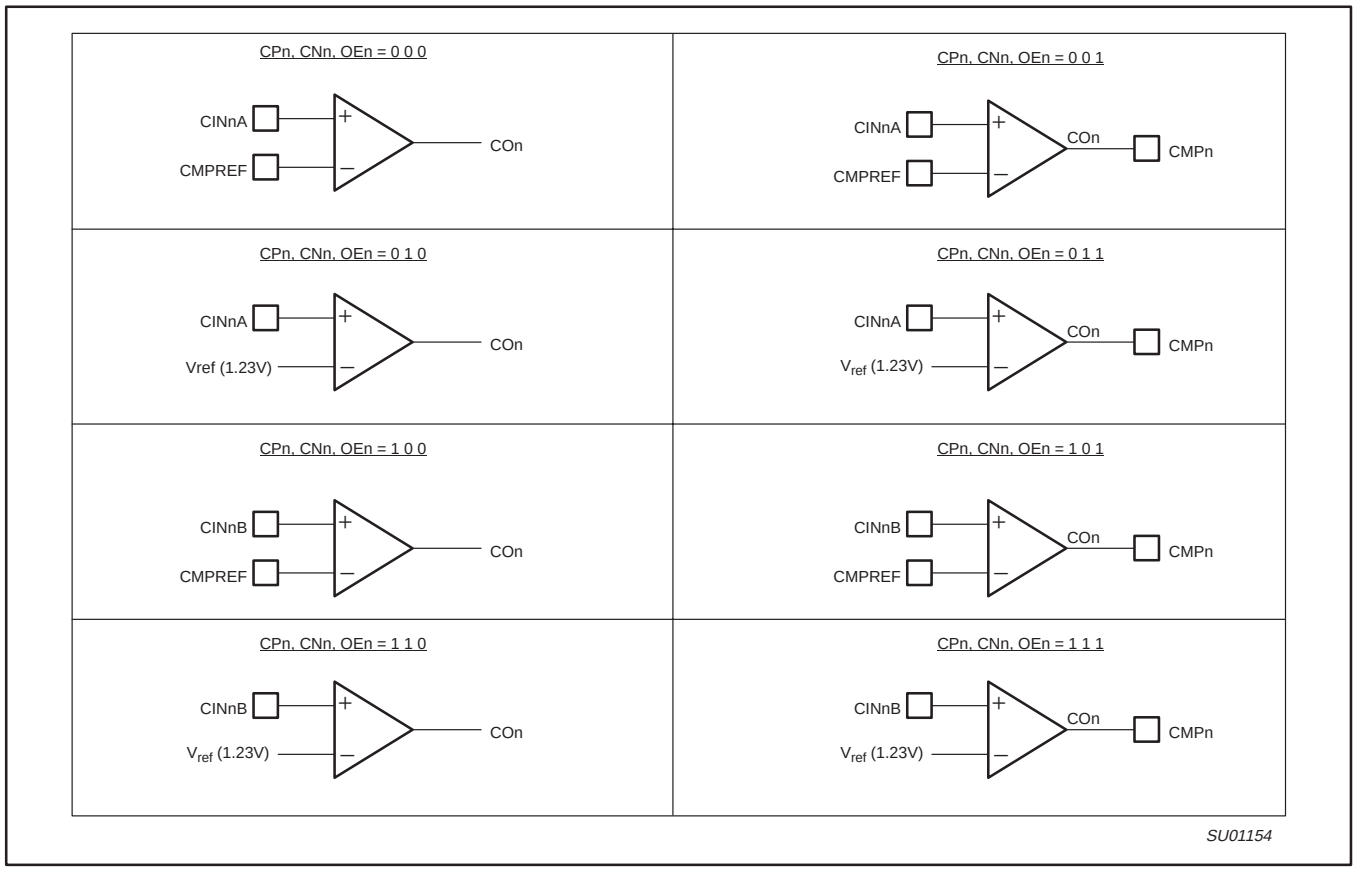


Figure 6. Comparator Configurations

ARL "Arbitration Loss" is 1 when transmit Active was set, but this device lost arbitration to another transmitter. Transmit Active is cleared when ARL is 1. There are four separate cases in which ARL is set.

1. If the program sent a 1 or repeated start, but another device sent a 0, or a stop, so that SDA is 0 at the rising edge of SCL. (If the other device sent a stop, the setting of ARL will be followed shortly by STP being set.)

2. If the program sent a 1, but another device sent a repeated start, and it drove SDA low before SCL could be driven low. (This type of ARL is always accompanied by STR = 1.)

3. In master mode, if the program sent a repeated start, but another device sent a 1, and it drove SCL low before this device could drive SDA low.

4. In master mode, if the program sent stop, but it could not be sent because another device sent a 0.

STR "STaRt" is set to a 1 when an I^2C start condition is detected at a non-idle slave or at a master. (STR is not set when an idle slave becomes active due to a start bit; the slave has nothing useful to do until the rising edge of SCL sets DRDY.)

STP "SToP" is set to 1 when an I^2C stop condition is detected at a non-idle slave or at a master. (STP is not set for a stop condition at an idle slave.)

MASTER "MASTER" is 1 if this device is currently a master on the I^2C. MASTER is set when MASTRQ is 1 and the bus is not busy (i.e., if a start bit hasn't been received since reset or a "Timer I" time-out, or if a stop has been received since the last start). MASTER is cleared when ARL is set, or after the software writes MASTRQ = 0 and then XSTP = 1.

Writing I2CON

Typically, for each bit in an I^2C message, a service routine waits for ATN = 1. Based on DRDY, ARL, STR, and STP, and on the current bit position in the message, it may then write I2CON with one or more of the following bits, or it may read or write the I2DAT register.

CXA Writing a 1 to "Clear Xmit Active" clears the Transmit Active state. (Reading the I2DAT register also does this.)

Regarding Transmit Active

Transmit Active is set by writing the I2DAT register, or by writing I2CON with XSTR = 1 or XSTP = 1. The I^2C interface will only drive the SDA line low when Transmit Active is set, and the ARL bit will only be set to 1 when Transmit Active is set. Transmit Active is cleared by reading the I2DAT register, or by writing I2CON with CXA = 1. Transmit Active is automatically cleared when ARL is 1.

IDLE Writing 1 to "IDLE" causes a slave's I^2C hardware to ignore the I^2C until the next start condition (but if MASTRQ is 1, then a stop condition will cause this device to become a master).

CDR Writing a 1 to "Clear Data Ready" clears DRDY. (Reading or writing the I2DAT register also does this.)

CARL Writing a 1 to "Clear Arbitration Loss" clears the ARL bit.

CSTR Writing a 1 to "Clear STaRt" clears the STR bit.

CSTP Writing a 1 to "Clear SToP" clears the STP bit. Note that if one or more of DRDY, ARL, STR, or STP is 1, the low time of SCL is stretched until the service routine responds by clearing them.

XSTR Writing 1s to "Xmit repeated STaRt" and CDR tells the I^2C hardware to send a repeated start condition. This should only be at a master. Note that XSTR need not and should not be used to send an "initial" (non-repeated) start; it is sent automatically by the I^2C hardware. Writing XSTR = 1 includes the effect of writing I2DAT with XDAT = 1; it sets Transmit Active and releases SDA to high during the SCL low time. After SCL goes high, the I^2C hardware waits for the suitable minimum time and then drives SDA low to make the start condition.

XSTP Writing 1s to "Xmit SToP" and CDR tells the I^2C hardware to send a stop condition. This should only be done at a master. If there are no more messages to initiate, the service routine should clear the MASTRQ bit in I2CFG to 0 before writing XSTP with 1. Writing XSTP = 1 includes the effect of writing I2DAT with XDAT = 0; it sets Transmit Active and drives SDA low during the SCL low time. After SCL goes high, the I^2C hardware waits for the suitable minimum time and then releases SDA to high to make the stop condition.

I/O Ports

The P87LPC767 has 3 I/O ports, port 0, port 1, and port 2. The exact number of I/O pins available depend upon the oscillator and reset options chosen. At least 15 pins of the P87LPC767 may be used as I/Os when a two-pin external oscillator and an external reset circuit are used. Up to 18 pins may be available if fully on-chip oscillator and reset configurations are chosen.

All but three I/O port pins on the P87LPC767 may be software configured to one of four types on a bit-by-bit basis, as shown in Table 4. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input only. Two configuration registers for each port choose the output type for each port pin.

Table 5. Port Output Configuration Settings

PxM1.y	PxM2.y	Port Output Mode
0	0	Quasi-bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance)
1	1	Open Drain

Quasi-Bidirectional Output Configuration

The default port output configuration for standard P87LPC767 I/O ports is the quasi-bidirectional output that is common on the 80C51 and most of its derivatives. This output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the pin is pulled low, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

One of these pull-ups, called the “very weak” pull-up, is turned on whenever the port latch for the pin contains a logic 1. The very weak pull-up sources a very small current that will pull the pin high if it is left floating.

A second pull-up, called the “weak” pull-up, is turned on when the port latch for the pin contains a logic 1 and the pin itself is also at a logic 1 level. This pull-up provides the primary source current for a quasi-bidirectional pin that is outputting a 1. If a pin that has a logic 1 on it is pulled low by an external device, the weak pull-up turns off, and only the very weak pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current to overpower the weak pull-up and take the voltage on the port pin below its input threshold.

The third pull-up is referred to as the “strong” pull-up. This pull-up is used to speed up low-to-high transitions on a quasi-bidirectional port pin when the port latch changes from a logic 0 to a logic 1. When this occurs, the strong pull-up turns on for a brief time, two CPU clocks, in order to pull the port pin high quickly. Then it turns off again.

The quasi-bidirectional port configuration is shown in Figure 12.

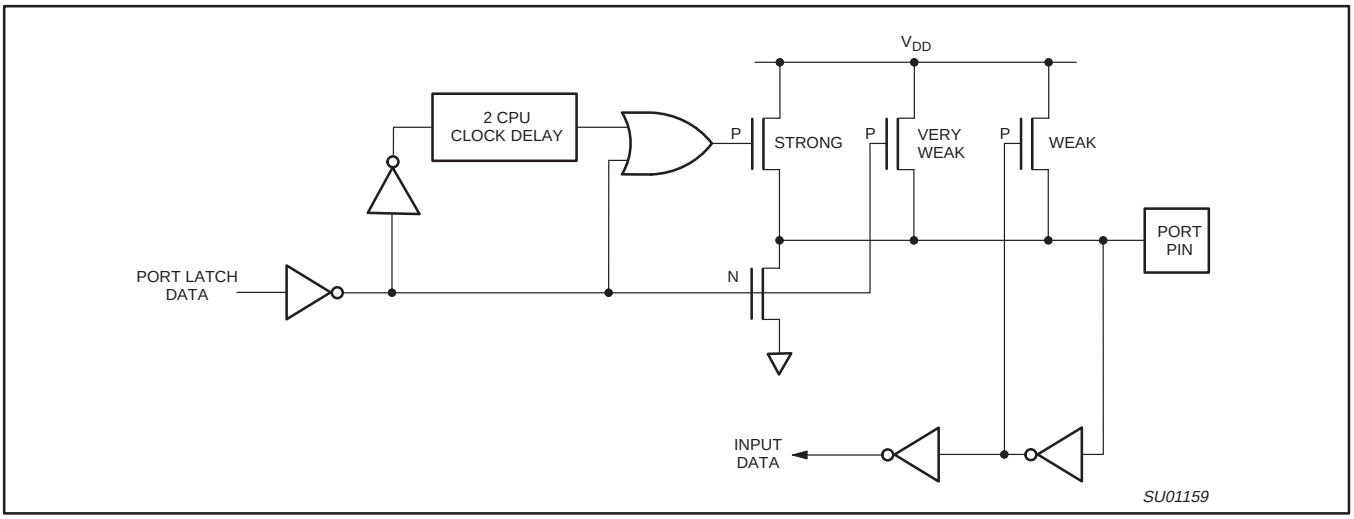


Figure 12. Quasi-Bidirectional Output

Open Drain Output Configuration

The open drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}. The pull-down for this mode is the same as for the quasi-bidirectional mode.

The open drain port configuration is shown in Figure 13.

Push-Pull Output Configuration

The push-pull output configuration has the same pull-down structure as both the open drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output.

The push-pull port configuration is shown in Figure 14.

The three port pins that cannot be configured are P1.2, P1.3, and P1.5. The port pins P1.2 and P1.3 are permanently configured as open drain outputs. They may be used as inputs by writing ones to their respective port latches. P1.5 may be used as a Schmitt trigger input if the P87LPC767 has been configured for an internal reset and is not using the external reset input function $\overline{RST}$.

Additionally, port pins P2.0 and P2.1 are disabled for both input and output if one of the crystal oscillator options is chosen. Those options are described in the Oscillator section.

The value of port pins at reset is determined by the PRHI bit in the UCFG1 register. Ports may be configured to reset high or low as needed for the application. When port pins are driven high at reset, they are in quasi-bidirectional mode and therefore do not source large amounts of current.

Every output on the P87LPC767 may potentially be used as a 20 mA sink LED drive output. However, there is a maximum total output current for all ports which must not be exceeded.

All ports pins of the P87LPC767 have slew rate controlled outputs. This is to limit noise generated by quickly switching output signals. The slew rate is factory set to approximately 10 ns rise and fall times.

The bits in the P2M1 register that are not used to control configuration of P2.1 and P2.0 are used for other purposes. These bits can enable Schmitt trigger inputs on each I/O port, enable toggle outputs from Timer 0 and Timer 1, and enable a clock output if either the internal RC oscillator or external clock input is being used. The last two functions are described in the Timer/Counters and Oscillator sections respectively. The enable bits for all of these functions are shown in Figure 15.

Each I/O port of the P87LPC767 may be selected to use TTL level inputs or Schmitt inputs with hysteresis. A single configuration bit determines this selection for the entire port. Port pins P1.2, P1.3, and P1.5 always have a Schmitt trigger input.

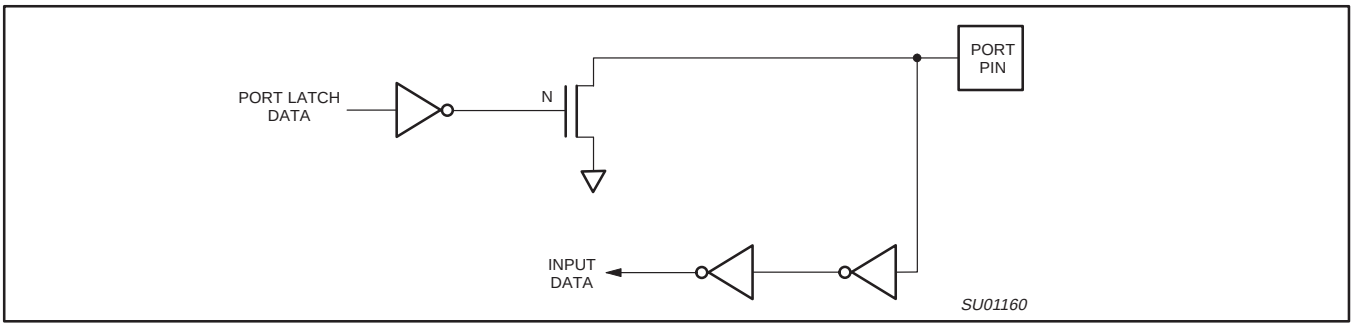


Figure 13. Open Drain Output

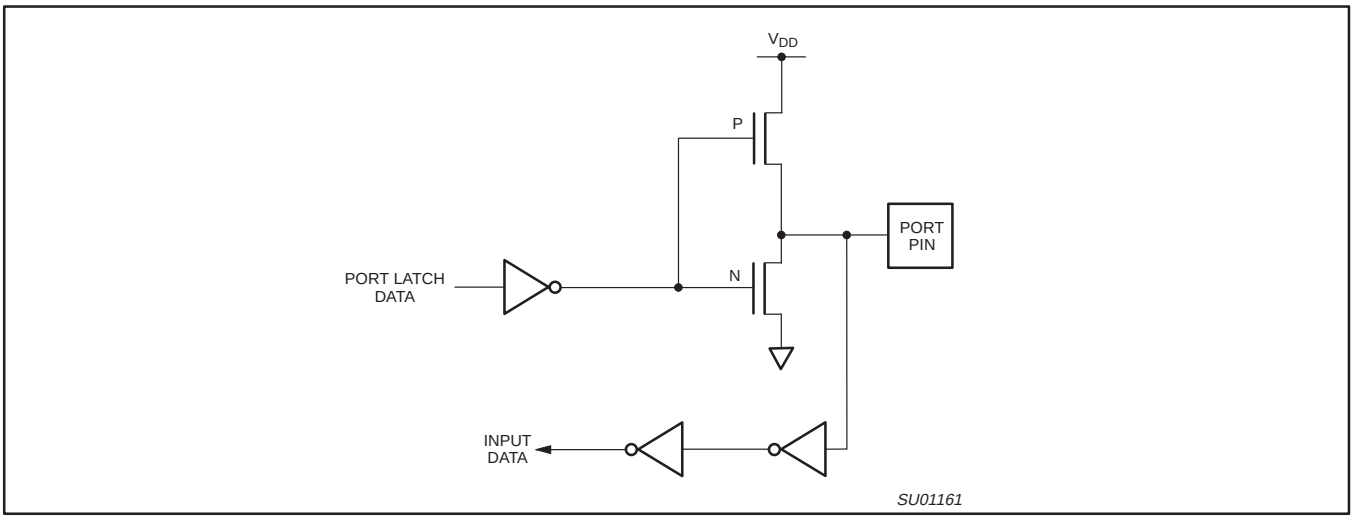


Figure 14. Push-Pull Output

Oscillator

The P87LPC767 provides several user selectable oscillator options, allowing optimization for a range of needs from high precision to lowest possible cost. These are configured when the EPROM is programmed. Basic oscillator types that are supported include: low, medium, and high speed crystals, covering a range from 20 kHz to 20 MHz; ceramic resonators; and on-chip RC oscillator.

Low Frequency Oscillator Option

This option supports an external crystal in the range of 20 kHz to 100 kHz.

Table 6 shows capacitor values that may be used with a quartz crystal in this mode.

Table 6. Recommended oscillator capacitors for use with the low frequency oscillator option

Oscillator Frequency	V_{DD} = 2.7 to 4.5 V			V_{DD} = 4.5 to 6.0 V		
	Lower Limit	Optimal Value	Upper Limit	Lower Limit	Optimal Value	Upper Limit
20 kHz	15 pF	15 pF	33 pF	33 pF	33 pF	47 pF
32 kHz	15 pF	15 pF	33 pF	33 pF	33 pF	47 pF
100 kHz	15 pF	15 pF	33 pF	15 pF	15 pF	33 pF

Medium Frequency Oscillator Option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

Table 7 shows capacitor values that may be used with a quartz crystal in this mode.

Table 7. Recommended oscillator capacitors for use with the medium frequency oscillator option

Oscillator Frequency	V_{DD} = 2.7 to 4.5 V		
	Lower Limit	Optimal Value	Upper Limit
100 kHz	33 pF	33 pF	47 pF
1 MHz	15 pF	15 pF	33 pF
4 MHz	15 pF	15 pF	33 pF

High Frequency Oscillator Option

This option supports an external crystal in the range of 4 to 20 MHz. Ceramic resonators are also supported in this configuration.

Table 8 shows capacitor values that may be used with a quartz crystal in this mode.

Table 8. Recommended oscillator capacitors for use with the high frequency oscillator option

Oscillator Frequency	V_{DD} = 2.7 to 4.5 V			V_{DD} = 4.5 to 6.0 V		
	Lower Limit	Optimal Value	Upper Limit	Lower Limit	Optimal Value	Upper Limit
4 MHz	15 pF	33 pF	47 pF	15 pF	33 pF	68 pF
8 MHz	15 pF	15 pF	33 pF	15 pF	33 pF	47 pF
16 MHz	–	–	–	15 pF	15 pF	33 pF
20 MHz	–	–	–	15 pF	15 pF	33 pF

On-Chip RC Oscillator Option

The on-chip RC oscillator option has a typical frequency of 6 MHz and can be divided down for slower operation through the use of the DIVM register. Note that the on-chip oscillator has a ±25% frequency tolerance and for that reason may not be suitable for use in some applications. A clock output on the X2/P2.0 pin may be enabled when the on-chip RC oscillator is used.

External Clock Input Option

In this configuration, the processor clock is input from an external source driving the X1/P2.1 pin. The rate may be from 0 Hz up to 20 MHz when V_{DD} is above 4.5 V and up to 10 MHz when V_{DD} is below 4.5 V. When the external clock input mode is used, the X2/P2.0 pin may be used as a standard port pin. A clock output on the X2/P2.0 pin may be enabled when the external clock input is used.

Clock Output

The P87LPC767 supports a clock output function when either the on-chip RC oscillator or external clock input options are selected. This allows external devices to synchronize to the P87LPC767. When enabled, via the ENCLK bit in the P2M1 register, the clock output appears on the X2/CLKOUT pin whenever the on-chip oscillator is running, including in Idle mode. The frequency of the clock output is 1/6 of the CPU clock rate. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power. The clock output may also be enabled when the external clock input option is selected.

Table 9. Sources of Wakeup from Power Down Mode

Wakeup Source	Conditions
External Interrupt 0 or 1	The corresponding interrupt must be enabled.
Keyboard Interrupt	The keyboard interrupt feature must be enabled and properly set up. The corresponding interrupt must be enabled.
Comparator 1 or 2	The comparator(s) must be enabled and properly set up. The corresponding interrupt must be enabled.
Watchdog Timer Reset	The watchdog timer must be enabled via the WDTE bit in the UCFG1 EPROM configuration byte.
Watchdog Timer Interrupt	The WDTE bit in the UCFG1 EPROM configuration byte must not be set. The corresponding interrupt must be enabled.
Brownout Detect Reset	The BOD bit in AUXR1 must not be set (brownout detect not disabled). The BOI bit in AUXR1 must not be set (brownout interrupt disabled).
Brownout Detect Interrupt	The BOD bit in AUXR1 must not be set (brownout detect not disabled). The BOI bit in AUXR1 must be set (brownout interrupt enabled). The corresponding interrupt must be enabled.
Reset Input	The external reset input must be enabled.
A/D converter	Must use internal RC clock (RCCLK = 1) for A/D converter to work in Power Down mode. The A/D must be enabled and properly set up. The corresponding interrupt must be enabled.

Table 11. Baud Rates, Timer Values, and CPU Clock Frequencies for SMOD1 = 1

Timer Count	Baud Rate						
	2400	4800	9600	19.2k	38.4k	57.6k	115.2k
–1	0.2304	0.4608	0.9216	* 1.8432	* 3.6864	5.5296	* 11.0592
–2	0.4608	0.9216	* 1.8432	* 3.6864	* 7.3728	* 11.0592	–
–3	0.6912	1.3824	2.7648	5.5296	* 11.0592	16.5888	–
–4	0.9216	* 1.8432	* 3.6864	* 7.3728	* 14.7456	–	–
–5	1.1520	2.3040	4.6080	9.2160	* 18.4320	–	–
–6	1.3824	2.7648	5.5296	* 11.0592	–	–	–
–7	1.6128	3.2256	6.4512	12.9024	–	–	–
–8	* 1.8432	* 3.6864	* 7.3728	* 14.7456	–	–	–
–9	2.0736	4.1472	8.2944	16.5888	–	–	–
–10	2.3040	4.6080	9.2160	* 18.4320	–	–	–
–11	2.5344	5.0688	10.1376	–	–	–	–
–12	2.7648	5.5296	* 11.0592	–	–	–	–
–13	2.9952	5.9904	11.9808	–	–	–	–
–14	3.2256	6.4512	12.9024	–	–	–	–
–15	3.4560	6.9120	13.8240	–	–	–	–
–16	* 3.6864	* 7.3728	* 14.7456	–	–	–	–
–17	3.9168	7.8336	15.6672	–	–	–	–
–18	4.1472	8.2944	16.5888	–	–	–	–
–19	4.3776	8.7552	17.5104	–	–	–	–
–20	4.6080	9.2160	* 18.4320	–	–	–	–
–21	4.8384	9.6768	19.3536	–	–	–	–

NOTES TO TABLES 10 AND 11:

1. Tables 6 and 7 apply to UART modes 1 and 3 (variable rate modes), and show CPU clock rates in MHz for standard baud rates from 2400 to 115.2k baud.
2. Table 6 shows timer settings and CPU clock rates with the SMOD1 bit in the PCON register = 0 (the default after reset), while Table 7 reflects the SMOD1 bit = 1.
3. The tables show all potential CPU clock frequencies up to 20 MHz that may be used for baud rates from 9600 baud to 115.2k baud. Other CPU clock frequencies that would give only lower baud rates are not shown.
4. Table entries marked with an asterisk (*) indicate standard crystal and ceramic resonator frequencies that may be obtained from many sources without special ordering.

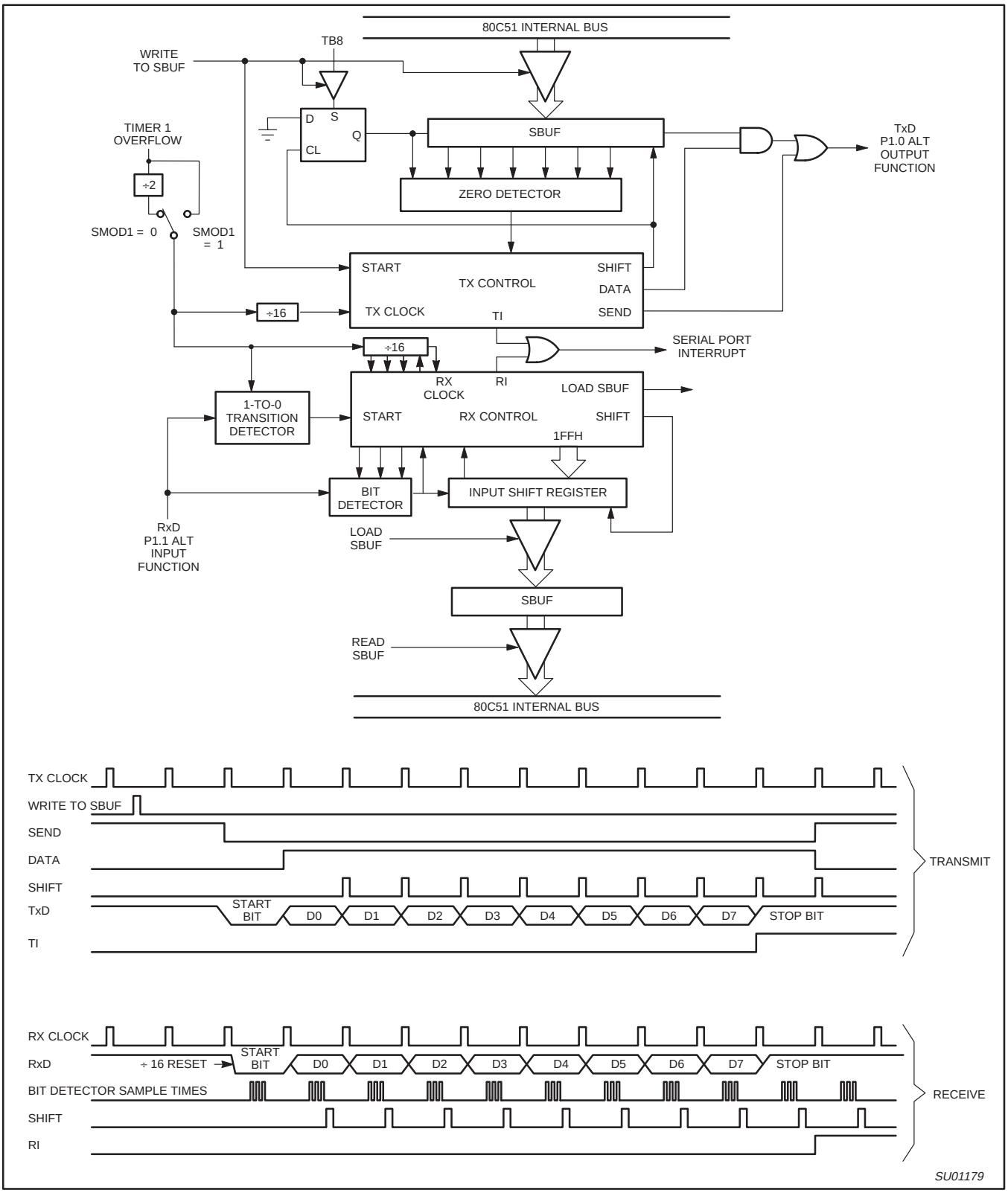


Figure 32. Serial Port Mode 1

More About UART Modes 2 and 3

Eleven bits are transmitted (through TxD), or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8) can be assigned the value of 0 or 1. On receive, the 9the data bit goes into RB8 in SCON. The baud rate is programmable to either 1/16 or 1/32 of the CPU clock frequency in Mode 2. Mode 3 may have a variable baud rate generated from Timer 1.

Figures 33 and 34 show a functional diagram of the serial port in Modes 2 and 3. The receive portion is exactly the same as in Mode 1. The transmit portion differs from Mode 1 only in the 9th bit of the transmit shift register.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads TB8 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SBUF” signal.)

The transmission begins with activation of SEND, which puts the start bit at TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that. The first shift clocks a 1 (the stop bit) into the 9th bit position of the shift register. Thereafter, only zeros are clocked in. Thus, as data bits shift out to the right, zeros are clocked in from the left. When TB8 is at the output position of the shift register, then the stop bit is just to the left of TB8, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 11th divide-by-16 rollover after “write to SBUF.”

Reception is initiated by a detected 1-to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written to the input shift register.

At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of R–D. The value accepted is the value that was seen in at least 2 of the 3 samples. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in Modes 2 and 3 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI.

The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated. 1. RI = 0, and 2. Either SM2 = 0, or the received 9th data bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits go into SBUF. One bit time later, whether the above conditions were met or not, the unit goes back to looking for a 1-to-0 transition at the RxD input.

Multiprocessor Communications

UART modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received or transmitted. When data is received, the 9th bit is stored in RB8. The UART can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. One way to use this feature in multiprocessor systems is as follows:

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that follow. The slaves that weren’t being addressed leave their SM2 bits set and go on about their business, ignoring the subsequent data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit, although this is better done with the Framing Error flag. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

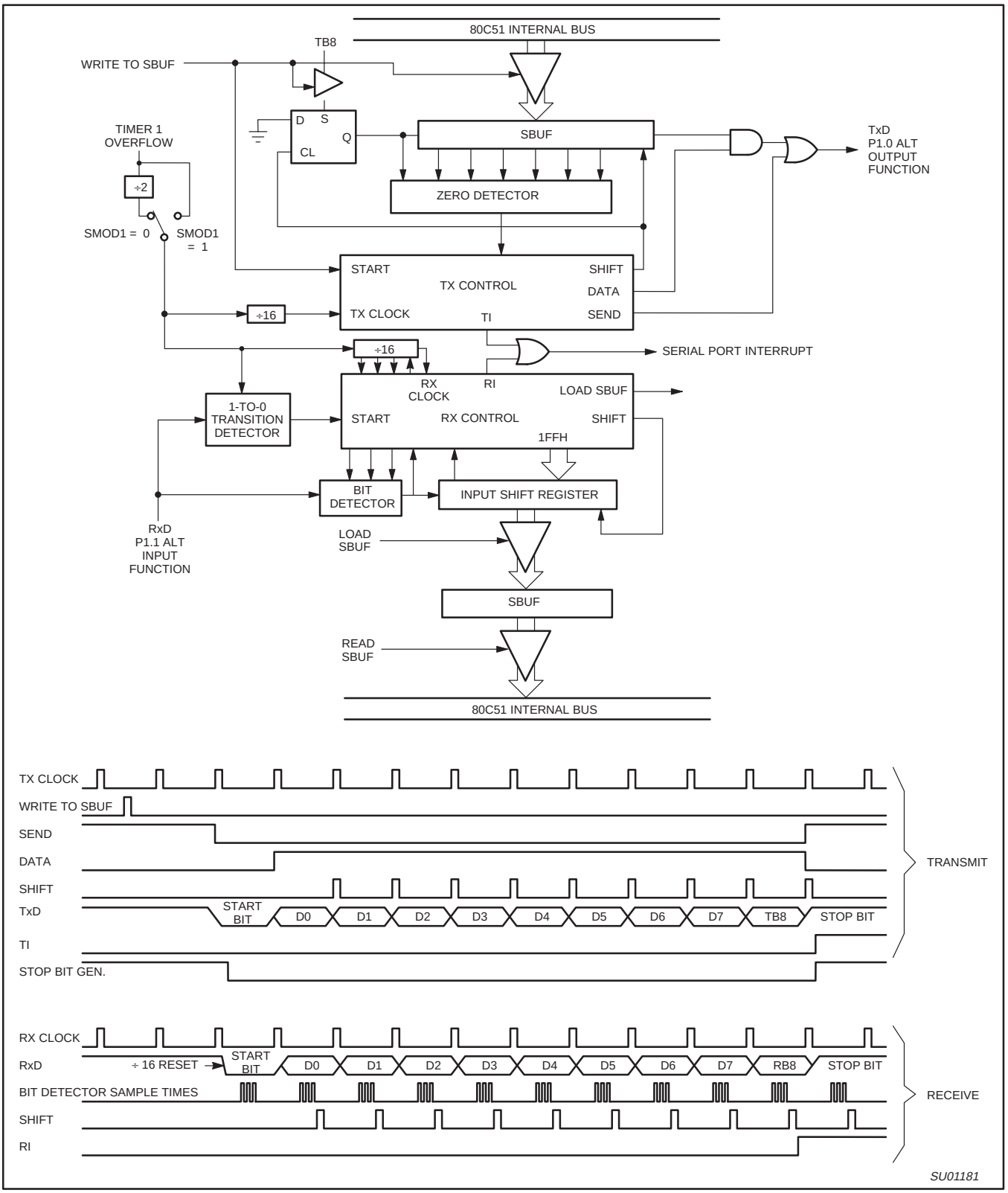


Figure 34. Serial Port Mode 3

UCFG2 Address: FD01h Unprogrammed Value: FFh

7	6	5	4	3	2	1	0
SB2	SB1	—	—	—	—	—	—

BIT	SYMBOL	FUNCTION
UCFG2.7, 6	SB2, SB1	EPROM security bits. See table entitled, “EPROM Security Bits” for details.
UCFG2.5–0	—	Reserved for future use.

SU01186

Figure 39. EPROM System Configuration Byte 2 (UCFG2)

Security Bits
When neither of the security bits are programmed, the code in the EPROM can be verified. When only security bit 1 is programmed, all further programming of the EPROM is disabled. At that point, only security bit 2 may still be programmed. When both security bits are programmed, EPROM verify is also disabled.

Table 12. EPROM Security Bits

SB2	SB1	Protection Description
1	1	Both security bits unprogrammed. No program security features enabled. EPROM is programmable and verifiable.
1	0	Only security bit 1 programmed. Further EPROM programming is disabled. Security bit 2 may still be programmed.
0	1	Only security bit 2 programmed. This combination is not supported.
0	0	Both security bits programmed. All EPROM verification and programming are disabled.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Operating temperature under bias	–55 to +125	°C
Storage temperature range	–65 to +150	°C
Voltage on $\overline{RST}/V_{PP}$ pin to V_{SS}	0 to +11.0	V
Voltage on any other pin to V_{SS}	–0.5 to V_{DD}+0.5 V	V
Maximum I_{OL} per I/O pin	20	mA
Power dissipation (based on package heat transfer, not device power consumption)	1.5	W

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification are not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.

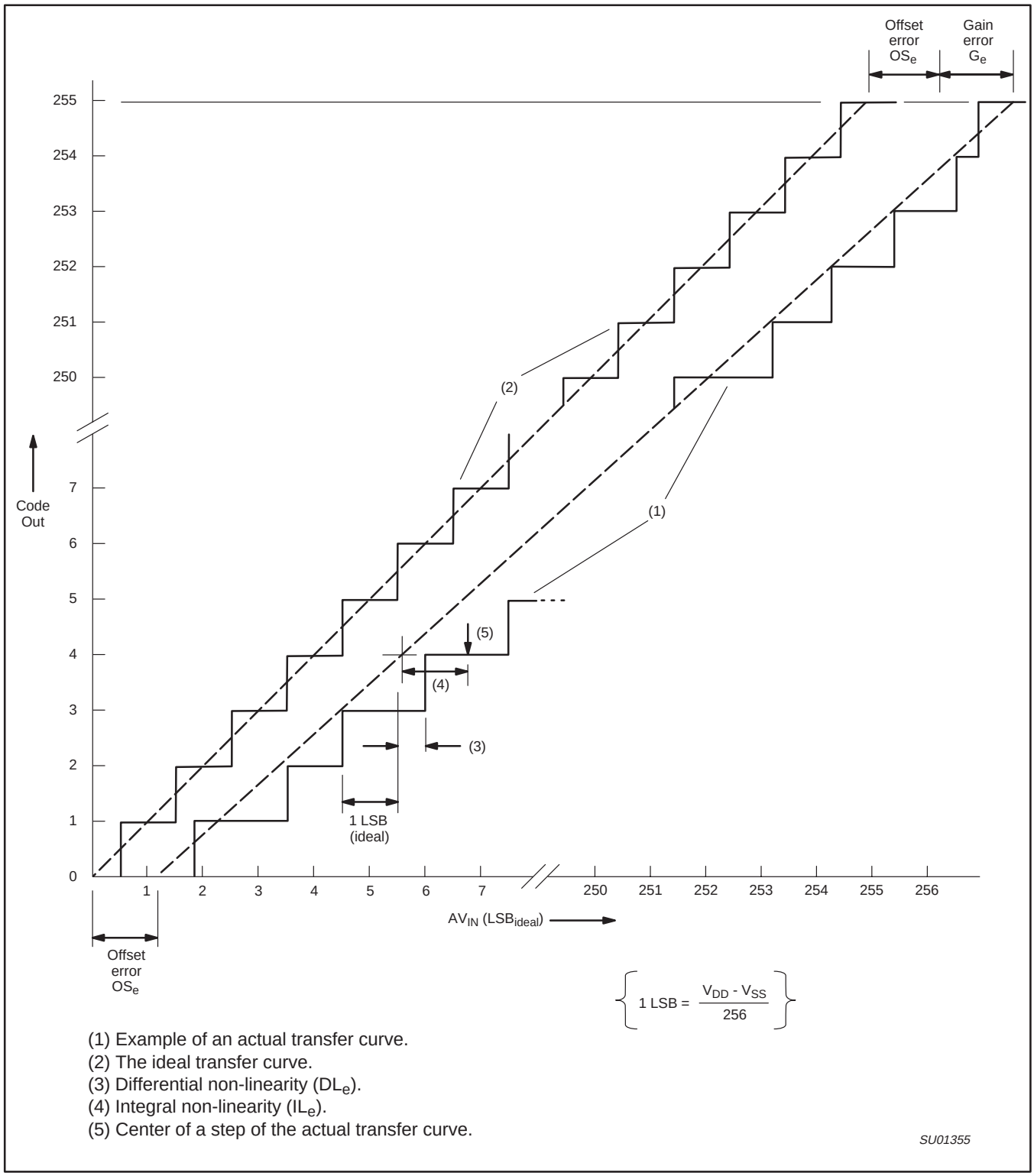


Figure 40. A/D Conversion Characteristics

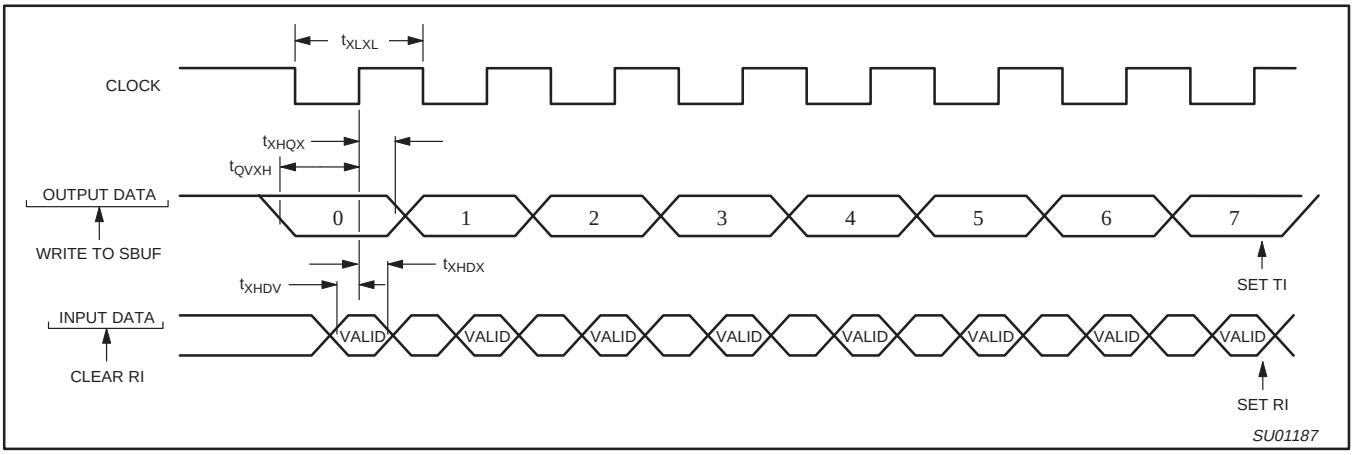


Figure 41. Shift Register Mode Timing

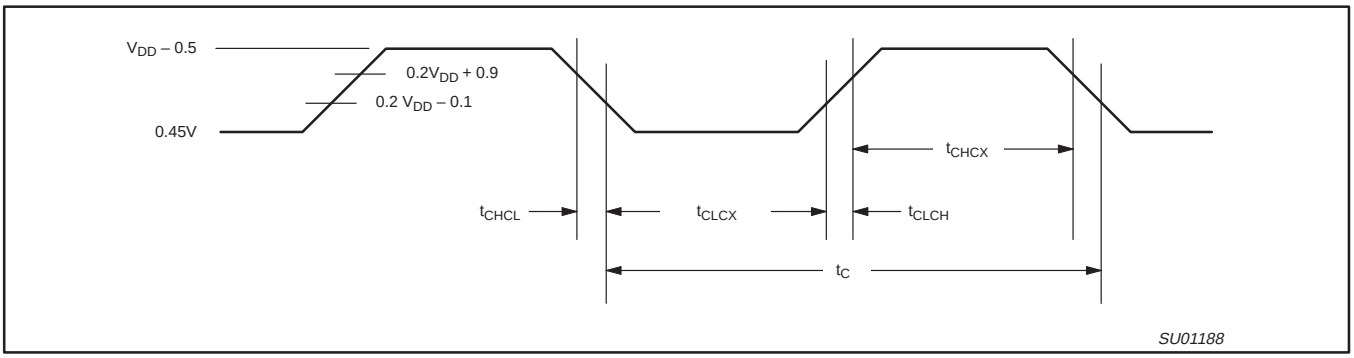


Figure 42. External Clock Timing

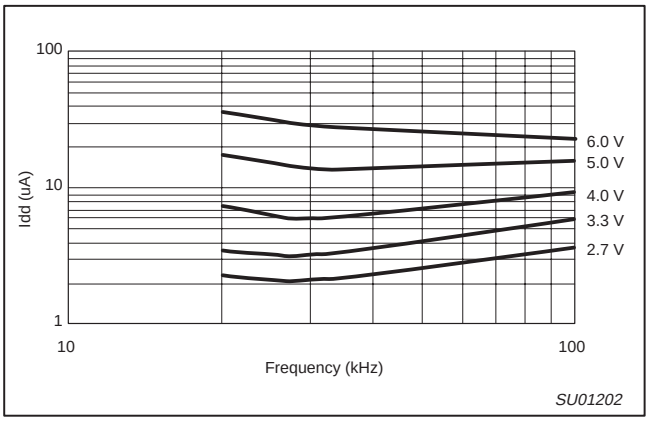


Figure 43. Typical Idd versus frequency (low frequency oscillator, 25 °C)

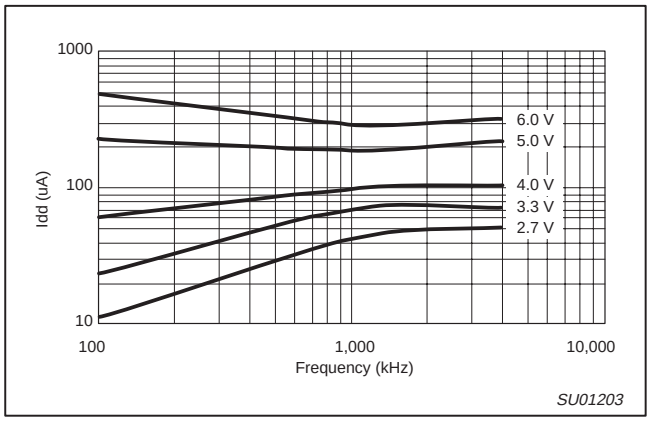
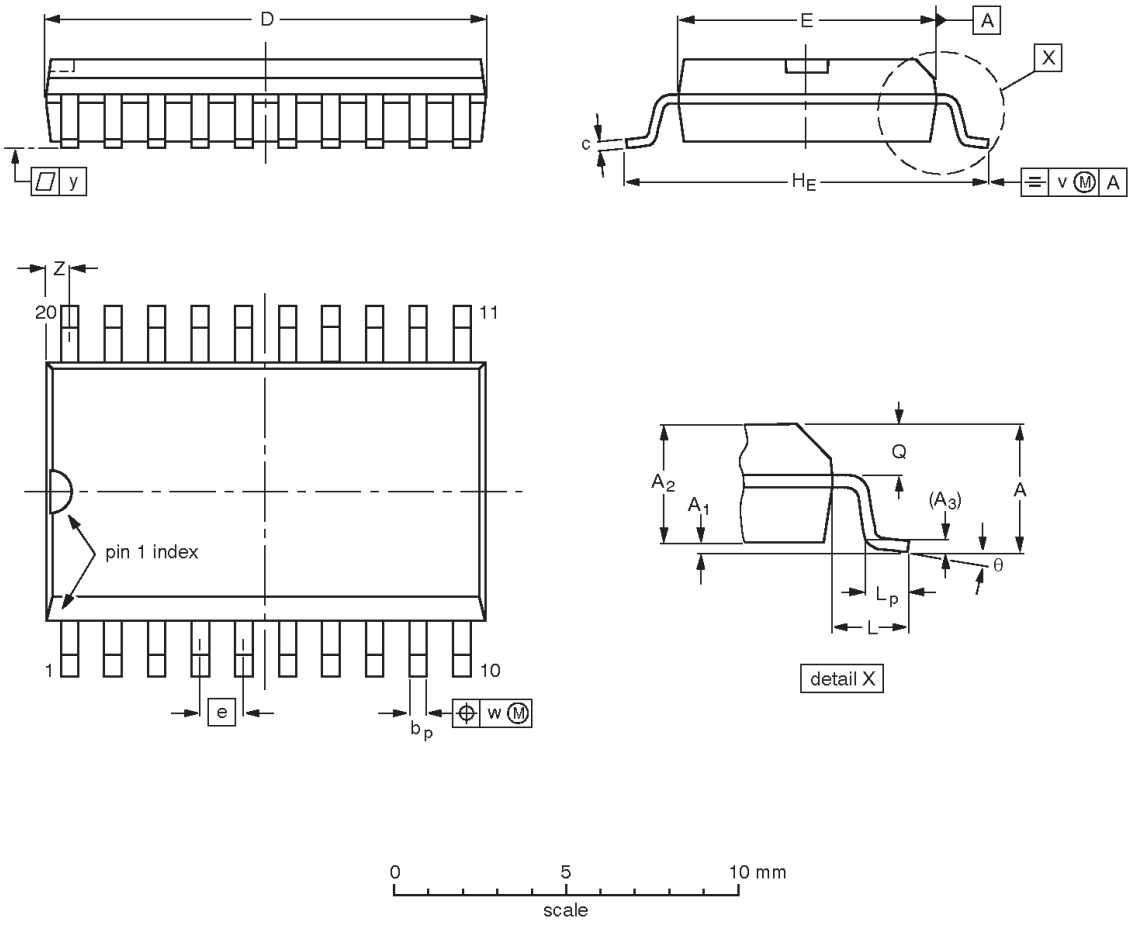


Figure 44. Typical Idd versus frequency (medium frequency oscillator, 25 °C)

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013				~~97-05-22~~ 99-12-27

REVISION HISTORY

Date	CPCN	Description
2002 Mar 25	9397 750 09557	– Added revision history – Updated Reset section
2001 Aug 07	9397 750 08675	Previous release

Low power, low price, low pin count (20 pin) microcontroller with 4-kbyte OTP and 8-bit A/D converter

P87LPC767

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Date of release: 03-02

Document order number: 9397 750 09557

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