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NXP USA Inc. - P87LPC767FD,512 Datasheet



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Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-50
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p87lpc767fd-512

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

BLOCK DIAGRAM



Low power, low price, low pin count (20 pin) microcontroller with 4-kbyte OTP and 8-bit A/D converter



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Figure 5. Comparator Input and Output Connections



Figure 6. Comparator Configurations

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Internal Reference Voltage

An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as V_{ref} , is 1.28 V ±10%.

Comparator Interrupt

Each comparator has an interrupt flag CMFn contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt. The interrupt will be generated when the corresponding enable bit ECn in the IEN1 register is set and the interrupt system is enabled via the EA bit in the IEN0 register.

Comparators and Power Reduction Modes

Either or both comparators may remain enabled when Power Down or Idle mode is activated. The comparators will continue to function in the power reduction mode. If a comparator interrupt is enabled, a change of the comparator output state will generate an interrupt and wake up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in power down mode. The reason is that with the oscillator stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

Comparators consume power in Power Down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue.

Comparator Configuration Example

The code shown in Figure 7 is an example of initializing one comparator. Comparator 1 is configured to use the CIN1A and CMPREF inputs, outputs the comparator result to the CMP1 pin, and generates an interrupt when the comparator output changes.

The interrupt routine used for the comparator must clear the interrupt flag (CMF1 in this case) before returning.

CmpIni	.t:	
mo	v PT0AD,#301	n ; Disable digital inputs on pins that are used
		; for analog functions: CIN1A, CMPREF.
an	1 POM2,#0cfl	n ; Disable digital outputs on pins that are used
or	l POM1,#30h	; for analog functions: CIN1A, CMPREF.
mo	v CMP1,#24h	; Turn on comparator 1 and set up for:
		; - Positive input on CIN1A.
		; - Negative input from CMPREF pin.
		; - Output to CMP1 pin enabled.
ca	ll delay10us	; The comparator has to start up for at
		; least 10 microseconds before use.
an	l CMP1,#0feł	n ; Clear comparator 1 interrupt flag.
se	tb EC1	; Enable the comparator 1 interrupt. The
		; priority is left at the current value.
se	tb EA	; Enable the interrupt system (if needed).
re	t	; Return to caller.
		SU01189

Figure 7.

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Table 2. Interaction of TIRUN with SLAVEN, MASTRQ, and MASTER

SLAVEN, MASTRQ, MASTER	TIRUN	OPERATING MODE
All 0	0	The I ² C interface is disabled. Timer I is cleared and does not run. This is the state assumed after a reset. If an I ² C application wants to ignore the I ² C at certain times, it should write SLAVEN, MASTRQ, and TIRUN all to zero.
All 0	1	The I ² C interface is disabled.
Any or all 1	0	The I ² C interface is enabled. The 3 low-order bits of Timer I run for min-time generation, but the hi-order bits do not, so that there is no checking for I ² C being "hung." This configuration can be used for very slow I ² C operation.
Any or all 1	1	The I ² C interface is enabled. Timer I runs during frames on the I ² C, and is cleared by transitions on SCL, and by Start and Stop conditions. This is the normal state for I ² C operation.

Table 3. CT1, CT0 Values

CT1, CT0	Min Time Count (Machine Cycles)	CPU Clock Max (for 100 kHz I ² C)	Timeout Period (Machine Cycles)
1 0	7	8.4 MHz	1023
0 1	6	7.2 MHz	1022
0 0	5	6.0 MHz	1021
11	4	4.8 MHz	1020

Interrupts

The P87LPC767 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the P87LPC767's many interrupt sources. The P87LPC767 supports up to 13 interrupt sources.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts at once.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the IPO, IPOH, IP1, and IP1H registers. An interrupt service routine in progress can be

interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. So, if two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve simultaneous requests of the same priority level.

Table 3 summarizes the interrupt sources, flag bits, vector addresses, enable bits, priority bits, arbitration ranking, and whether each interrupt may wake up the CPU from Power Down mode.

Table 4. Summary of Interrupts

Description	Interrupt Flag Bit(s)	Vector Address	Interrupt Enable Bit(s)	Interrupt Priority	Arbitration Ranking	Power Down Wakeup
External Interrupt 0	IE0	0003h	EX0 (IEN0.0)	IP0H.0, IP0.0	1 (highest)	Yes
Timer 0 Interrupt	TF0	000Bh	ET0 (IEN0.1)	IP0H.1, IP0.1	4	No
External Interrupt 1	IE1	0013h	EX1 (IEN0.2)	IP0H.2, IP0.2	7	Yes
Timer 1 Interrupt	TF1	001Bh	ET1 (IEN0.3)	IP0H.3, IP0.3	10	No
Serial Port Tx and Rx	TI & RI	0023h	ES (IEN0.4)	IP0H.4, IP0.4	12	No
Brownout Detect	BOF	002Bh	EBO (IEN0.5)	IP0H.5, IP0.5	2	Yes
I ² C Interrupt	ATN	0033h	EI2 (IEN1.0)	IP1H.0, IP1.0	5	No
KBI Interrupt	KBF	003Bh	EKB (IEN1.1)	IP1H.1, IP1.1	8	Yes
Comparator 2 interrupt	CMF2	0043h	EC2 (IEN1.2)	IP1H.2, IP1.2	11	Yes
Watchdog Timer	WDOVF	0053h	EWD (IEN0.6)	IP0H.6, IP0.6	3	Yes
A/D Converter	ADCI	005Bh	EAD (IEN1.4)	IP1H.4, IP1.4	6	Yes
Comparator 1 interrupt	CMF1	0063h	EC1 (IEN1.5)	IP1H.5, IP1.5	9	Yes
Timer I	_	0073h	ETI (IEN1.7)	IP1H.7, IP1.7	13 (lowest)	No

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Figure 15. Port 2 Mode Register 1 (P2M1)

Keyboard Interrupt (KBI)

The Keyboard Interrupt function is intended primarily to allow a single interrupt to be generated when any key is pressed on a keyboard or keypad connected to specific pins of the P87LPC767, as shown in Figure 16. This interrupt may be used to wake up the CPU from Idle or Power Down modes. This feature is particularly useful in handheld, battery powered systems that need to carefully manage power consumption yet also need to be convenient to use.

The P87LPC767 allows any or all pins of port 0 to be enabled to cause this interrupt. Port pins are enabled by the setting of bits in

the KBI register, as shown in Figure 17. The Keyboard Interrupt Flag (KBF) in the AUXR1 register is set when any enabled pin is pulled low while the KBI interrupt function is active. An interrupt will generated if it has been enabled. Note that the KBF bit must be cleared by software.

Due to human time scales and the mechanical delay associated with keyswitch closures, the KBI feature will typically allow the interrupt service routine to poll port 0 in order to determine which key was pressed, even if the processor has to wake up from Power Down mode. Refer to the section on Power Reduction Modes for details.



Figure 16. Keyboard Interrupt

KBI	Addre	ess: 86h								Reset Value: 00h
	Not E	Bit Addressable	9							
		-		-			•			
		/	6	5	4	3	2	1	0	
		KBI	.7 KBI.6	KBI.5	KBI.4	KBI.3	KBI.2	KBI.1	KBI.0	
	BIT	SYMBOL	FUNCTION							
	KBI.7	KBI.7	When set, ena	ables P0.7	as a caus	e of a Key	board Inte	errupt.		
	KBI.6	KBI.6	When set, ena	ables P0.6	as a caus	e of a Key	/board Inte	errupt.		
	KBI.5	KBI.5	When set, ena	ables P0.5	as a caus	e of a Key	board Inte	errupt.		
	KBI.4	KBI.4	When set, ena	ables P0.4	as a caus	e of a Key	board Inte	errupt.		
	KBI.3	KBI.3	When set, ena	ables P0.3	as a caus	e of a Key	/board Inte	errupt.		
	KBI.2	KBI.2	When set, ena	ables P0.2	as a caus	e of a Key	/board Inte	errupt.		
	KBI.1	KBI.1	When set, ena	ables P0.1	as a caus	e of a Key	board Inte	errupt.		
	KBI.0	KBI.0	When set, ena	ables P0.0	as a caus	e of a Key	board Inte	errupt.		
	Note: the	Keyboard Inte	rrupt must be en	abled in or	der for the	e settings	of the KBI	register to	be effectiv	e. The interrupt flag
	(KBF) is lo	ocated at bit 7	of AUXR1.							
										SU01164

Figure 17. Keyboard Interrupt Register (KBI)

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Oscillator

The P87LPC767 provides several user selectable oscillator options, allowing optimization for a range of needs from high precision to lowest possible cost. These are configured when the EPROM is

programmed. Basic oscillator types that are supported include: low, medium, and high speed crystals, covering a range from 20 kHz to 20 MHz; ceramic resonators; and on-chip RC oscillator.

Low Frequency Oscillator Option

This option supports an external crystal in the range of 20 kHz to 100 kHz.

Table 6 shows capacitor values that may be used with a quartz crystal in this mode.

Table 6. Recommended oscillator capacitors for use with the low frequency oscillator option

Oscillator		V_{DD} = 2.7 to 4.5 V	-	V _{DD} = 4.5 to 6.0 V			
Frequency	Lower Limit	Optimal Value	Upper Limit	Lower Limit	Optimal Value	Upper Limit	
20 kHz	15 pF	15 pF	33 pF	33 pF	33 pF	47 pF	
32 kHz	15 pF	15 pF	33 pF	33 pF	33 pF	47 pF	
100 kHz	15 pF	15 pF	33 pF	15 pF	15 pF	33 pF	

Medium Frequency Oscillator Option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

Table 7 shows capacitor values that may be used with a quartz crystal in this mode.

Table 7. Recommended oscillator capacitors for use with the medium frequency oscillator option

Oscillator Frequency	V _{DD} = 2.7 to 4.5 V							
Oscillator r requercy	Lower Limit	Optimal Value	Upper Limit					
100 kHz	33 pF	33 pF	47 pF					
1 MHz	15 pF	15 pF	33 pF					
4 MHz	15 pF	15 pF	33 pF					

High Frequency Oscillator Option

This option supports an external crystal in the range of 4 to 20 MHz. Ceramic resonators are also supported in this configuration.

Table 8 shows capacitor values that may be used with a quartz crystal in this mode.

Table 8. Recommended oscillator capacitors for use with the high frequency oscillator option

Oscillator		V_{DD} = 2.7 to 4.5 V		V _{DD} = 4.5 to 6.0 V			
Frequency	Lower Limit	Optimal Value Upper Limit		Lower Limit	Optimal Value	Upper Limit	
4 MHz	15 pF	33 pF	47 pF	15 pF	33 pF	68 pF	
8 MHz	15 pF	15 pF	33 pF	15 pF	33 pF	47 pF	
16 MHz	-	-	-	15 pF	15 pF	33 pF	
20 MHz	-	-	-	15 pF	15 pF	33 pF	

On-Chip RC Oscillator Option

The on-chip RC oscillator option has a typical frequency of 6 MHz and can be divided down for slower operation through the use of the DIVM register. Note that the on-chip oscillator has a $\pm 25\%$ frequency tolerance and for that reason may not be suitable for use in some applications. A clock output on the X2/P2.0 pin may be enabled when the on-chip RC oscillator is used.

External Clock Input Option

In this configuration, the processor clock is input from an external source driving the X1/P2.1 pin. The rate may be from 0 Hz up to 20 MHz when V_{DD} is above 4.5 V and up to 10 MHz when V_{DD} is below 4.5 V. When the external clock input mode is used, the X2/P2.0

pin may be used as a standard port pin. A clock output on the X2/P2.0 pin may be enabled when the external clock input is used.

Clock Output

The P87LPC767 supports a clock output function when either the on-chip RC oscillator or external clock input options are selected. This allows external devices to synchronize to the P87LPC767. When enabled, via the ENCLK bit in the P2M1 register, the clock output appears on the X2/CLKOUT pin whenever the on-chip oscillator is running, including in Idle mode. The frequency of the clock output is 1/6 of the CPU clock rate. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power. The clock output may also be enabled when the external clock input option is selected.

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Figure 20. Block Diagram of Oscillator Control

CPU Clock Modification: CLKR and DIVM

For backward compatibility, the CLKR configuration bit allows setting the P87LPC767 instruction and peripheral timing to match standard 80C51 timing by dividing the CPU clock by two. Default timing for the P87LPC767 is 6 CPU clocks per machine cycle while standard 80C51 timing is 12 clocks per machine cycle. This division also applies to peripheral timing, allowing 80C51 code that is oscillator frequency and/or timer rate dependent. The CLKR bit is located in the EPROM configuration register UCFG1, described under EPROM Characteristics

In addition to this, the CPU clock may be divided down from the oscillator rate by a programmable divider, under program control. This function is controlled by the DIVM register. If the DIVM register is set to zero (the default value), the CPU will be clocked by either the unmodified oscillator rate, or that rate divided by two, as determined by the previously described CLKR function.

When the DIVM register is set to some value N (between 1 and 255), the CPU clock is divided by 2 * (N + 1). Clock division values from 4 through 512 are thus possible. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption, in a manner similar to Idle mode. By dividing the clock, the CPU can retain the ability to respond to events other than those that can cause interrupts (i.e., events that allow exiting the Idle mode) by executing its normal program at a lower rate. This can allow bypassing the oscillator startup time in cases where Power Down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

Power Monitoring Functions

The P87LPC767 incorporates power monitoring functions designed to prevent incorrect operation during initial power up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-On Detect and Brownout Detect.

Brownout Detection

The Brownout Detect function allows preventing the processor from failing in an unpredictable manner if the power supply voltage drops below a certain level. The default operation is for a brownout detection to cause a processor reset, however it may alternatively be configured to generate an interrupt by setting the BOI bit in the AUXR1 register (AUXR1.5).

The P87LPC767 allows selection of two Brownout levels: 2.5 V or 3.8 V. When V_{DD} drops below the selected voltage, the brownout detector triggers and remains active until V_{DD} is returns to a level above the Brownout Detect voltage. When Brownout Detect causes a processor reset, that reset remains active as long as V_{DD} remains below the Brownout Detect voltage. When Brownout Detect generates an interrupt, that interrupt occurs once as V_{DD} crosses from above to below the Brownout Detect voltage. For the interrupt to be processed, the interrupt system and the BOI interrupt must both be enabled (via the EA and EBO bits in IEN0).

When Brownout Detect is activated, the BOF flag in the PCON register is set so that the cause of processor reset may be determined by software. This flag will remain set until cleared by software.

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Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register (THn and TLn) are used. See Figure 27

Mode 2

Mode 2 configures the Timer register as an 8-bit Counter (TL1) with automatic reload, as shown in Figure 28. Overflow from TLn not only sets TFn, but also reloads TLn with the contents of THn, which must be preset by software. The reload leaves THn unchanged. Mode 2 operation is the same for Timer 0 and Timer 1.

Mode 3

When Timer 1 is in Mode 3 it is stopped. The effect is the same as setting TR1 = 0.

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate 8-bit counters. The logic for Mode 3 on Timer 0 is shown in Figure 29. TL0 uses the Timer 0 control bits: C/T, GATE, TR0, INT0, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the "Timer 1" interrupt.

Mode 3 is provided for applications that require an extra 8-bit timer. With Timer 0 in Mode 3, an P87LPC767 can look like it has three Timer/Counters. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it into and out of its own Mode 3. It can still be used by the serial port as a baud rate generator, or in any application not requiring an interrupt.



Figure 27. Timer/Counter 0 or 1 in Mode 1 (16-Bit Counter)



Figure 28. Timer/Counter 0 or 1 in Mode 2 (8-Bit Auto-Reload)

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Figure 29. Timer/Counter 0 Mode 3 (Two 8-Bit Counters)

Timer Overflow Toggle Output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. This function is enabled by control bits TOOE and T1OE in the P2M1 register, and apply to Timer 0 and Timer 1 respectively. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

UART

The P87LPC767 includes an enhanced 80C51 UART. The baud rate source for the UART is timer 1 for modes 1 and 3, while the rate is fixed in modes 0 and 2. Because CPU clocking is different on the P87LPC767 than on the standard 80C51, baud rate calculation is somewhat different. Enhancements over the standard 80C51 UART include Framing Error detection and automatic address recognition.

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the SBUF register. However, if the first byte still hasn't been read by the time reception of the second byte is complete, the first byte will be lost. The serial port receive and transmit registers are both accessed through Special Function Register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

The serial port can be operated in 4 modes:

Mode 0

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at 1/6 of the CPU clock frequency.

Mode 1

10 bits are transmitted (through TxD) or received (through RxD): a start bit (logical 0), 8 data bits (LSB first), and a stop bit (logical 1). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate.

Mode 2

11 bits are transmitted (through TxD) or received (through RxD): start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/16 or 1/32 of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

Mode 3

11 bits are transmitted (through TxD) or received (through RxD): a start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

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Baud Rates

The baud rate in Mode 0 is fixed: Mode 0 Baud Rate = CPU clock/6. The baud rate in Mode 2 depends on the value of bit SMOD1 in Special Function Register PCON. If SMOD1 = 0 (which is the value on reset), the baud rate is 1/32 of the CPU clock frequency. If SMOD1 = 1, the baud rate is 1/16 of the CPU clock frequency.

Mode 2 Baud Rate =
$$\frac{1 + SMOD1}{32} \times CPU$$
 clock frequency

Using Timer 1 to Generate Baud Rates

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD1. The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either "timer" or "counter" operation, and in any of its 3 running modes. In the most typical applications, it is configured for "timer" operation, in the auto-reload mode (high nibble of TMOD = 0010b). In that case the baud rate is given by the formula:

Mode 1, 3 Baud Rate =
$$\frac{\frac{\text{CPU clock frequency}}{192 \text{ (or 96 if SMOD1 = 1)}}}{256 - (\text{TH1})}$$

Tables 6 and 7 list various commonly used baud rates and how they can be obtained using Timer 1 as the baud rate generator.

Table 10. Baud Rates, Timer Values, and CPU Clock Frequencies for SMOD1 = 0

Timer Count	Baud Rate										
Timer Count	2400	4800	9600	19.2k	38.4k	57.6k					
-1	0.4608	0.9216	* 1.8432	* 3.6864	* 7.3728	* 11.0592					
-2	0.9216	1.8432	* 3.6864	* 7.3728	* 14.7456						
-3	1.3824	2.7648	5.5296	* 11.0592	-	-					
-4	* 1.8432	* 3.6864	* 7.3728	* 14.7456	-	-					
-5	2.3040	4.6080	9.2160	* 18.4320	-	-					
-6	2.7648	5.5296	* 11.0592	-	-	-					
-7	3.2256	6.4512	12.9024	-	-	-					
-8	* 3.6864	* 7.3728	* 14.7456	-	-	-					
-9	4.1472	8.2944	16.5888	-	-	-					
-10	4.6080	9.2160	* 18.4320	-	-	-					

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More About UART Mode 0

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/6 the CPU clock frequency. Figure 31 shows a simplified functional diagram of the serial port in Mode 0, and associated timing.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal at S6P2 also loads a 1 into the 9th position of the transmit shift register and tells the TX Control block to commence a transmission. The internal timing is such that one full machine cycle will elapse between "write to SBUF" and activation of SEND.

SEND enables the output of the shift register to the alternate output function line of P1.1 and also enable SHIFT CLOCK to the alternate output function line of P1.0. SHIFT CLOCK is low during S3, S4, and S5 of every machine cycle, and high during S6, S1, and S2. At S6P2 of every machine cycle in which SEND is active, the contents of the transmit shift are shifted to the right one position.

As data bits shift out to the right, zeros come in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position, is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control block to do one last shift and then deactivate SEND and set T1. Both of these actions occur at S1P1 of the 10th machine cycle after "write to SBUF." Reception is initiated by the condition REN = 1 and R1 = 0. At S6P2 of the next machine cycle, the RX Control unit writes the bits 1111110 t o the receive shift register, and in the next clock phase activates RECEIVE.

RECEIVE enable SHIFT CLOCK to the alternate output function line of P1.0. SHIFT CLOCK makes transitions at S3P1 and S6P1 of every machine cycle. At S6P2 of every machine cycle in which RECEIVE is active, the contents of the receive shift register are shifted to the left one position. The value that comes in from the right is the value that was sampled at the P1.1 pin at S5P2 of the same machine cycle.

As data bits come in from the right, 1s shift out to the left. When the 0 that was initially loaded into the rightmost position arrives at the leftmost position in the shift register, it flags the RX Control block to do one last shift and load SBUF. At S1P1 of the 10th machine cycle after the write to SCON that cleared RI, RECEIVE is cleared as RI is set.

More About UART Mode 1

Ten bits are transmitted (through TxD), or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in SCON. In the P87LPC767 the baud rate is determined by the Timer 1 overflow rate. Figure 32 shows a simplified functional diagram of the serial port in Mode 1, and associated timings for transmit receive.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal also loads a 1 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission actually commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the "write to SBUF" signal.)

The transmission begins with activation of SEND which puts the start bit at TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that.

As data bits shift out to the right, zeros are clocked in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 10th divide-by-16 rollover after "write to SBUF."

Reception is initiated by a detected 1-to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written into the input shift register. Resetting the divide-by-16 counter aligns its rollovers with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RxD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in mode 1 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated.: 1. R1 = 0, and 2. Either SM2 = 0, or the received stop bit = 1.

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated. At this time, whether the above conditions are met or not, the unit goes back to looking for a 1-to-0 transition in RxD.



Figure 31. Serial Port Mode 0





Figure 32. Serial Port Mode 1



Figure 33. Serial Port Mode 2



Figure 34. Serial Port Mode 3

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Additional Features

The AUXR1 register contains several special purpose control bits that relate to several chip features. AUXR1 is described in Figure 37.

Software Reset

The SRST bit in AUXR1 allows software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. If a value is written to AUXR1 that contains a 1 at bit position 3, all SFRs will be initialized and execution will resume at program address 0000. Care should be taken when writing to AUXR1 to avoid accidental software resets.

Dual Data Pointers

The dual Data Pointer (DPTR) adds to the ways in which the processor can specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. The DPTR that is not currently selected is not accessible to software unless the DPS bit is toggled.

Specific instructions affected by the Data Pointer selection are:

- INC DPTR Increments the Data Pointer by 1.
- JMP @A+DPTR Jump indirect relative to DPTR value.

- MOV DPTR, #data16 Load the Data Pointer with a 16-bit constant.
- MOVC A, @A+DPTR Move code byte relative to DPTR to the accumulator.
- MOVX A, @DPTR Move data byte the accumulator to data memory relative to DPTR.
- MOVX @DPTR, A Move data byte from data memory relative to DPTR to the accumulator.

Also, any instruction that reads or manipulates the DPH and DPL registers (the upper and lower bytes of the current DPTR) will be affected by the setting of DPS. The MOVX instructions have limited application for the P87LPC767 since the part does not have an external data bus. However, they may be used to access EPROM configuration information (see EPROM Characteristics section).

Bit 2 of AUXR1 is permanently wired as a logic 0. This is so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

AUXR1	Address	: A2h									Reset Value: 00h
	Not Bit A	Addressable	9								
			7	6	5	4	3	2	1	0	
			KBF	BOD	BOI	LPEP	SRST	0	_	DPS	
		L									
Bľ	т	SYMBOL	FUI	NCTION							
AL	JXR1.7	KBF	Key fund	board Intertion goes	errupt Flag low. Must	. Set when a be cleared	any pin of p by softwar	port 0 tha e.	t is enabled	for the Ke	yboard Interrupt
AL	JXR1.6	BOD	Bro Mor	wn Out Di hitoring Fu	sable. Whe	en set, turns ction for de	s off brown tails.	out detec	tion and sav	ves power.	. See Power
AL	JXR1.5	BOI	Bro the sec	wn Out In brownout tion for de	terrupt. Wh detect fund tails.	nen set, prev ction to be u	vents brow ised as an	nout dete interrupt.	ction from c See the Po	ausing a owner Monit	chip reset and allows coring Functions
AL	JXR1.4	LPEP	Low only deta	/ Power E / be cleare ails.	PROM cor ed by powe	ntrol bit. Allo er-on or brow	ws power wnout rese	savings ir t. See the	n low voltage Power Rec	e systems Juction Mo	. Set by software. Can odes section for
AL	JXR1.3	SRST	Sof	tware Res	et. When s	set by softwa	are, resets	the P87L	.PC767 as i	f a hardwa	are reset occurred.
AL	JXR1.2	—	This inte	s bit conta rfering wit	ins a hard- h other bits	wired 0. All s in the regi	ows togglir ster.	ng of the I	DPS bit by ii	ncrementii	ng AUXR1, without
AL	JXR1.1	—	Res	served for	future use	. Should not	t be set to	1 by user	programs.		
AL	JXR1.0	DPS	Dat	a Pointer	Select. Ch	ooses one o	of two Data	Pointers	for use by t	he progra	m. See text for details.
											SU01639

Figure 37. AUXR1 Register

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Figure 39. EPROM System Configuration Byte 2 (UCFG2)

Security Bits

When neither of the security bits are programmed, the code in the EPROM can be verified. When only security bit 1 is programmed, all further programming of the EPROM is disabled. At that point, only security bit 2 may still be programmed. When both security bits are programmed, EPROM verify is also disabled.

Table 12. EPROM Security Bits

SB2	SB1	Protection Description
1	1	Both security bits unprogrammed. No program security features enabled. EPROM is programmable and verifiable.
1	0	Only security bit 1 programmed. Further EPROM programming is disabled. Security bit 2 may still be programmed.
0	1	Only security bit 2 programmed. This combination is not supported.
0	0	Both security bits programmed. All EPROM verification and programming are disabled.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Operating temperature under bias	–55 to +125	°C
Storage temperature range	-65 to +150	°C
Voltage on RST/V _{PP} pin to V _{SS}	0 to +11.0	V
Voltage on any other pin to V_{SS}	–0.5 to V _{DD} +0.5 V	V
Maximum I _{OL} per I/O pin	20	mA
Power dissipation (based on package heat transfer, not device power consumption)	1.5	W

NOTES:

 Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification are not implied.

2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.

