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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Active
Programmable Type	In System Programmable (min 10K program/erase cycles)
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	64
Number of Gates	-
Number of I/O	32
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/atf1504as-10ju44">https://www.e-xfl.com/product-detail/microchip-technology/atf1504as-10ju44</a>

## Enhanced Features

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- Improved Connectivity (Additional Feedback Routing, Alternate Input Routing)
- Output Enable Product Terms
- Transparent — Latch Mode
- Combinatorial Output with Registered Feedback within Any Macrocell
- Three Global Clock Pins
- ITD (Input Transition Detection) Circuits on Global Clocks, Inputs, and I/O
- Fast Registered Input from Product Term
- Programmable “Pin-keeper” Option
- $V_{CC}$  Power-up Reset Option
- Pull-up Option on JTAG Pins TMS and TDI
- Advanced Power Management Features
  - Edge-controlled Power-down “L”
  - Individual Macrocell Power Option
  - Disable ITD on Global Clocks, Inputs, and I/O

## Description

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The Atmel<sup>®</sup> ATF1504AS(L) is a high-performance, high-density Complex Programmable Logic Device (CPLD) which utilizes the Atmel proven electrically-erasable memory technology. With 64 logic macrocells and up to 68 inputs, it easily integrates logic from several TTL, SSI, MSI, LSI, and classic PLDs. The ATF1504AS(L) enhanced routing switch matrices increases usable gate count and the odds of successful pin-locked design modifications.

The ATF1504AS(L) has up to 68 bi-directional I/O pins and four dedicated input pins, depending on the type of device package selected. Each dedicated pin can also serve as a global control signal, register clock, register reset, or output enable. Each of these control signals can be selected for use individually within each macrocell.

Each of the 64 macrocells generates a buried feedback which goes to the global bus. Each input and I/O pin also feeds into the global bus. The switch matrix in each logic block then selects 40 individual signals from the global bus. Each macrocell also generates a foldback logic term which goes to a regional bus. Cascade logic between macrocells in the ATF1504AS(L) allows fast, efficient generation of complex logic functions. The ATF1504AS(L) contains four such logic chains; each capable of creating sum term logic with a fan-in of up to 40 product terms.

The ATF1504AS(L) macrocell, shown in [Figure 1](#), is flexible enough to support highly-complex logic functions operating at high speed. The macrocell consists of five sections:

- Product Terms and Product Term Select Multiplexer
- OR/XOR/CASCADE Logic
- Flip-flop
- Output Select and Enable
- Logic Array Inputs

### 3. Macrocell Sections

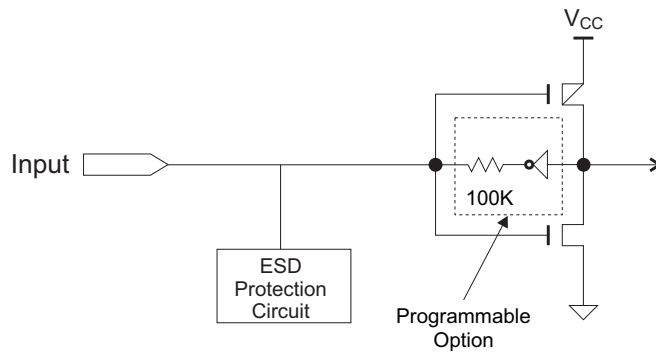
**Table 3-1. Macrocell Sections**

Section	Description
Product Terms and Select Mux	<p>Each ATF1504AS(L) macrocell has five product terms. Each product term receives as its possible inputs all signals from both the global bus and regional bus.</p> <p>The Product Term Select Multiplexer (PTMUX) allocates the five product terms as needed to the macrocell logic gates and control signals. The PTMUX programming is determined by the design compiler, which selects the optimum macrocell configuration.</p>
OR/XOR/CASCADE Logic	<p>The ATF1504AS(L) logic structure is designed to efficiently support all types of logic. Within a single macrocell, all the product terms can be routed to the OR gate, creating a 5-input AND/OR sum term. With the addition of the CASIN from neighboring macrocells, this can be expanded to as many as 40 product terms with a little small additional delay.</p> <p>The macrocell's XOR gate allows efficient implementation of compare and arithmetic functions. One input to the XOR comes from the OR sum term. The other XOR input can be a product term or a fixed high-level or low-level. For combinatorial outputs, the fixed level input allows polarity selection. For registered functions, the fixed levels allow DeMorgan minimization of product terms. The XOR gate is also used to emulate T-type and JK-type flip-flops.</p>
Flip-flop	<p>The ATF1504AS(L) flip-flop has very flexible data and control functions. The data input can come from either the XOR gate, from a separate product term, or directly from the I/O pin. Selecting the separate product term allows creation of a buried registered feedback within a combinatorial output macrocell. (This feature is automatically implemented by the fitter software). In addition to D, T, JK, and SR operation, the flip-flop can also be configured as a flow-through latch. In this mode, data passes through when the clock is high and is latched when the clock is low.</p> <p>The clock itself can either be one of the Global CLK Signals (GCK[0:2]) or an individual product term. The flip-flop changes state on the clock's rising edge. When the GCK signal is used as the clock, one of the macrocell product terms can be selected as a clock enable. When the clock enable function is active and the enable signal (product term) is low, all clock edges are ignored. The flip-flop's Asynchronous Reset signal (AR) can either be the Global Clear (GCLEAR), a product term, or always off. AR can also be a logic OR of GCLEAR with a product term. The Asynchronous Preset (AP) can be a product term or always off.</p>
Output Select and Enable	<p>The ATF1504AS(L) macrocell output can be selected as registered or combinatorial. The buried feedback signal can be either combinatorial or registered signal regardless of whether the output is combinatorial or registered.</p> <p>The output enable multiplexer (MOE) controls the output enable signals. Any buffer can be permanently enabled for simple output operation. Buffers can also be permanently disabled to allow use of the pin as an input. In this configuration all the macrocell resources are still available, including the buried feedback, expander, and CASCADE logic. The output enable for each macrocell can be selected as either of the two dedicated OE input pins as an I/O pin configured as an input, or as an individual product term.</p>
Global Bus/Switch Matrix	<p>The global bus contains all input and I/O pin signals, as well as, the buried feedback signal from all 64 macrocells. The switch matrix in each logic block receives as its possible inputs all signals from the global bus. Under software control, up to 40 of these signals can be selected as inputs to the logic block.</p>
Foldback Bus	<p>Each macrocell also generates a foldback product term. This signal goes to the regional bus and is available to four macrocells. The foldback is an inverse polarity of one of the macrocell's product terms. The sixteen foldback terms in each region allow generation of high fan-in sum terms (up to sixteen product terms) with a nominal additional delay.</p>

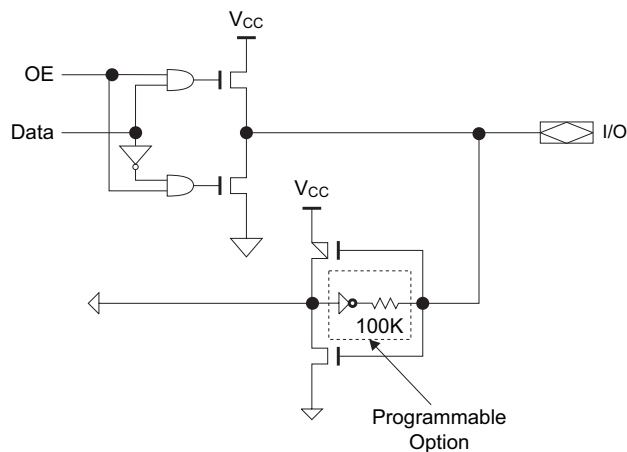
## 4. Programmable Pin-keeper Option for Inputs and I/Os

The ATF1504AS(L) offers the option of programming all input and I/O pins so the pin-keeper circuits can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high-level or low-level. This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

**Figure 4-1. Input Diagram**



**Figure 4-2. I/O Diagram**



## 5. Speed/Power Management

The ATF1504AS(L) has several built-in speed and power management features. The ATF1504AS(L) contains circuitry which automatically puts the device into a low-power standby mode when no logic transitions are occurring. This not only reduces power consumption during inactive periods, but also provides proportional power savings for most applications running at system speeds below 5MHz. This feature may be selected as a device option.

To further reduce power, each ATF1504AS(L) macrocell has a Reduced Power bit feature. This feature allows individual macrocells to be configured for maximum power savings. This feature may be selected as a design option.

All ATF1504AS(L) have an optional power-down mode. In this mode, current drops to below 10mA. When the power-down option is selected, either PD1 or PD2 pins (or both) can be used to power-down the part. The power-down option is selected in the design source file. When enabled, the device goes into power-down when either PD1 or PD2 is high. In the power-down mode, all internal logic signals are latched and held, as are any enabled outputs.

All pin transitions are ignored until the PD pin is brought low. When the power-down feature is enabled, the PD1 or PD2 pin cannot be used as a logic input or output; however, the pin's macrocell may still be used to generate buried foldback and cascade logic signals.

All power-down AC characteristic parameters are computed from external input or I/O pins, with Reduced Power bit turned on. For macrocells in reduced-power mode (Reduced Power bit turned on), the reduced-power adder,  $t_{RPA}$ , must be added to the AC parameters, which include the data paths  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{ACL}$ ,  $t_{ACH}$ , and  $t_{SEXP}$ .

The ATF1504AS(L) macrocell also has an option whereby the power can be reduced on a per macrocell basis. By enabling this power-down option, macrocells that are not used in an application can be turned-down, thereby reducing the overall power consumption of the device.

Each output also has individual slew rate control. This may be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed. Outputs default to slow switching, and may be specified as fast switching in the design file.

## 6. Design Software Support

ATF1504AS(L) designs are supported by several industry-standard third-party tools. Automated fitters allow logic synthesis using a variety of high level description languages and formats.

## 7. Power-up Reset

The ATF1504AS(L) is designed with a power-up reset, a feature critical for state machine initialization. At a point delayed slightly from  $V_{CC}$  crossing  $V_{RST}$ , all registers will be initialized, and the state of each output will depend on the polarity of its buffer. However, due to the asynchronous nature of reset and uncertainty of how  $V_{CC}$  actually rises in the system, the following conditions are required:

- The  $V_{CC}$  rise must be monotonic,
- After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and,
- The clock must remain stable during  $T_D$ .

The ATF1504AS(L) has two options for the hysteresis about the reset level,  $V_{RST}$ , Small and Large. During the fitting process users may configure the device with the Power-up Reset hysteresis set to Large or Small. Atmel POF2JED users may select the Large option by including the flag "-power\_reset" on the command line after "filename.POF". To allow the registers to be properly reinitialized with the Large hysteresis option selected, the following condition is added:

- If  $V_{CC}$  falls below 2.0V, it must shut off completely before the device is turned on again.

When the Large hysteresis option is active,  $I_{CC}$  is reduced by several hundred micro amps as well.

## 8. Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF1504AS(L) fuse patterns. Once programmed, fuse verify is inhibited; however, the 16-bit User Signature remains accessible.

## 9. Programming

ATF1504AS(L) devices are In-System Programmable (ISP) devices utilizing the 4-pin JTAG protocol. This capability eliminates package handling normally required for programming and facilitates rapid design iterations and field changes.

Atmel provides ISP hardware and software to allow programming of the ATF1504AS(L) via the PC. ISP is performed by using either a download cable or a comparable board tester or a simple microprocessor interface.

To facilitate ISP programming by the Automated Test Equipment (ATE) vendors. Serial Vector Format (SVF) files can be created by Atmel provided software utilities.

ATF1504AS(L) devices can also be programmed using standard third-party programmers. With third-party programmer, the JTAG ISP port can be disabled thereby allowing four additional I/O pins to be used for logic.

Contact your local Atmel representatives or Atmel PLD applications for details.

## 10. ISP Programming Protection

The ATF1504AS(L) has a special feature which locks the device and prevents the inputs and I/O from driving if the programming process is interrupted for any reason. The inputs and I/O default to high-Z state during such a condition. In addition, the pin-keeper option preserves the former state during device programming if this circuit were previously programmed on the device. This prevents disturbing the operation of other circuits in the system while the ATF1504AS(L) is being programmed via ISP.

All ATF1504AS(L) devices are initially shipped in the erased state thereby making them ready to use for ISP.

Note: For more information refer to the “Designing for In-System Programmability with Atmel CPLDs” application note.

## 11. Electrical Characteristics

### 11.1 Absolute Maximum Ratings\*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V <sup>(1)</sup>
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V <sup>(1)</sup>
Programming Voltage with Respect to Ground	-2.0V to +14.0V <sup>(1)</sup>

\*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.60VDC, which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is  $V_{CC} + 0.75\text{VDC}$ , which may overshoot to 7.0V for pulses of less than 20ns.

### 11.2 Pin Capacitance

Table 11-1. Pin Capacitance<sup>(1)</sup>

	Typ	Max	Units	Conditions
$C_{IN}$	8	10	pF	$V_{IN} = 0\text{V}$ ; $f = 1\text{MHz}$
$C_{I/O}$	8	10	pF	$V_{OUT} = 0\text{V}$ ; $f = 1\text{MHz}$

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested. The OGI pin (high-voltage pin during programming) has a maximum capacitance of 12pF.

### 11.3 DC and AC Operating Conditions

Table 11-2. DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient)	0°C to 70°C	-40°C to 85°C
$V_{CCINT}$ or $V_{CCIO}$ (5.0V) Power Supply	5.0V $\pm$ 5%	5.0V $\pm$ 10%
$V_{CCIO}$ (3.3V) Power Supply	3.0V to 3.6V	3.0V to 3.6V

## 11.4 DC Characteristics

Table 11-3. DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I <sub>IL</sub>	Input or I/O Low Leakage Current	V <sub>IN</sub> = V <sub>CC</sub>				-2	-10	μA
I <sub>IH</sub>	Input or I/O High Leakage Current					2	10	
I <sub>OZ</sub>	Tri-state Output Off-state Current	V <sub>O</sub> = V <sub>CC</sub> or GND			-40		40	μA
I <sub>CC1</sub>	Power Supply Current, Standby	V <sub>CC</sub> = Max V <sub>IN</sub> = 0, V <sub>CC</sub>	Std Mode	Com.		105		mA
				Ind.		130		mA
			“L” Mode	Com.		10		μA
				Ind.		10		μA
I <sub>CC2</sub>	Power Supply Current, Power-down Mode	V <sub>CC</sub> = Max V <sub>IN</sub> = 0, V <sub>CC</sub>	“PD” Mode			1	10	mA
I <sub>CC3</sub> <sup>(2)</sup>	Current in Reduced-power Mode	V <sub>CC</sub> = Max V <sub>IN</sub> = 0, V <sub>CC</sub>	Std Power	Com		85		ma
				Ind		105		
V <sub>CCIO</sub>	Supply Voltage	5.0V Device Output		Com.	4.75		5.25	V
				Ind.	4.50		5.50	V
V <sub>CCIO</sub>	Supply Voltage	3.3V Device Output			3.00		3.60	V
V <sub>IL</sub>	Input Low Voltage				-0.30		0.80	V
V <sub>IH</sub>	Input High Voltage				2.00		V <sub>CCIO</sub> + 0.3	V
V <sub>OL</sub>	Output Low Voltage (TTL)	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>CCIO</sub> = Min, I <sub>OL</sub> = 12mA		Com.			0.45	V
				Ind.				
	Output Low Voltage (CMOS)	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>CC</sub> = Min, I <sub>OL</sub> = 0.1mA		Com.			0.20	V
				Ind.			0.20	V
V <sub>OH</sub>	Output High Voltage (TTL)	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>CCIO</sub> = Min, I <sub>OH</sub> = -4.0mA			2.4			V

- Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30s.  
2. When macrocell reduced-power feature is enabled.



## 11.5 AC Characteristics

Table 11-4. AC Characteristics<sup>(1)(2)</sup>

Symbol	Parameter	-7		-10		-25		Units
		Min	Max	Min	Max	Min	Max	
$t_{PD1}$	Input or Feedback to Non-registered Output		7.5		10		25	ns
$t_{PD2}$	I/O Input or Feedback to Non-registered Feedback		7		9		25	ns
$t_{SU}$	Global Clock Setup Time	6		7		20		ns
$t_H$	Global Clock Hold Time	0		0		0		ns
$t_{FSU}$	Global Clock Setup Time of Fast Input	3		3		5		ns
$t_{FH}$	Global Clock Hold Time of Fast Input	0.5		0.5		2		ns
$t_{COP}$	Global Clock to Output Delay		4.5		5		13	ns
$t_{CH}$	Global Clock High Time	3		4		7		ns
$t_{CL}$	Global Clock Low Time	3		4		7		ns
$t_{ASU}$	Array Clock Setup Time	3		3		5		ns
$t_{AH}$	Array Clock Hold Time	2		3		6		ns
$t_{ACOP}$	Array Clock Output Delay		7.5		10		25	ns
$t_{ACH}$	Array Clock High Time	3		4		10		ns
$t_{ACL}$	Array Clock Low Time	3		4		10		ns
$t_{CNT}$	Minimum Clock Global Period		8		10		22	ns
$f_{CNT}$	Maximum Internal Global Clock Frequency	125		100		50		MHz
$t_{ACNT}$	Minimum Array Clock Period		8		10		22	ns
$f_{ACNT}$	Maximum Internal Array Clock Frequency	125		100		50		MHz
$f_{MAX}$	Maximum Clock Frequency	166.7		125		60		MHz
$t_{IN}$	Input Pad and Buffer Delay		0.5		0.5		2	ns
$t_{IO}$	I/O Input Pad and Buffer Delay		0.5		0.5		2	ns
$t_{FIN}$	Fast Input Delay		1		1		2	ns
$t_{SEXP}$	Foldback Term Delay		4		5		12	ns
$t_{PEXP}$	Cascade Logic Delay		0.8		0.8		1.2	ns
$t_{LAD}$	Logic Array Delay		3		5		8	ns

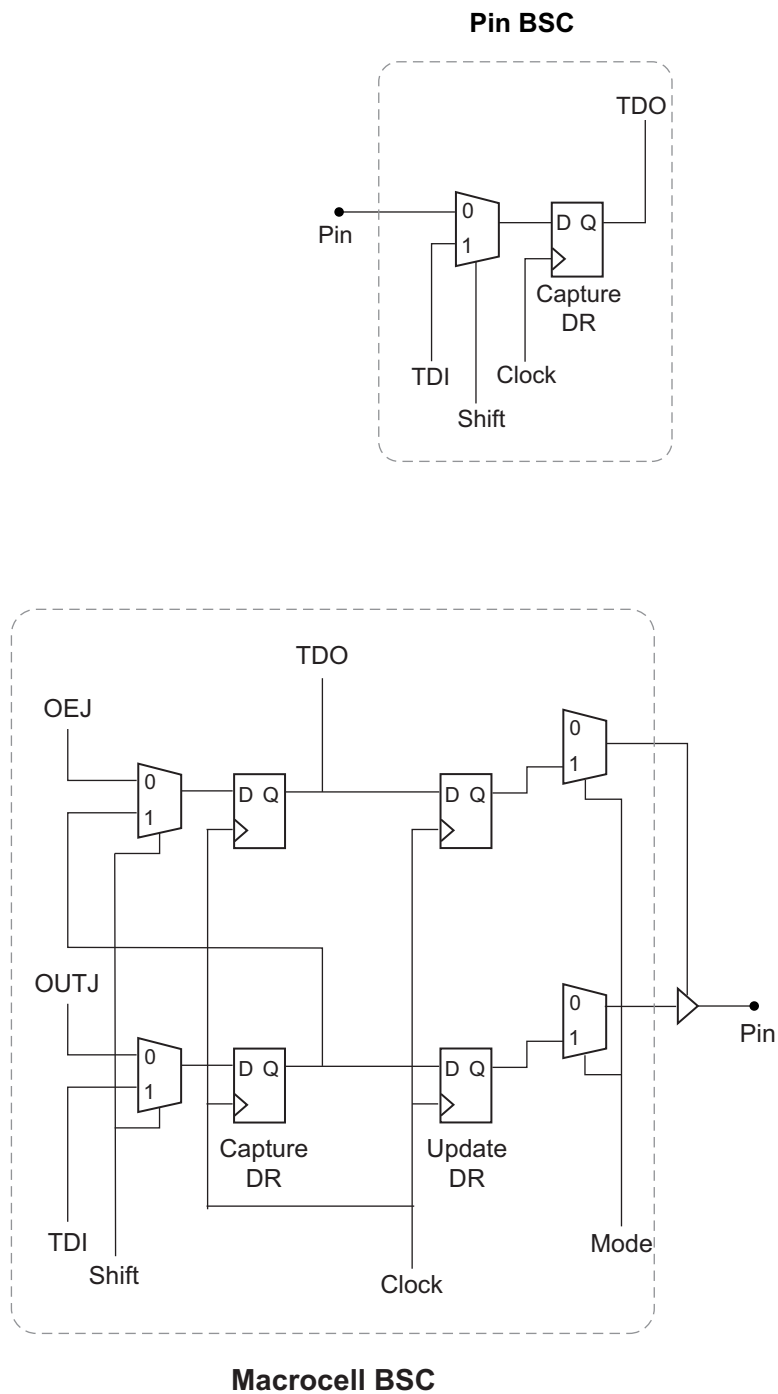
- Notes: 1. See ordering information for valid part numbers.  
2. The  $t_{RPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{TIC}$ ,  $t_{ACL}$ , and  $t_{SEXP}$  parameters for macrocells running in the reduced-power mode.

**Table 11-4. AC Characteristics<sup>(1)(2)</sup> (Continued)**

Symbol	Parameter	-7		-10		-25		Units
		Min	Max	Min	Max	Min	Max	
t <sub>LAC</sub>	Logic Control Delay		3		5		8	ns
t <sub>IOE</sub>	Internal Output Enable Delay		2		2		4	ns
t <sub>OD1</sub>	Output Buffer and Pad Delay (Slow slew rate = OFF; V <sub>CCIO</sub> = 5.0V; C <sub>L</sub> = 35pF)		2		1.5		6	ns
t <sub>OD2</sub>	Output Buffer and Pad Delay (Slow slew rate = OFF; V <sub>CCIO</sub> = 3.3V; C <sub>L</sub> = 35pF)		2.5		2.0		7	ns
t <sub>OD3</sub>	Output Buffer and Pad Delay (Slow slew rate = ON; V <sub>CCIO</sub> = 5.0V or 3.3V; C <sub>L</sub> = 35pF)		5		5.5		10	ns
t <sub>ZX1</sub>	Output Buffer Enable Delay (Slow slew rate = OFF; V <sub>CCIO</sub> = 5.0V; C <sub>L</sub> = 35pF)		4.0		5.0		10	ns
t <sub>ZX2</sub>	Output Buffer Enable Delay (Slow slew rate = OFF; V <sub>CCIO</sub> = 3.3V; C <sub>L</sub> = 35pF)		4.5		5.5		10	ns
t <sub>ZX3</sub>	Output Buffer Enable Delay (Slow slew rate = ON; V <sub>CCIO</sub> = 5.0V/3.3V; C <sub>L</sub> = 35pF)		9		9		12	ns
t <sub>XZ</sub>	Output Buffer Disable Delay (C <sub>L</sub> = 5pF)		4		5		8	ns
t <sub>SU</sub>	Register Setup Time	3		3		6		ns
t <sub>H</sub>	Register Hold Time	2		3		6		ns
t <sub>FSU</sub>	Register Setup Time of Fast Input	3		3		3		ns
t <sub>FH</sub>	Register Hold Time of Fast Input	0.5		0.5		2.5		ns
t <sub>RD</sub>	Register Delay		1		2		2	ns
t <sub>COMB</sub>	Combinatorial Delay		1		2		2	ns
t <sub>IC</sub>	Array Clock Delay		3		5		8	ns
t <sub>EN</sub>	Register Enable Time		3		5		8	ns
t <sub>GLOB</sub>	Global Control Delay		1		1		1	ns
t <sub>PRE</sub>	Register Preset Time		2		3		6	ns
t <sub>CLR</sub>	Register Clear Time		2		3		6	ns
t <sub>UIM</sub>	Switch Matrix Delay		1		1		2	ns
t <sub>RPA</sub>	Reduced-power Adder <sup>(2)</sup>		10		11		15	ns

- Notes:
1. See ordering information for valid part numbers.
  2. The t<sub>RPA</sub> parameter must be added to the t<sub>LAD</sub>, t<sub>LAC</sub>, t<sub>TIC</sub>, t<sub>ACL</sub>, and t<sub>SEXP</sub> parameters for macrocells running in the reduced-power mode.

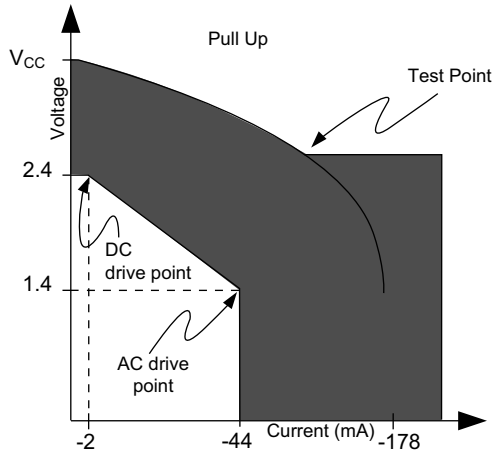
**Figure 14-2. BSC Configuration for Macrocell**



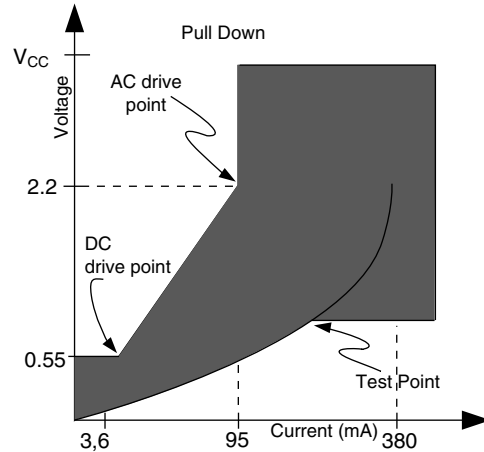
## 15. PCI Compliance

The ATF1504AS(L) supports the growing need in the industry to support the new Peripheral Component Interconnect (PCI) interface standard in PCI-based designs and specifications. The PCI interface calls for high current drivers, which are much larger than the traditional TTL drivers. In general, PLDs and FPGAs parallel outputs to support the high current load required by the PCI interface. The ATF1504AS(L) allows this without contributing to system noise while delivering low output-to-output skew. Having a programmable high drive option is also possible without increasing output delay or pin capacitance.

**Figure 15-1. PCI Voltage-to-current Curves for +5.0V Signaling in Pull-up Mode**



**Figure 15-2. PCI Voltage-to-current Curves for +5.0V Signaling in Pull-down Mode**



**Table 15-1. PCI DC Characteristics**

Symbol	Parameter	Conditions	Min	Max	Units
$V_{CC}$	Supply Voltage		4.75	5.25	V
$V_{IH}$	Input High Voltage		2.0	$V_{CC} + 0.5$	V
$V_{IL}$	Input Low Voltage		-0.5	0.8	V
$I_{IH}$	Input High Leakage Current	$V_{IN} = 2.7V$		70	$\mu A$
$I_{IL}$	Input Low Leakage Current	$V_{IN} = 0.5V$		-70	$\mu A$
$V_{OH}$	Output High Voltage	$I_{OUT} = -2mA$	2.4		V
$V_{OL}$	Output Low Voltage	$I_{OUT} = 3mA, 6mA$		0.55	V
$C_{IN}$	Input Pin Capacitance			10	pF
$C_{CLK}$	CLK Pin Capacitance			12	pF
$C_{IDSEL}$	IDSEL Pin Capacitance			8	pF
$L_{PIN}$	Pin Inductance			20	nH

Note: 1. Leakage current is with pin-keeper off.

**Table 15-2. PCI AC Characteristics**

Symbol	Parameter	Conditions	Min	Max	Units
$I_{OH(AC)}$	Switching Current High (Test High)	$0 < V_{OUT} \leq 1.4$	-44		mA
		$1.4 < V_{OUT} < 2.4$	$-44 + (V_{OUT} - 1.4)/0.024$		mA
		$3.1 < V_{OUT} < V_{CC}$		Equation A	mA
		$V_{OUT} = 3.1V$		-142	$\mu A$
$I_{OL(AC)}$	Switching Current Low (Test Point)	$V_{OUT} > 2.2V$	95		mA
		$2.2 > V_{OUT} > 0$	$V_{OUT}/0.023$		mA
		$0.1 > V_{OUT} > 0$		Equation B	mA
		$V_{OUT} = 0.71$		206	mA
$I_{CL}$	Low Clamp Current	$-5 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$		mA
$SLEW_R$	Output Rise Slew Rate	0.4V to 2.4V load	0.5	3	V/ns
$SLEW_F$	Output Fall Slew Rate	2.4V to 0.4V load	0.5	3	V/ns

Notes: 1. Equation A:  $I_{OH} = 11.9 (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$  for  $V_{CC} > V_{OUT} > 3.1V$ .  
2. Equation B:  $I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$  for  $0V < V_{OUT} < 0.71V$ .

## 16. Pinouts

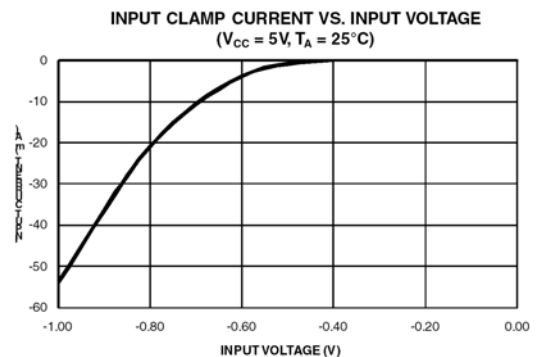
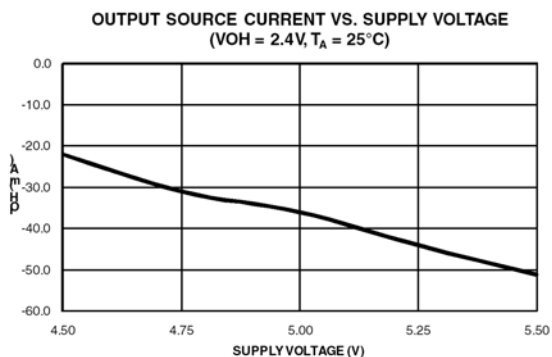
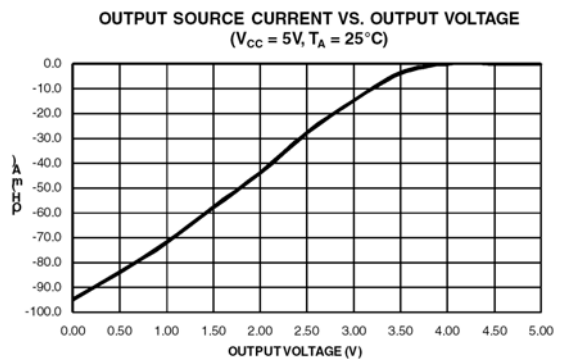
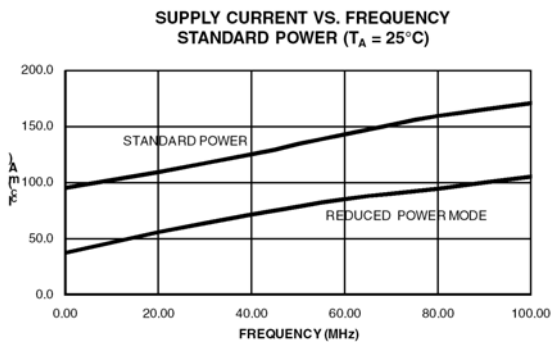
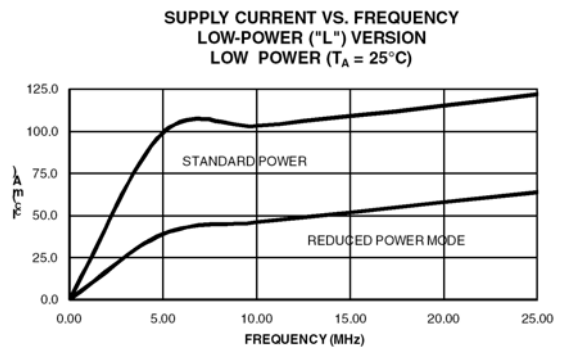
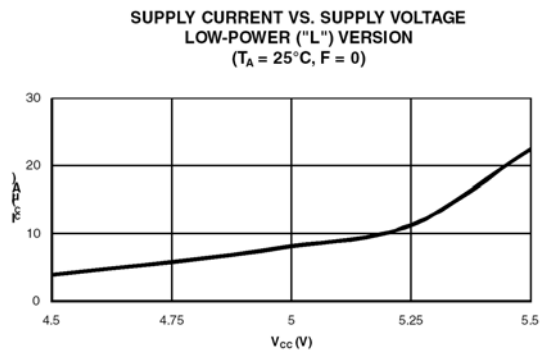
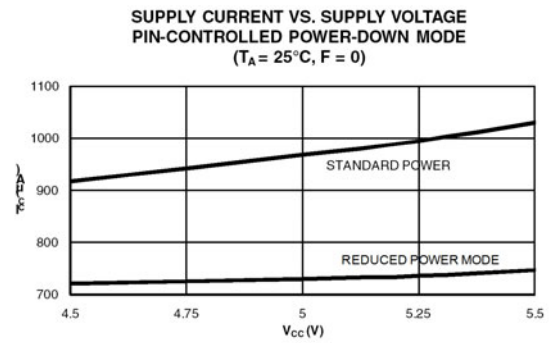
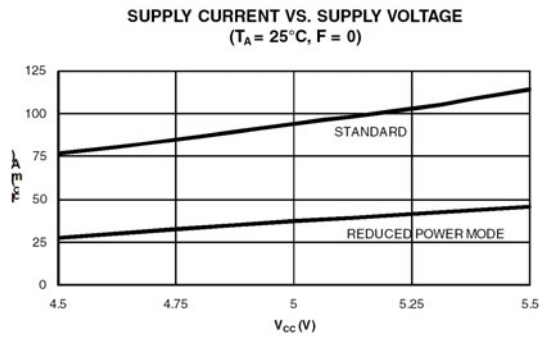
### 16.1 ATF1504AS(L) Dedicated Pinouts

Dedicated Pin	44-lead TQFP	44-lead J-lead	84-lead J-lead	100-lead TQFP
INPUT/OE2/GCLK2	40	2	2	90
INPUT/GCLR	39	1	1	89
INPUT/OE1	38	44	84	88
INPUT/GCLK1	37	43	83	87
I/O /GCLK3	35	41	81	85
I/O/PD (1,2)	5, 19	11, 25	20, 46	12, 42
I/O/TDI (JTAG)	1	7	14	4
I/O/TMS (JTAG)	7	13	23	15
I/O/TCK (JTAG)	26	32	62	62
I/O/TDO (JTAG)	32	38	71	73
GND	4, 16, 24, 36	10, 22, 30, 42	7, 19, 32, 42, 47, 59, 72, 82	11, 26, 38, 43, 59, 74, 86, 95
V <sub>CCINT</sub>	9, 17, 29, 41	3, 15, 23, 35	3, 43	39, 91
V <sub>CCIO</sub>	—	—	13, 26, 38, 53, 66, 78	3, 18, 34, 51, 66, 82
N/C	—	—	—	1, 2, 5, 7, 22, 24, 27, 28, 49, 50, 53, 55, 70, 72, 77, 78
# of Signal Pins	36	36	68	68
# User I/O Pins	32	32	64	64

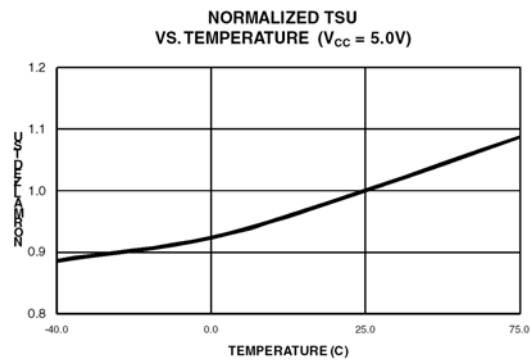
Note: OE (1, 2) . . . . . Global OE Pins  
 GCLR . . . . . Global Clear Pin  
 GCLK (1, 2, 3) . . . . . Global Clock Pins  
 PD (1, 2) . . . . . Power-down pins  
 TDI, TMS, TCK, TDO . . . JTAG pins used for boundary-scan testing or in-system programming  
 GND . . . . . Ground Pins  
 V<sub>CCINT</sub> . . . . . V<sub>CC</sub> pins for the device (+5V - Internal)  
 V<sub>CCIO</sub> . . . . . V<sub>CC</sub> pins for output drivers (for I/O pins) (+5V or 3.3V - I/Os)

## 16.2 ATF1504AS(L) I/O Pinouts

MC	PLC	44-lead PLCC	44-lead TQFP	84-lead PLCC	100-lead TQFP	MC	PLC	44-lead PLCC	44-lead TQFP	84-lead PLCC	100-lead TQFP
1	A	12	6	22	14	33	C	24	18	44	40
2	A	—	—	21	13	34	C	—	—	45	41
3	A/PD1	11	5	20	12	35	C/PD2	25	19	46	42
4	A	9	3	18	10	36	C	26	20	48	44
5	A	8	2	17	9	37	C	27	21	49	45
6	A	—	—	16	8	38	C	—	—	50	46
7	A	—	—	15	6	39	C	—	—	51	47
8/TDI	A	7	1	14	4	40	C	28	22	52	48
9	A	—	—	12	100	41	C	29	23	54	52
10	A	—	—	11	99	42	C	—	—	55	54
11	A	6	44	10	98	43	C	—	—	56	56
12	A	—	—	9	97	44	C	—	—	57	57
13	A	—	—	8	96	45	C	—	—	58	58
14	A	5	43	6	94	46	C	31	25	60	60
15	A	—	—	5	93	47	C	—	—	61	61
16	A	4	42	4	92	48/TCK	C	32	26	62	62
17	B	21	15	41	37	49	D	33	27	63	63
18	B	—	—	40	36	50	D	—	—	64	64
19	B	20	14	39	35	51	D	34	28	65	65
20	B	19	13	37	33	52	D	36	30	67	67
21	B	18	12	36	32	53	D	37	31	68	68
22	B	—	—	35	31	54	D	—	—	69	69
23	B	—	—	34	30	55	D	—	—	70	71
24	B	17	11	33	29	56/TDO	D	38	32	71	73
25	B	16	10	31	25	57	D	39	33	73	75
26	B	—	—	30	23	58	D	—	—	74	76
27	B	—	—	29	21	59	D	—	—	75	79
28	B	—	—	28	20	60	D	—	—	76	80
29	B	—	—	27	19	61	D	—	—	77	81
30	B	14	8	25	17	62	D	40	34	79	83
31	B	—	—	24	16	63	D	—	—	80	84
32/TMS	B	13	7	23	15	64	D/GCLK3	41	35	81	85

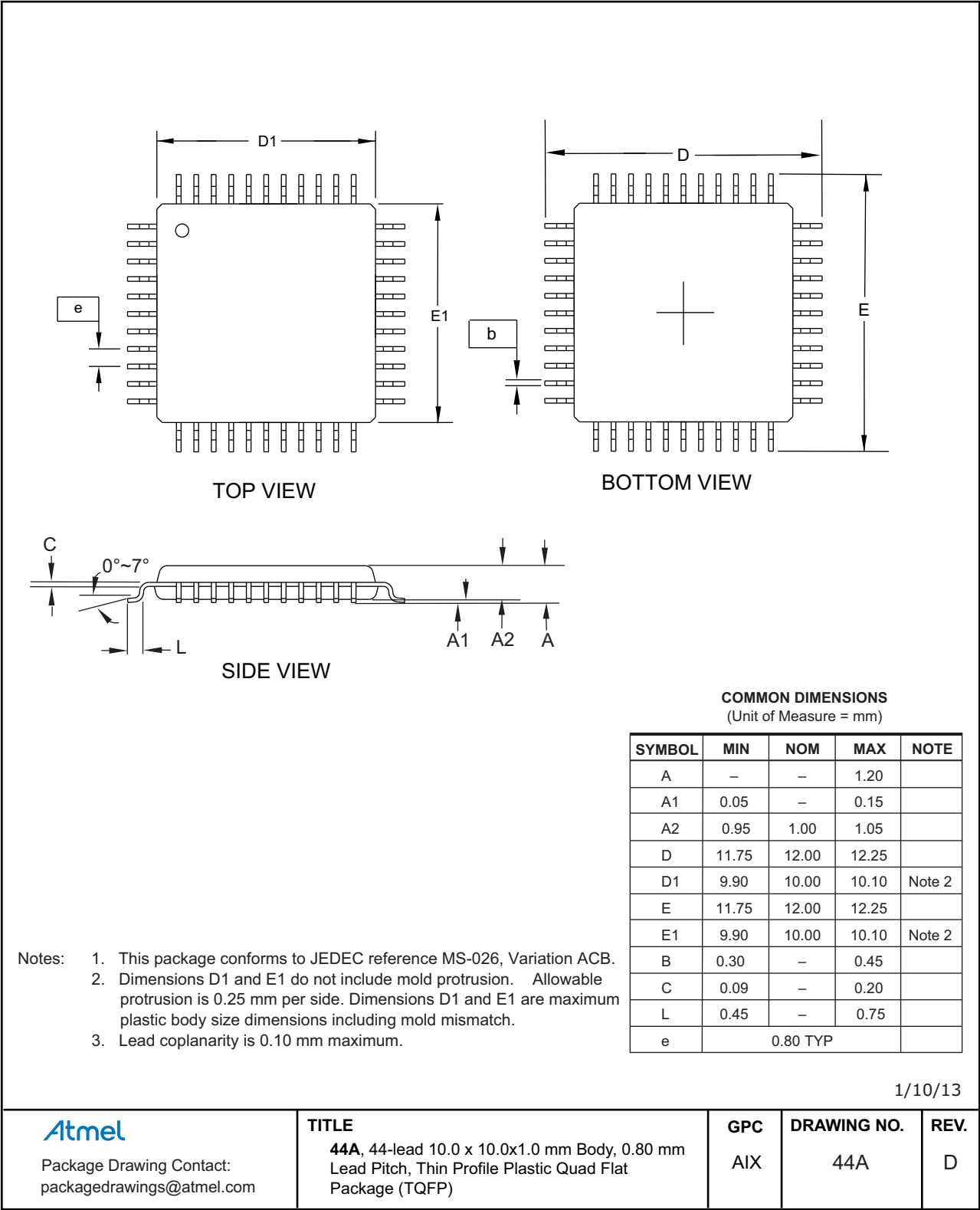




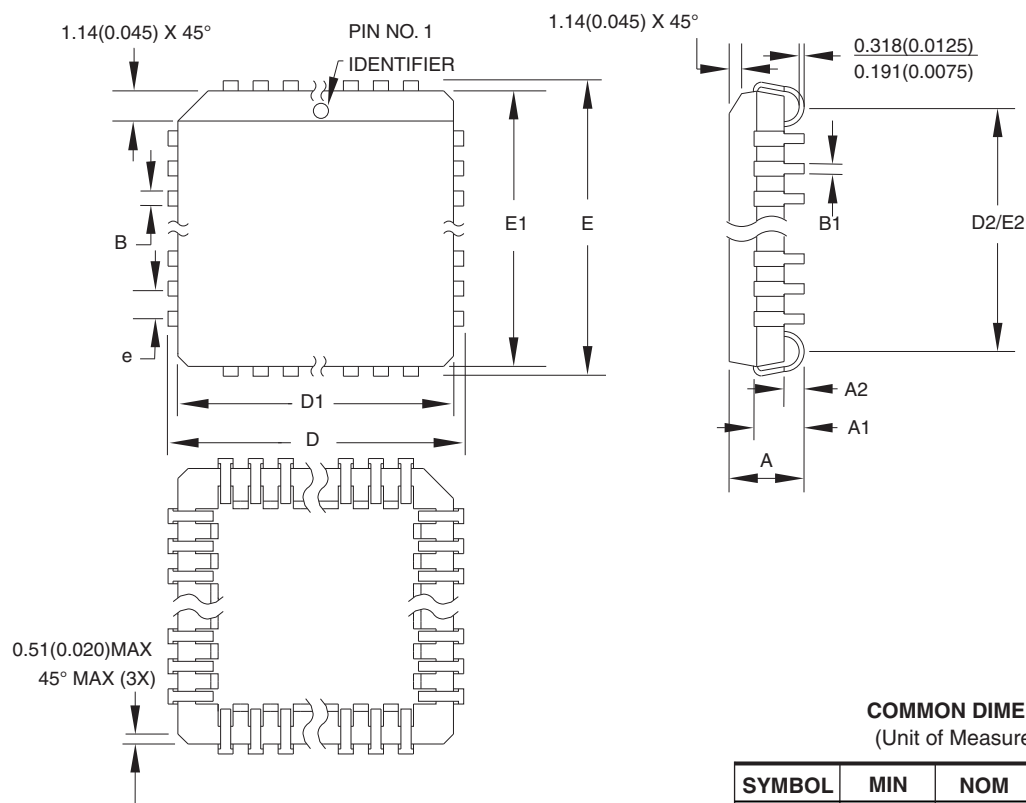


18. Packaging Information

18.1 44A — 44-lead TQFP



## 18.2 44J — 44-lead PLCC



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	—	4.572	
A1	2.286	—	3.048	
A2	0.508	—	—	
D	17.399	—	17.653	
D1	16.510	—	16.662	Note 2
E	17.399	—	17.653	
E1	16.510	—	16.662	Note 2
D2/E2	14.986	—	16.002	
B	0.660	—	0.813	
B1	0.330	—	0.533	
e	1.270 TYP			

- Notes: 1. This package conforms to JEDEC reference MS-018, Variation AC.  
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.  
 3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

**Atmel**

Package Drawing Contact:  
packagedrawings@atmel.com

**TITLE**

**44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)**

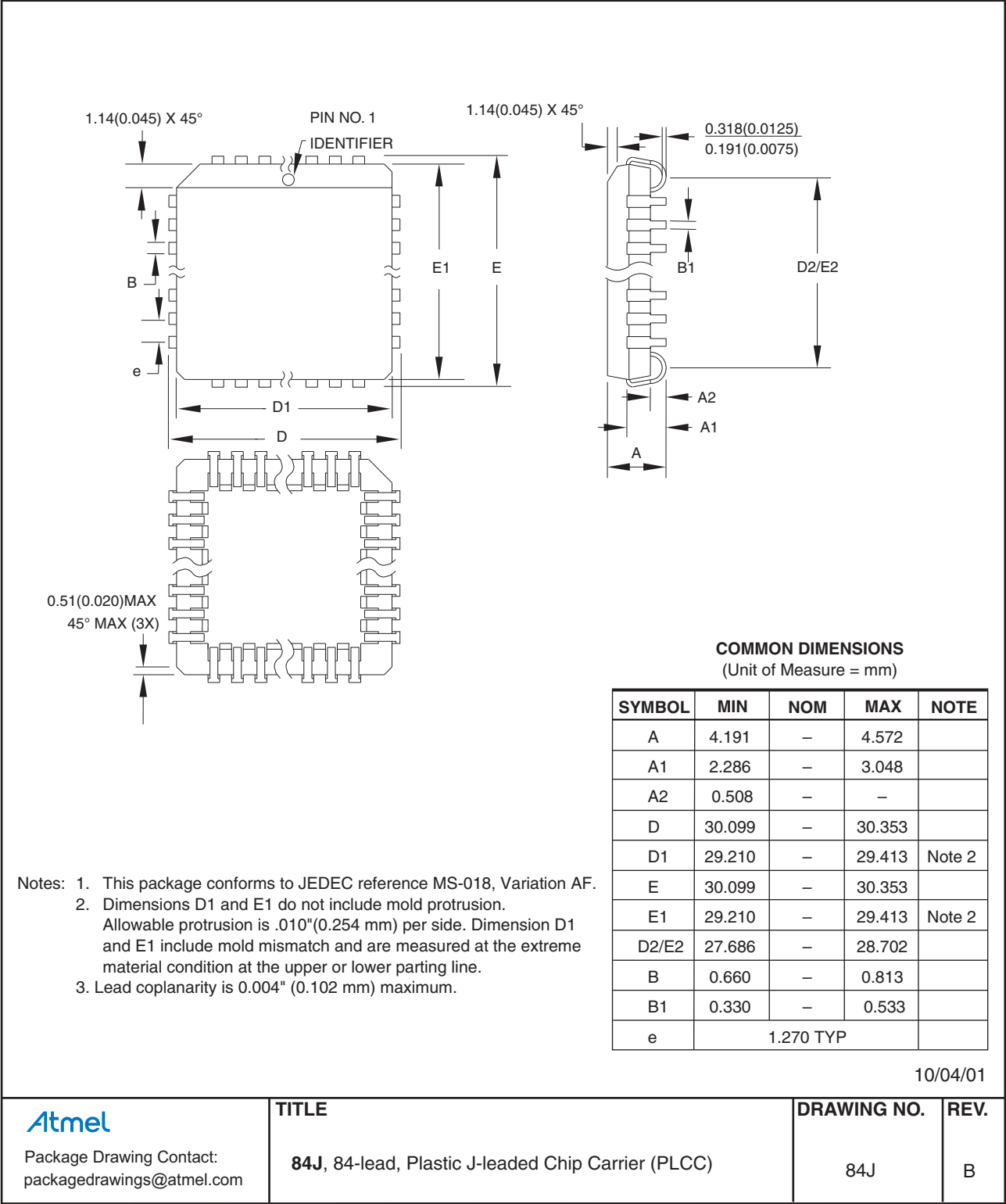
**DRAWING NO.**

44J

**REV.**

B

18.3 84J — 84-lead PLCC



## 18.4 100A — 100-lead TQFP

