Renesas Electronics America Inc - R5F212G6SNFP#W4 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	8MHz
Connectivity	LINbus, SIO, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	27
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212g6snfp-w4

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1.2 Product List

Table 1.2 lists Product List for R8C/2G Group, Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/2G Group.

Table 1.2 Product List for R8C/2G Group **Current of Apr. 2008**

Part No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F212G4SNFP	16 Kbytes	512 bytes	PLQP0032GB-A	N version
R5F212G5SNFP	24 Kbytes	1 Kbytes	PLQP0032GB-A	
R5F212G6SNFP	32 Kbytes	1 Kbytes	PLQP0032GB-A	
R5F212G4SDFP	16 Kbytes	512 bytes	PLQP0032GB-A	D version
R5F212G5SDFP	24 Kbytes	1 Kbytes	PLQP0032GB-A	
R5F212G6SDFP	32 Kbytes	1 Kbytes	PLQP0032GB-A	

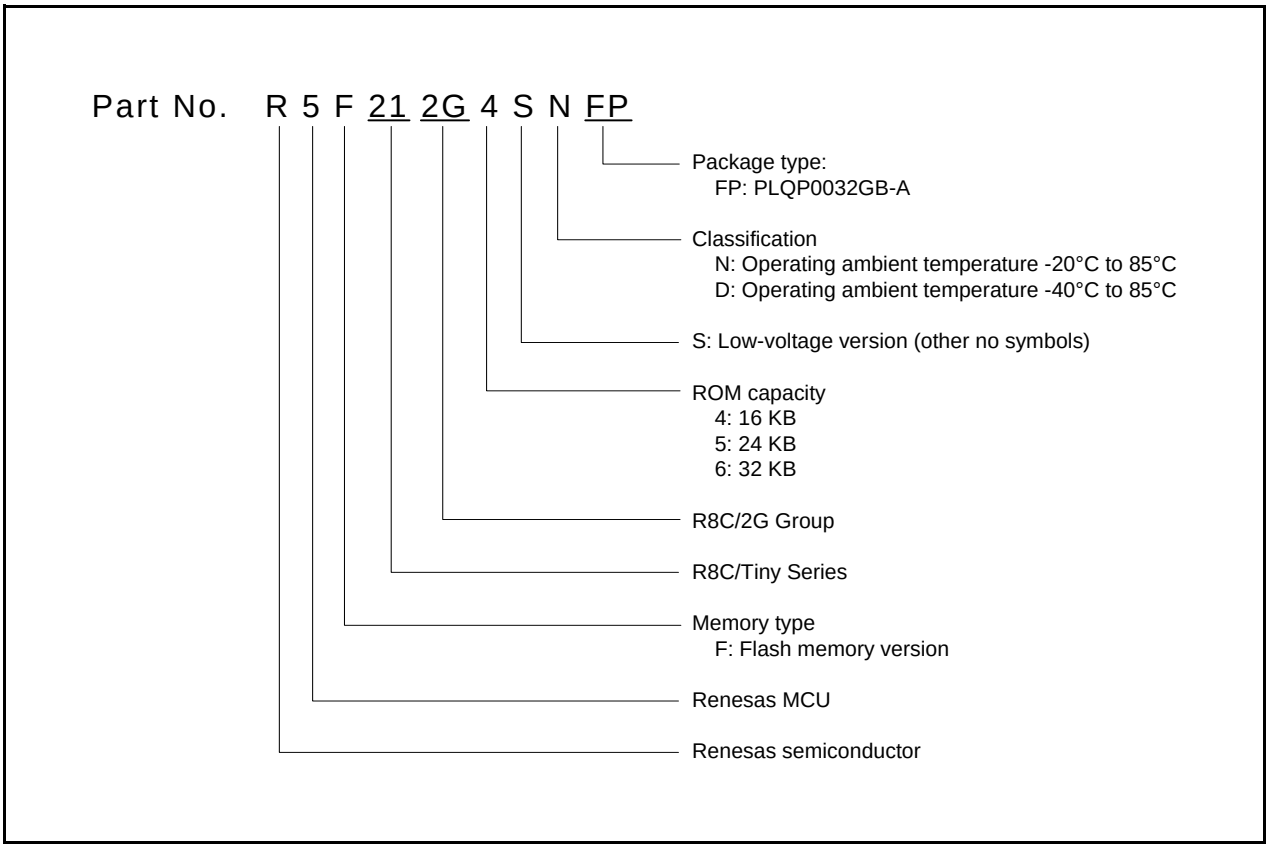


Figure 1.1 Part Number, Memory Size, and Package of R8C/2G Group

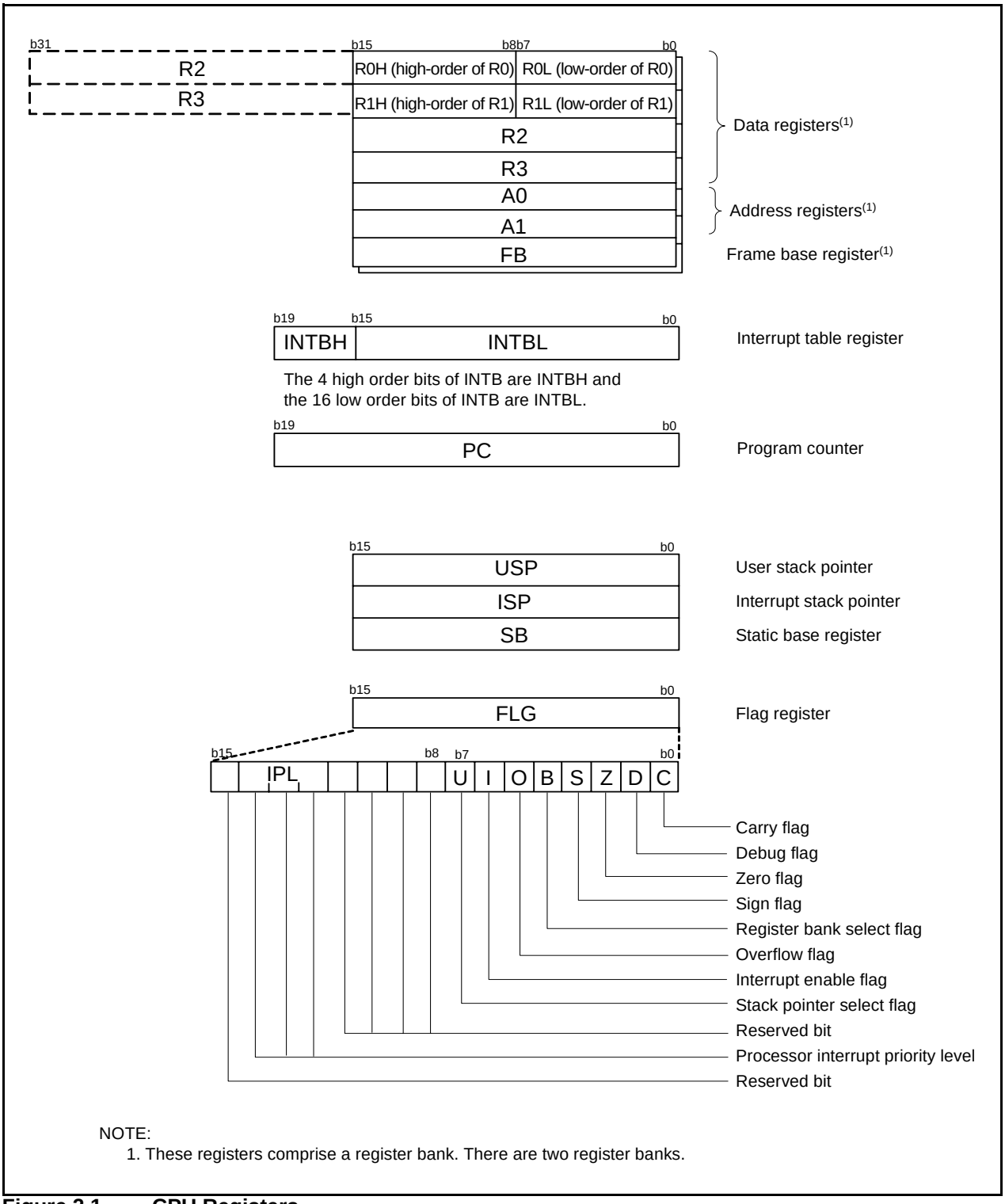
Table 1.3 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules			
			Interrupt	Timer	Serial Interface	Comparator
1		P3_5		TRFO12		
2		P3_7		(TRAO)/(TRFO11)(1)		
3	$\overline{\text{RESET}}$					
4	XCOUT	(P4_4)				
5	VSS					
6	XCIN	(P4_3)				
7	VCC					
8	MODE					
9		P4_5	$\overline{\text{INT0}}$			
10		P1_7	$\overline{\text{INT1}}$	TRAIO		
11		P3_6	($\overline{\text{INT1}}$)(1)			
12		P3_1		TRBO		
13		P3_0		TRAO		
14		P3_2	$\overline{\text{INT2}}$			
15		P1_6			CLK0	VCOUT2
16		P1_5	($\overline{\text{INT1}}$)(1)	(TRAIO)(1)	RXD0	
17		P1_4			TXD0	
18		P1_3	$\overline{\text{KI3}}$	(TRBO)(1)		VCOUT1
19		P1_2	$\overline{\text{KI2}}$	TRFO02		CVREF
20		P6_5		(TREO)(1)	CLK2	
21		P1_1	$\overline{\text{KI1}}$	TRFO01		VCMP2
22		P1_0	$\overline{\text{KI0}}$	TRFO00		VCMP1
23		P3_3		TRFO10/TRFI		
24		P3_4		TRFO11		
25		P0_7	($\overline{\text{KI0}}$)(1)			
26		P0_6	$\overline{\text{INT4}}$			
27		P0_5				
28		P0_4		(TREO)(1)		
29		P6_3			TXD2	
30		P6_0		TREO		
31		P6_6	($\overline{\text{KI1}}$)(1)			
32		P6_4			RXD2	

NOTE:
1. Can be assigned to the pin in parentheses by a program.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



NOTE:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

Table 4.6 SFR Information (6)(1)

Address	Register	Symbol	After reset
0130h			
0131h			
0132h			
0133h			
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h	UART2 Transmit/Receive Mode Register	U2MR	00h
0161h	UART2 Bit Rate Register	U2BRG	XXh
0162h	UART2 Transmit Buffer Register	U2TB	XXh
0163h			XXh
0164h	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
0165h	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
0166h	UART2 Receive Buffer Register	U2RB	XXh
0167h			XXh
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.7 SFR Information (7)(1)

Address	Register	Symbol	After reset
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.8 SFR Information (8)(1)

Address	Register	Symbol	After reset
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			
01C0h			
01C1h			
01C2h			
01C3h			
01C4h			
01C5h			
01C6h			
01C7h			
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h			
01E1h			
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.9 SFR Information (9)[1]

Address	Register	Symbol	After reset
01F0h			
01F1h			
01F2h			
01F3h			
01F4h			
01F5h			
01F6h			
01F7h			
01F8h			
01F9h			
01FAh			
01FBh			
01FCh			
01FDh			
01FEh			
01FFh			
0200h			
0201h			
0202h			
0203h			
0204h			
0205h			
0206h			
0207h			
0208h			
0209h			
020Ah			
020Bh			
020Ch			
020Dh			
020Eh			
020Fh			
0210h			
0211h			
0212h			
0213h			
0214h			
0215h			
0216h			
0217h			
0218h			
0219h			
021Ah			
021Bh			
021Ch			
021Dh			
021Eh			
021Fh			
0220h			
0221h			
0222h			
0223h			
0224h			
0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 5.3 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)		100(3)	–	–	times
–	Byte program time		–	50	400	µs
–	Block erase time		–	0.4	9	s
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time(7)	Ambient temperature = 55°C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.8 Comparator Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vref	Internal reference voltage	V_{CC} = 2.2 V to 5.5 V, T_{opr} = 25°C	1.15	1.25	1.35	V
		V_{CC} = 2.2 V to 5.5 V, T_{opr} = –40 to 85°C	–	1.25	–	V
Vcref	External input reference voltage	V_{CC} = 2.2 V to 4.0 V	0.5	–	V_{CC} – 1.1	V
		V_{CC} = 4.0 V to 5.5 V	0.5	–	V_{CC} – 1.5	
Vcin	External comparison voltage input range		–0.3	–	V_{CC} + 0.3	V
Vofs	Input offset voltage		–	20	120	mV
Tcrsp	Response time		–	4	–	µs

NOTE:
1. The measurement condition is T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.

Table 5.9 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-F	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V_{CC} = 4.75 V to 5.25 V, T_{opr} = 0 to 60°C(2)	7.76	8	8.24	MHz
		V_{CC} = 2.7 V to 5.5 V, T_{opr} = –20 to 85°C(2)	7.68	8	8.32	MHz
		V_{CC} = 2.7 V to 5.5 V, T_{opr} = –40 to 85°C(2)	7.44	8	8.32	MHz
		V_{CC} = 2.2 V to 5.5 V, T_{opr} = –20 to 85°C(3)	7.04	8	8.96	MHz
		V_{CC} = 2.2 V to 5.5 V, T_{opr} = –40 to 85°C(3)	6.8	8	9.2	MHz

NOTES:
1. The measurement condition is T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. These standard values show when the HRA1 register is set to the value before shipment and the HRA2 register is set to 00h.
3. These standard values show when the correction value in the FRA6 register is written into the HRA1 register.

Table 5.10 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	15	–	µA

NOTE:
1. V_{CC} = 2.2 to 5.5 V, T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.

Table 5.11 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP exit time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.12 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output “H” voltage		I_{OH} = –5 mA	V_{CC} – 2.0	–	V_{CC}	V
			I_{OH} = –200 μA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage		I_{OL} = 5 mA	–	–	2.0	V
			I_{OL} = 200 μA	–	–	0.45	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT4}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, RXD0, RXD2, CLK0, CLK2		0.1	0.5	–	V
		$\overline{RESET}$		0.1	1.0	–	V
I_{IH}	Input “H” current		VI = 5 V, V_{CC} = 5 V	–	–	5.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 5 V	–	–	–5.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 5 V	30	50	167	kΩ
R_{fXCIN}	Feedback resistance	XCIN		–	18	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode	2.0	–	–	V

NOTE:
1. V_{CC} = 4.2 to 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.

Table 5.13 Electrical Characteristics (2) [Vcc = 5 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed on-chip oscillator mode	High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5	8	mA
			High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		Low-speed on-chip oscillator mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	µA
		Low-speed clock mode	High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) FMR47 = 1	–	130	300	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) Program operation on RAM Flash memory off, FMSTP = 1	–	30	–	µA
		Wait mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	75	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	60	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit disabled (BGRCR0 = 1)	–	4	–	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit disabled (BGRCR0 = 1)	–	2.2	–	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit enabled (BGRCR0 = 0)	–	8	–	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit enabled (BGRCR0 = 0)	–	6	–	µA
		Stop mode	XCIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	–	0.8	3	µA
			XCIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	–	1.2	–	µA
			XCIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	–	5	8	µA
			XCIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	–	5.5	–	µA

Timing Requirements
(Unless Otherwise Specified: V_{CC} = 5 V, V_{SS} = 0 V at T_{opr} = 25°C) [V_{CC} = 5 V]

Table 5.14 XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

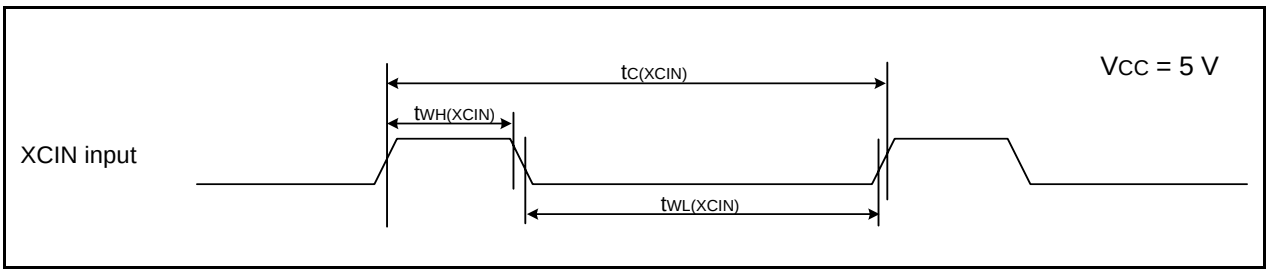


Figure 5.3 XCIN Input Timing Diagram when V_{CC} = 5 V

Table 5.15 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

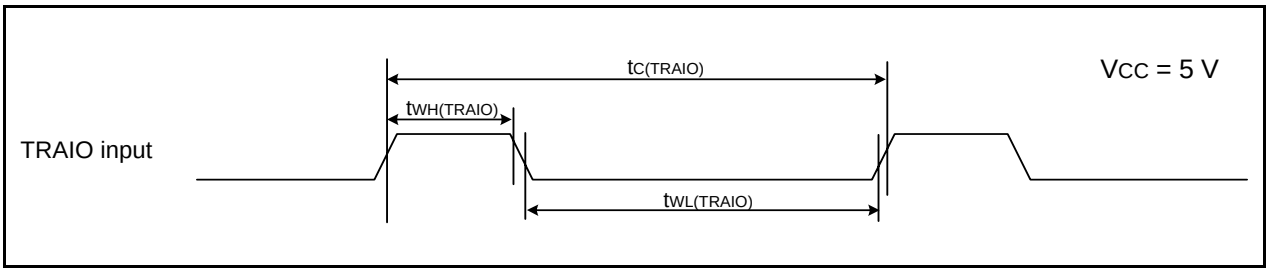


Figure 5.4 TRAIO Input Timing Diagram when V_{CC} = 5 V

Table 5.18 Electrical Characteristics (3) [V_{CC} = 3 V]

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output “H” voltage		I_{OH} = –1 mA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage		I_{OL} = 1 mA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT4}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, RXD0, RXD2, CLK0, CLK2		0.1	0.3	–	V
		$\overline{RESET}$		0.1	0.4	–	V
I_{IH}	Input “H” current		VI = 3 V, V_{CC} = 3 V	–	–	4.0	µA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 3 V	–	–	–4.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 3 V	66	160	500	kΩ
R_{fXCIN}	Feedback resistance	XCIN		–	18	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode	1.8	–	–	V

NOTE:
1. V_{CC} =2.7 to 3.3 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.

Table 5.19 Electrical Characteristics (4) [Vcc = 3 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss	High-speed on-chip oscillator mode	High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5	–	mA
			High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		Low-speed on-chip oscillator mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	µA
		Low-speed clock mode	High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) FMR47 = 1	–	130	300	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) Program operation on RAM Flash memory off, FMSTP = 1	–	30	–	µA
		Wait mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	70	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	55	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit disabled (BGRCR0 = 1)	–	3.8	–	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit disabled (BGRCR0 = 1)	–	2	–	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit enabled (BGRCR0 = 0)	–	8	–	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit enabled (BGRCR0 = 0)	–	6	–	µA
		Stop mode	XCIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	–	0.7	3	µA
			XCIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	–	1.1	–	µA
			XCIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	–	5	7	µA
			XCIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	–	5.5	–	µA

Timing requirements
(Unless Otherwise Specified: V_{CC} = 3 V, V_{SS} = 0 V at T_{opr} = 25°C) [V_{CC} = 3 V]

Table 5.20 XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

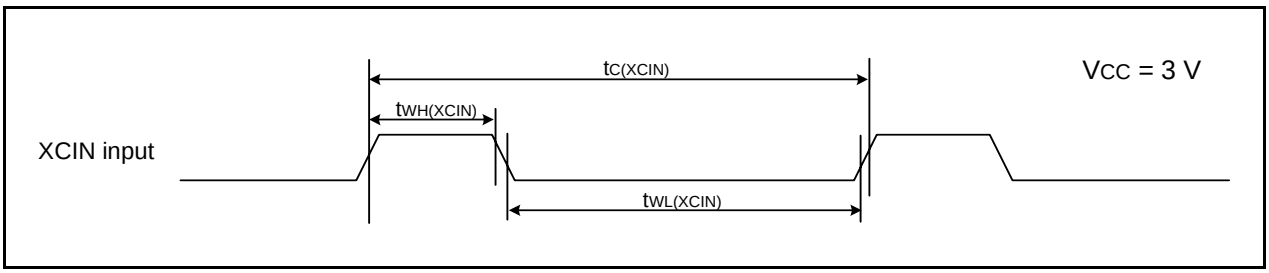


Figure 5.7 XCIN Input Timing Diagram when V_{CC} = 3 V

Table 5.21 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

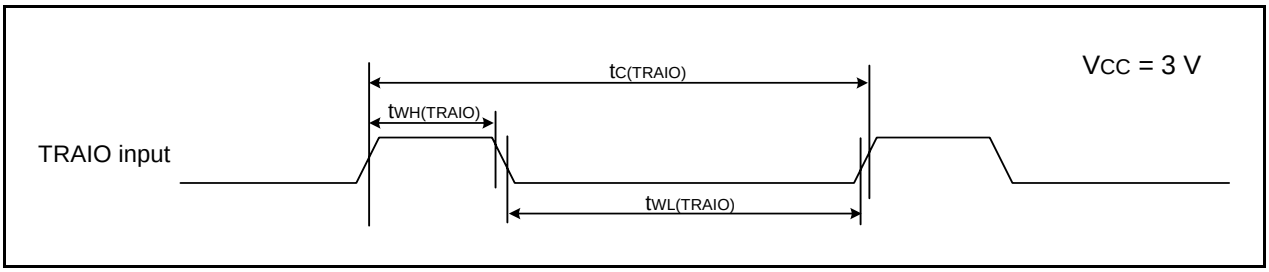


Figure 5.8 TRAIO Input Timing Diagram when V_{CC} = 3 V

Table 5.22 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	–	ns
$t_{W(CKH)}$	CLKi input “H” width	150	–	ns
$t_{W(CKL)}$	CLKi Input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 2

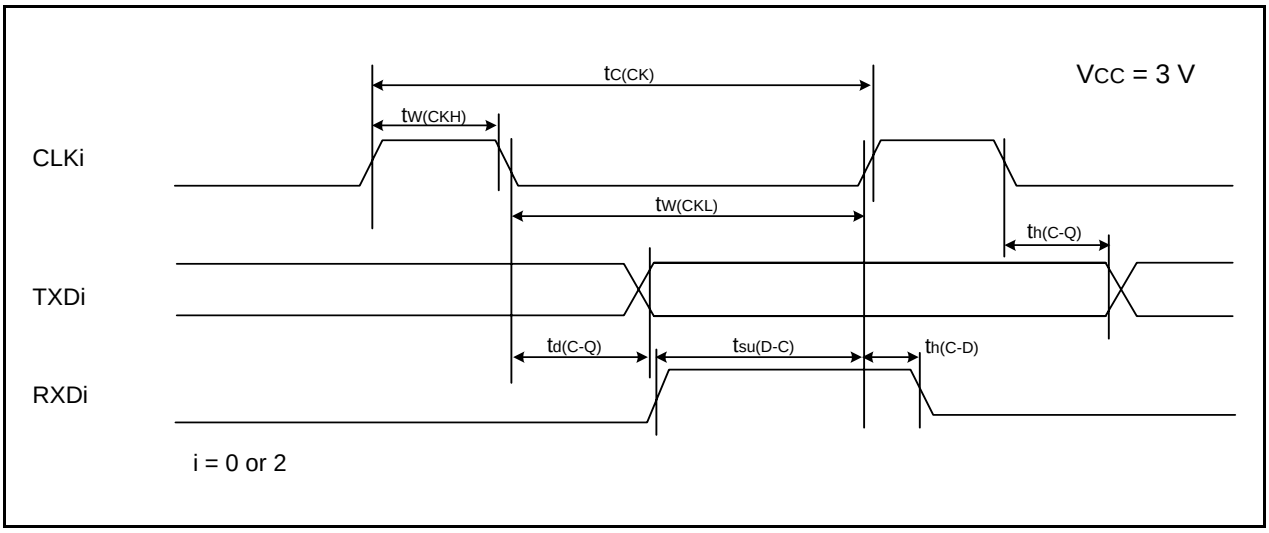


Figure 5.9 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.23 External Interrupt $\overline{INTi}$ (i = 0, 1, 2, 4) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

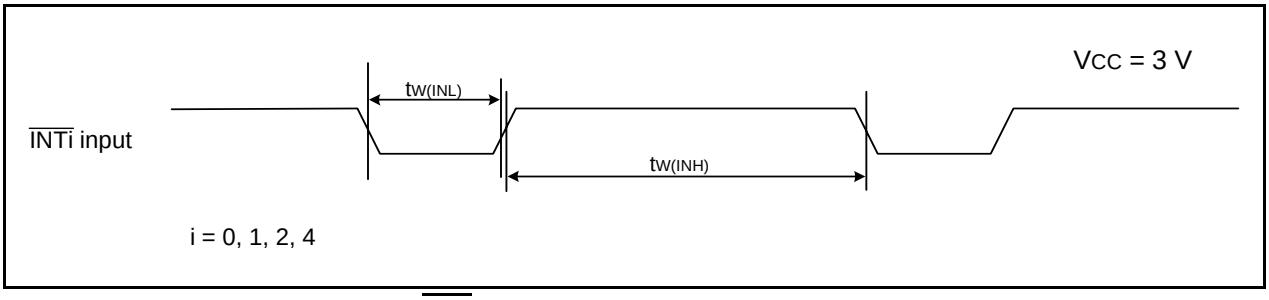


Figure 5.10 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 3 V

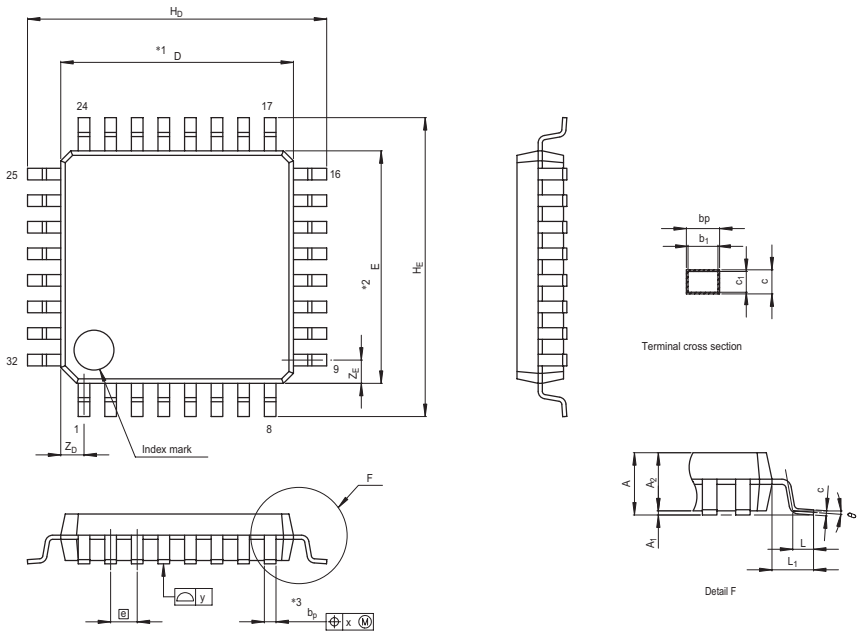
Table 5.25 Electrical Characteristics (6) [Vcc = 2.2 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are Vss	High-speed on-chip oscillator mode	High-speed on-chip oscillator on = 4 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	–	mA
			High-speed on-chip oscillator on = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		Low-speed on-chip oscillator mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	100	230	µA
		Low-speed clock mode	High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) FMR47 = 1	–	100	230	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) Program operation on RAM Flash memory off, FMSTP = 1	–	25	–	µA
		Wait mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	22	60	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	20	55	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit disabled (BGRCR0 = 1)	–	3	–	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit disabled (BGRCR0 = 1)	–	1.8	–	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit enabled (BGRCR0 = 0)	–	7	–	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit enabled (BGRCR0 = 0)	–	6	–	µA
		Stop mode	XCIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	–	0.7	3	µA
			XCIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	–	1.1	–	µA
			XCIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	–	5	7	µA
			XCIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	–	5.5	–	µA

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP32-7x7-0.80	PLQP0032GB-A	32P6U-A	0.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	0.7	—
Z_E	—	0.7	—
L	0.3	0.5	0.7
L_1	—	1.0	—