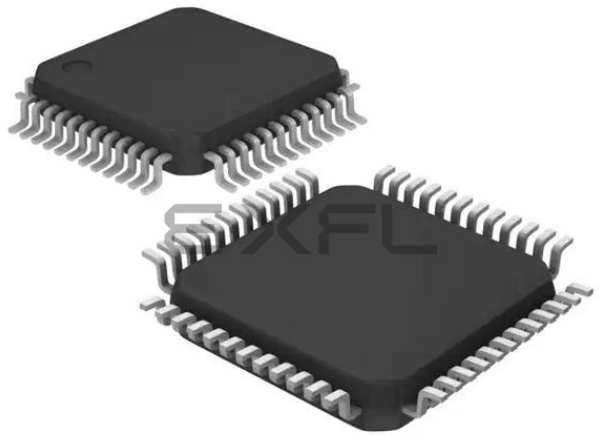

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	70MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2102fbd48-118

5. Pinning information

5.1 Pinning

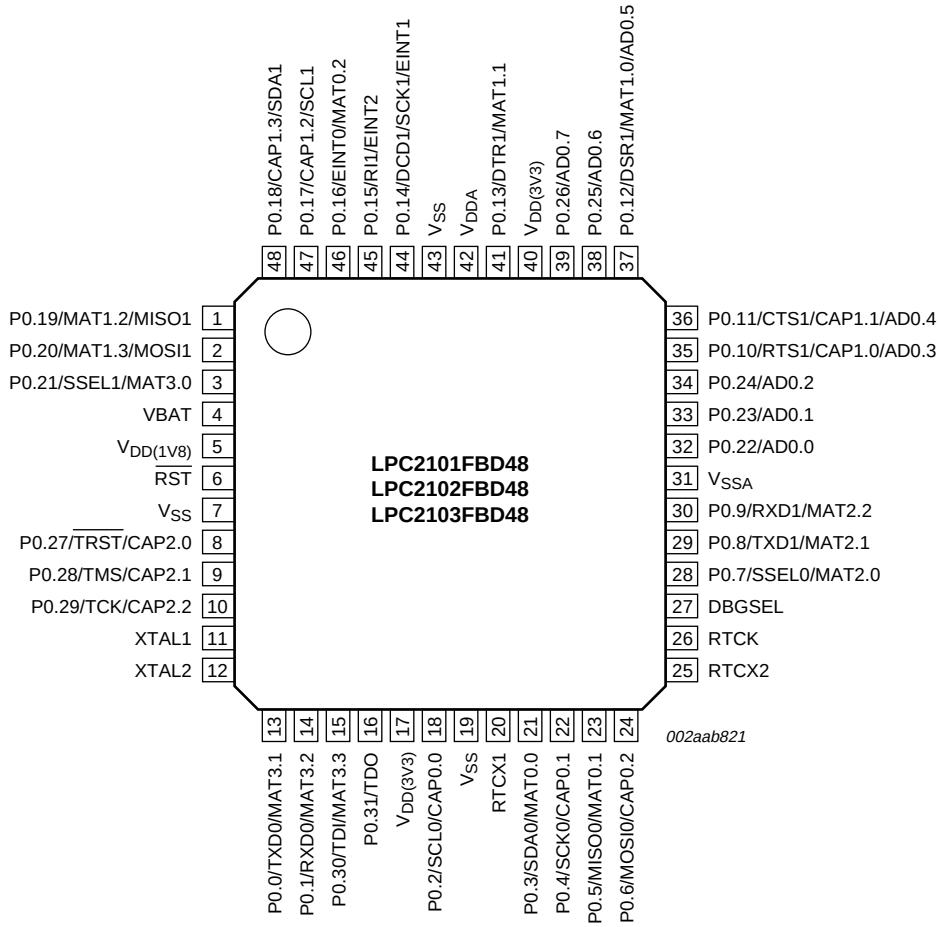


Fig 2. Pin configuration (LQFP48)

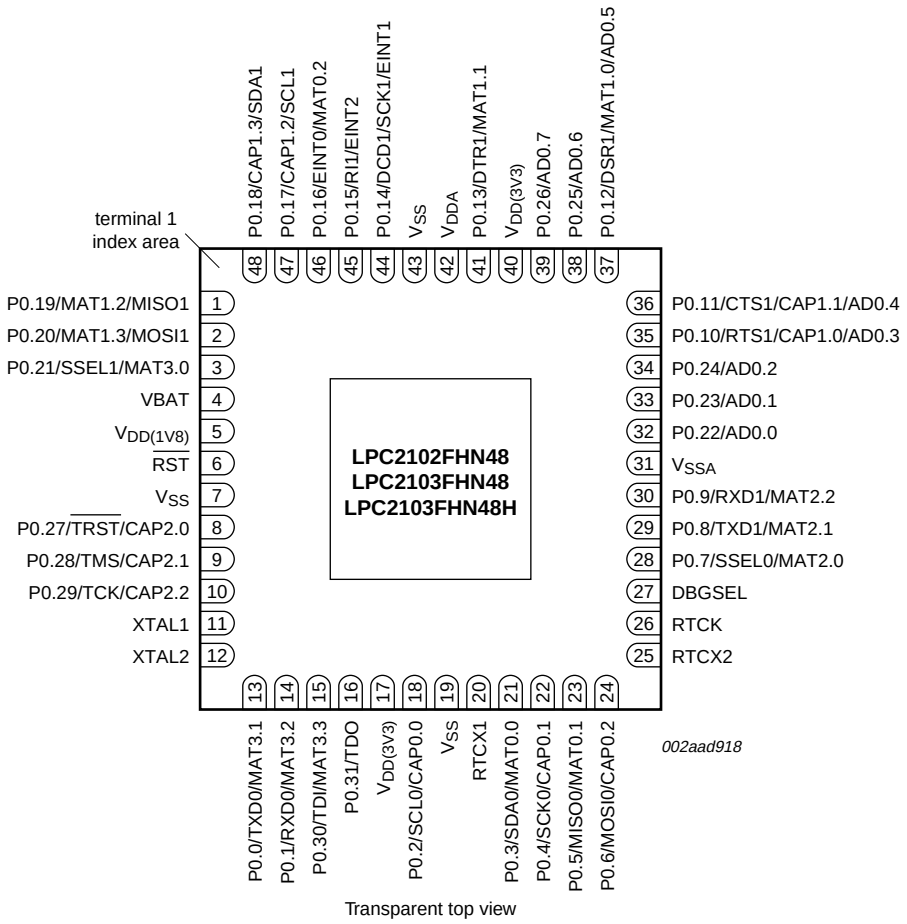


Fig 3. Pin configuration (HVQFN48)

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
P0.0 to P0.31		I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. A total of 31 pins of the Port 0 can be used as general purpose bidirectional digital I/Os while P0.31 is an output only pin. The operation of port 0 pins depends upon the pin function selected via the pin connect block.
P0.0/TXD0/ MAT3.1	13[1]	I/O	**P0.0 —** General purpose input/output digital pin.
		O	**TXD0 —** Transmitter output for UART0.
		O	**MAT3.1 —** PWM output 1 for Timer 3.
P0.1/RXD0/ MAT3.2	14[1]	I/O	**P0.1 —** General purpose input/output digital pin.
		I	**RXD0 —** Receiver input for UART0.
		O	**MAT3.2 —** PWM output 2 for Timer 3.
P0.2/SCL0/ CAP0.0	18[2]	I/O	**P0.2 —** General purpose input/output digital pin. Output is open-drain.
		I/O	**SCL0 —** I^2C0 clock Input/output. Open-drain output (for I^2C-bus compliance).
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P0.3/SDA0/ MAT0.0	21[2]	I/O	**P0.3 —** General purpose input/output digital pin. Output is open-drain.
		I/O	**SDA0 —** I^2C0 data input/output. Open-drain output (for I^2C-bus compliance).
		O	**MAT0.0 —** PWM output for Timer 0, channel 0. Output is open-drain.
P0.4/SCK0/ CAP0.1	22[1]	I/O	**P0.4 —** General purpose input/output digital pin.
		I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
		I	**CAP0.1 —** Capture input for Timer 0, channel 1.
P0.5/MISO0/ MAT0.1	23[1]	I/O	**P0.5 —** General purpose input/output digital pin.
		I/O	**MISO0 —** Master In Slave Out for SPI0. Data input to SPI master or data output from SPI slave.
		O	**MAT0.1 —** PWM output for Timer 0, channel 1.
P0.6/MOSI0/ CAP0.2	24[1]	I/O	**P0.6 —** General purpose input/output digital pin.
		I/O	**MOSI0 —** Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
P0.7/SSEL0/ MAT2.0	28[1]	I/O	**P0.7 —** General purpose input/output digital pin.
		I	**SSEL0 —** Slave Select for SPI0. Selects the SPI interface as a slave.
		O	**MAT2.0 —** PWM output for Timer 2, channel 0.
P0.8/TXD1/ MAT2.1	29[1]	I/O	**P0.8 —** General purpose input/output digital pin.
		O	**TXD1 —** Transmitter output for UART1.
		O	**MAT2.1 —** PWM output for Timer 2, channel 1.
P0.9/RXD1/ MAT2.2	30[1]	I/O	**P0.9 —** General purpose input/output digital pin.
		I	**RXD1 —** Receiver input for UART1.
		O	**MAT2.2 —** PWM output for Timer 2, channel 2.
P0.10/RTS1/ CAP1.0/AD0.3	35[3]	I/O	**P0.10 —** General purpose input/output digital pin.
		O	**RTS1 —** Request to Send output for UART1.
		I	**CAP1.0 —** Capture input for Timer 1, channel 0.
		I	**AD0.3 —** ADC 0, input 3.

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
P0.11/CTS1/ CAP1.1/AD0.4	36[3]	I/O	**P0.11 —** General purpose input/output digital pin.
		I	**CTS1 —** Clear to Send input for UART1.
		I	**CAP1.1 —** Capture input for Timer 1, channel 1.
		I	**AD0.4 —** ADC 0, input 4.
P0.12/DSR1/ MAT1.0/AD0.5	37[3]	I/O	**P0.12 —** General purpose input/output digital pin.
		I	**DSR1 —** Data Set Ready input for UART1.
		O	**MAT1.0 —** PWM output for Timer 1, channel 0.
		I	**AD0.5 —** ADC 0, input 5.
P0.13/DTR1/ MAT1.1	41[1]	I/O	**P0.13 —** General purpose input/output digital pin.
		O	**DTR1 —** Data Terminal Ready output for UART1.
		O	**MAT1.1 —** PWM output for Timer 1, channel 1.
P0.14/DCD1/ SCK1/EINT1	44[4][5]	I/O	**P0.14 —** General purpose input/output digital pin.
		I	**DCD1 —** Data Carrier Detect input for UART1.
		I/O	**SCK1 —** Serial Clock for SPI1. SPI clock output from master or input to slave.
		I	**EINT1 —** External interrupt 1 input.
P0.15/RI1/ EINT2	45[4]	I/O	**P0.15 —** General purpose input/output digital pin.
		I	**RI1 —** Ring Indicator input for UART1.
		I	**EINT2 —** External interrupt 2 input.
P0.16/EINT0/ MAT0.2	46[4]	I/O	**P0.16 —** General purpose input/output digital pin.
		I	**EINT0 —** External interrupt 0 input.
		O	**MAT0.2 —** PWM output for Timer 0, channel 2.
P0.17/CAP1.2/ SCL1	47[6]	I/O	**P0.17 —** General purpose input/output digital pin. The output is not open-drain.
		I	**CAP1.2 —** Capture input for Timer 1, channel 2.
		I/O	**SCL1 —** I^2C1 clock Input/output. This pin is an open-drain output if I^2C1 function is selected in the pin connect block.
P0.18/CAP1.3/ SDA1	48[6]	I/O	**P0.18 —** General purpose input/output digital pin. The output is not open-drain.
		I	**CAP1.3 —** Capture input for Timer 1, channel 3.
		I/O	**SDA1 —** I^2C1 data Input/output. This pin is an open-drain output if I^2C1 function is selected in the pin connect block.
P0.19/MAT1.2/ MISO1	1[1]	I/O	**P0.19 —** General purpose input/output digital pin.
		O	**MAT1.2 —** PWM output for Timer 1, channel 2.
		I/O	**MISO1 —** Master In Slave Out for SSP. Data input to SSP master or data output from SSP slave.
P0.20/MAT1.3/ MOSI1	2[1]	I/O	**P0.20 —** General purpose input/output digital pin.
		O	**MAT1.3 —** PWM output for Timer 1, channel 3.
		I/O	**MOSI1 —** Master Out Slave for SSP. Data output from SSP master or data input to SSP slave.
P0.21/SSEL1/ MAT3.0	3[1]	I/O	**P0.21 —** General purpose input/output digital pin.
		I	**SSEL1 —** Slave Select for SPI1. Selects the SPI interface as a slave.
		O	**MAT3.0 —** PWM output for Timer 3, channel 0.

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
P0.22/AD0.0	32[3]	I/O	**P0.22 —** General purpose input/output digital pin.
		I	**AD0.0 —** ADC 0, input 0.
P0.23/AD0.1	33[3]	I/O	**P0.23 —** General purpose input/output digital pin.
		I	**AD0.1 —** ADC 0, input 1.
P0.24/AD0.2	34[3]	I/O	**P0.24 —** General purpose input/output digital pin.
		I	**AD0.2 —** ADC 0, input 2.
P0.25/AD0.6	38[3]	I/O	**P0.25 —** General purpose input/output digital pin.
		I	**AD0.6 —** ADC 0, input 6.
P0.26/AD0.7	39[3]	I/O	**P0.26 —** General purpose input/output digital pin.
		I	**AD0.7 —** ADC 0, input 7.
P0.27/$\overline{\text{TRST}}$/CAP2.0	8[1]	I/O	**P0.27 —** General purpose input/output digital pin.
		I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface. If DBGSEL is HIGH, this pin is automatically configured for use with EmbeddedICE (Debug mode).
		I	**CAP2.0 —** Capture input for Timer 2, channel 0.
P0.28/TMS/CAP2.1	9[1]	I/O	**P0.28 —** General purpose input/output digital pin.
		I	**TMS —** Test Mode Select for JTAG interface. If DBGSEL is HIGH, this pin is automatically configured for use with EmbeddedICE (Debug mode).
		I	**CAP2.1 —** Capture input for Timer 2, channel 1.
P0.29/TCK/CAP2.2	10[1]	I/O	**P0.29 —** General purpose input/output digital pin.
		I	**TCK —** Test Clock for JTAG interface. This clock must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate. If DBGSEL is HIGH, this pin is automatically configured for use with EmbeddedICE (Debug mode).
		I	**CAP2.2 —** Capture input for Timer 2, channel 2.
P0.30/TDI/MAT3.3	15[1]	I/O	**P0.30 —** General purpose input/output digital pin.
		I	**TDI —** Test Data In for JTAG interface. If DBGSEL is HIGH, this pin is automatically configured for use with EmbeddedICE (Debug mode).
		O	**MAT3.3 —** PWM output 3 for Timer 3.
P0.31/TDO	16[1]	O	**P0.31 —** General purpose output only digital pin.
		O	**TDO —** Test Data Out for JTAG interface. If DBGSEL is HIGH, this pin is automatically configured for use with EmbeddedICE (Debug mode).
RTCX1	20[7][8]	I	Input to the RTC oscillator circuit. Input voltage must not exceed 1.8 V.
RTCX2	25[7][8]	O	Output from the RTC oscillator circuit.
RTCK	26[7]	I/O	**Returned test clock output:** Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up.
XTAL1	11	I	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTAL2	12	O	Output from the oscillator amplifier.
DBGSEL	27	I	**Debug select:** When LOW, the part operates normally. When externally pulled HIGH at reset, P0.27 to P0.31 are configured as JTAG port, and the part is in Debug mode[9]. Input with internal pull-down.
$\overline{\text{RST}}$	6	I	**External reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.

6.3 On-chip static RAM

On-chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8-bits, 16-bits, and 32-bits. The LPC2101/02/03 provide 2 kB, 4 kB or 8 kB of static RAM.

6.4 Memory map

The LPC2101/02/03 memory map incorporates several distinct regions, as shown in Figure 4.

In addition, the CPU interrupt vectors may be re-mapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in Section 6.17 "System control".

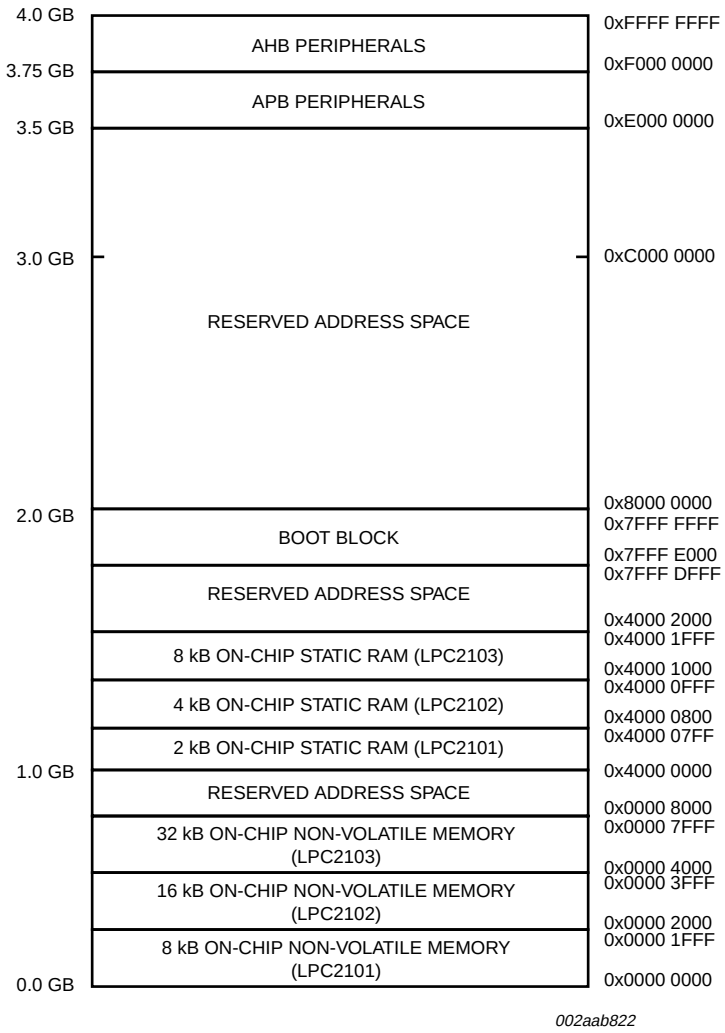


Fig 4. LPC2101/02/03 memory map

- Combined SPI master and slave.
- Maximum data bit rate of one eighth of the input clock rate.

6.12 SSP serial I/O controller

The LPC2101/02/03 each contain one SSP. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. However, only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with data frames of 4 bits to 16 bits flowing from the master to the slave and from the slave to the master. Often only one of these data streams carries meaningful data.

6.12.1 Features

- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor's Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- Four bits to 16 bits per frame

6.13 General purpose 32-bit timers/external event counters

The Timer/Counter is designed to count cycles of the Peripheral Clock (PCLK) or an externally supplied clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with 'or' and 'and', as well as 'broadcast' functions among them.

The LPC2101/02/03 can count external events on one of the capture inputs if the minimum external pulse is equal or longer than a period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs or used as external interrupts.

6.13.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- External event counter or timer operation.
- Four 32-bit capture channels per timer/counter that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Four external outputs per timer/counter corresponding to match registers, with the following capabilities:
  - Set LOW on match.

- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal pre-scaler.
- Selectable time period from ($T_{PCLK} \times 256 \times 4$) to ($T_{PCLK} \times 2^{32} \times 4$) in multiples of $T_{PCLK} \times 4$.

6.16 Real-time clock

The Real-Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.16.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra-low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Can use either the RTC dedicated 32 kHz oscillator input or clock derived from the external crystal/oscillator input at XTAL1. The programmable reference clock divider allows fine adjustment of the RTC.
- Dedicated power supply pin can be connected to a battery or the main 3.3 V.

6.17 System control

6.17.1 Crystal oscillator

The on-chip integrated oscillator operates with external crystal in range of 1 MHz to 25 MHz. The oscillator output frequency is called f_{osc} and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. f_{osc} and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.17.2 “PLL” and Section 10.1 “XTAL1 input” for additional information.

6.17.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 70 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 µs.

6.17.3 Reset and wake-up timer

Reset has two sources on the LPC2101/02/03: the $\overline{\text{RST}}$ pin and watchdog reset. The $\overline{\text{RST}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip reset by any source starts the wake-up timer (see wake-up timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined reset values.

The wake-up timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down and Deep power-down mode, any wake-up of the processor from the Power-down modes makes use of the wake-up timer.

The wake-up timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of V_{DD} ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g., capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

In Idle mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers, and internal buses.

In Power-down mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Power-down mode and the logic levels of chip output pins remain static. The Power-down mode can be terminated and normal operation resumed by either a reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Power-down mode reduces chip power consumption to nearly zero.

Selecting an external 32 kHz clock instead of the PCLK as a clock-source for the on-chip RTC will enable the microcontroller to have the RTC active during Power-down mode. Power-down current is increased with RTC active. However, it is significantly lower than in Idle mode.

In Deep-power down mode all power is removed from the internal chip logic except for the RTC module, the I/O ports, the SRAM, and the 32 kHz external oscillator. For additional power savings, SRAM and the 32 kHz oscillator can be powered down individually. The Deep power-down mode produces the lowest possible power consumption without actually removing power from the entire chip. In Deep power-down mode, the contents of registers and memory are not preserved except for SRAM, if selected, and three general purpose registers. Therefore, to resume operations, a full chip reset process is required.

A power selector module switches the RTC power supply from VBAT to $V_{DD(1V8)}$ whenever the core voltage is present on pin $V_{DD(1V8)}$ to conserve battery power.

A power control for peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings during Active and Idle mode.

6.17.8 APB

The APB divider determines the relationship between the processor clock (CCLK) and the clock used by peripheral devices (PCLK). The APB divider serves two purposes. The first is to provide peripherals with the desired PCLK via APB so that they can operate at the speed chosen for the ARM processor. In order to achieve this, the APB may be slowed down to $\frac{1}{2}$ to $\frac{1}{4}$ of the processor clock rate. Because the APB must work properly at power-up (and its timing cannot be altered if it does not work since the APB divider control registers reside on the APB), the default condition at reset is for the APB to run at $\frac{1}{4}$ of the processor clock rate. The second purpose of the APB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the APB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

6.18 Emulation and debugging

The LPC2101/02/03 support emulation and debugging via a JTAG serial port.

8. Static characteristics

Table 5. Static characteristics

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	1.65	1.8	1.95	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	2.6[4]	3.3	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage			2.6[5]	3.3	3.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT			2.0[6]	3.3	3.6	V
Standard port pins, $\overline{RST}$, RTCK							
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	3	µA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; no pull-down		-	-	3	µA
I_{OZ}	OFF-state output current	V_O = 0 V, $V_O = V_{DD(3V3)}$; no pull-up/down		-	-	3	µA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; T_j < 125 °C		-	-	100	mA
V_I	input voltage	pin configured to provide a digital function; $V_{DD(3V3)}$ and $V_{DDA} \geq 3.0$ V	[7][8][9]	0	-	5.5	V
		pin configured to provide a digital function; $V_{DD(3V3)}$ and V_{DDA} < 3.0 V	[7][8][9]	0		$V_{DD(3V3)}$	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	[10]	$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = −4 mA	[10]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V	[10]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[10]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[11]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DDA}$	[11]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V[12]		10	50	150	µA

Table 5. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$V_{o(XTAL2)}$	output voltage on pin XTAL2		0	-	1.8	V
$V_{i(RTCX1)}$	input voltage on pin RTCX1		0	-	1.8	V
$V_{o(RTCX2)}$	output voltage on pin RTCX2		0	-	1.8	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Core and internal rail.

[3] External rail.

[4] If $V_{DD(3V3)}$ < 3.0 V, the I/O pins are not 5 V tolerant, and the ADC input voltage is limited to V_{DDA} = 3.0 V.

[5] If V_{DDA} < 3.0 V, the I/O pins are not 5 V tolerant.

[6] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[7] Including voltage on outputs in 3-state mode.

[8] $V_{DD(3V3)}$ supply voltages must be present.

[9] 3-state outputs go into 3-state mode when $V_{DD(3V3)}$ is grounded.

[10] Accounts for 100 mV voltage drop in all supply lines.

[11] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[12] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V. $V_{DDA} \geq 3.0$ V and $V_{DD(3V3)} \geq 3.0$ V.

[13] Applies to P0.25:16.

[14] Battery supply current on pin VBAT.

[15] Input leakage current to V_{SS}.

Table 6. ADC static characteristics

V_{DDA} = 2.5 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified. ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DDA}	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	[1][2][3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity	[1][4]	-	-	±2	LSB
E_O	offset error	[1][5]	-	-	±3	LSB
E_G	gain error	[1][6]	-	-	±0.5	%
E_T	absolute error	[1][7]	-	-	±4	LSB

[1] Conditions: V_{SSA} = 0 V, V_{DDA} = 3.3 V and $V_{DD(3V3)}$ = 3.3 V for 10-bit resolution at full speed; V_{DDA} = 2.6 V, $V_{DD(3V3)}$ = 2.6 V for 8-bit resolution at full speed.

[2] The ADC is monotonic, there are no missing codes.

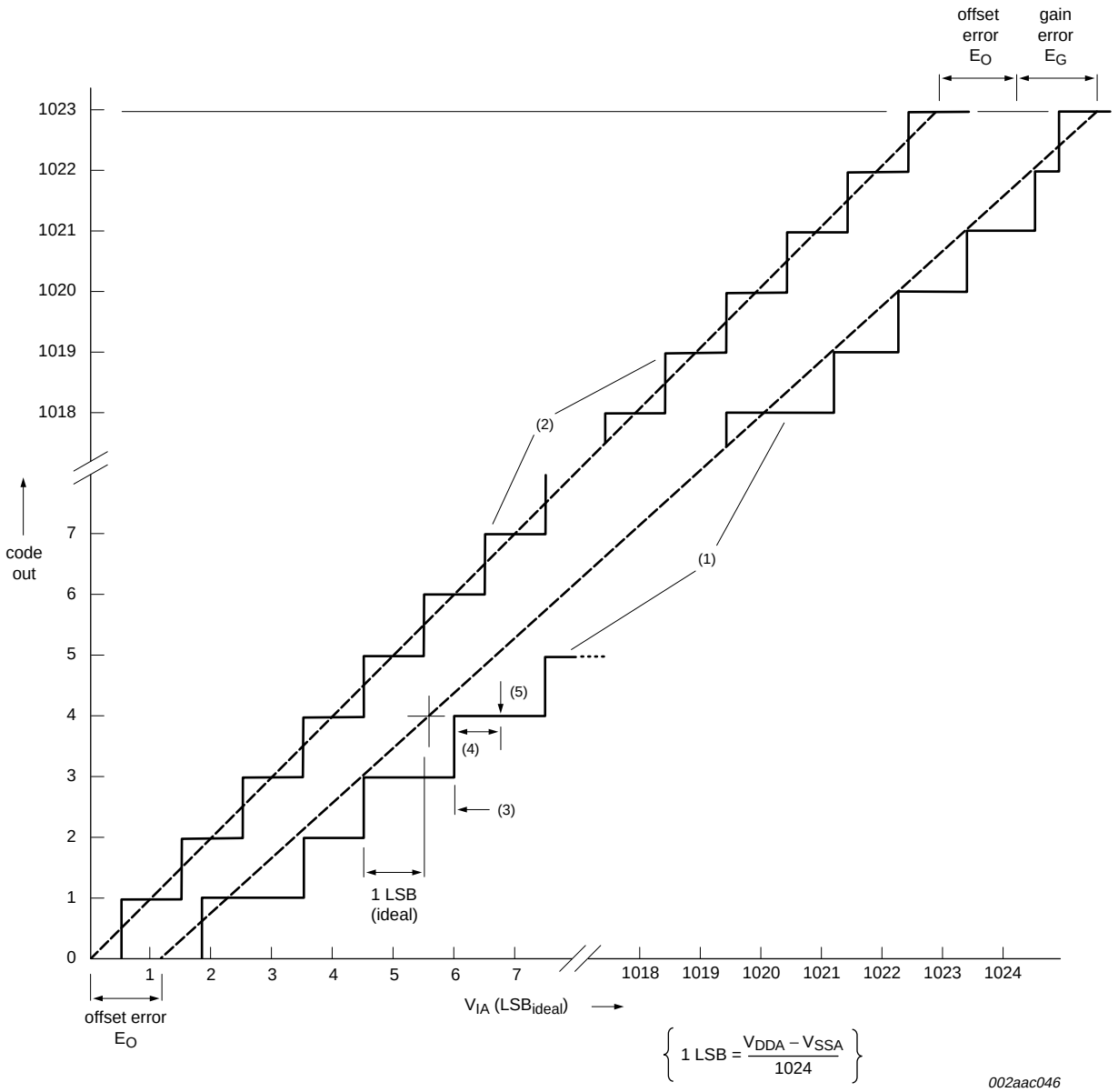
[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 5.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 5.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 5.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 5.

[7] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 5.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

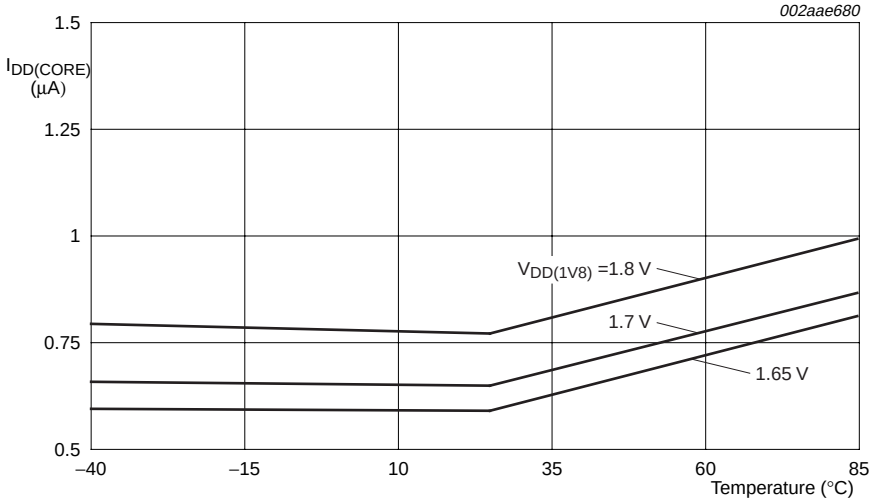
(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

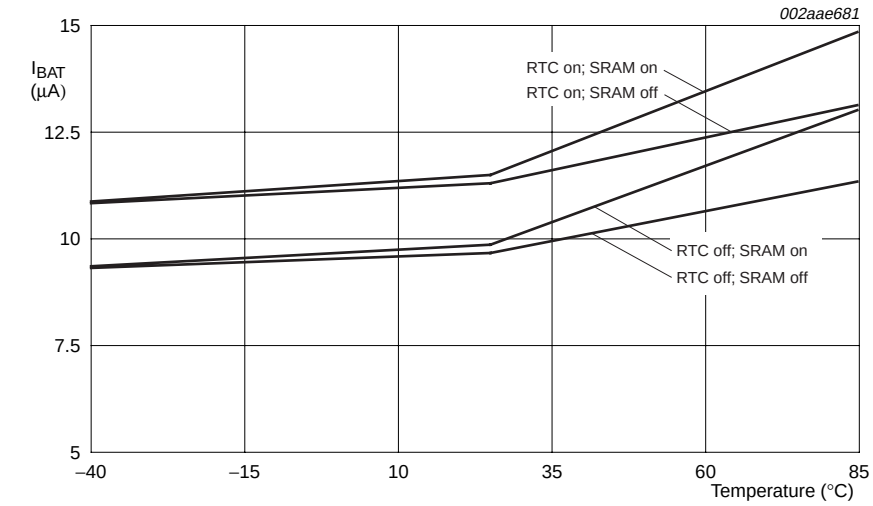
Fig 5. ADC conversion characteristics

8.1 Power consumption in Deep power-down mode



Test conditions: Deep power-down mode entered; RTC off; SRAM off; $V_{i(VBAT)} = V_{DD(3V3)} = V_{DDA} = 3.3$ V.

Fig 6. Core supply current $I_{DD(CORE)}$ measured at different temperatures and supply voltages



Test conditions: Deep power-down mode entered; $V_{i(BAT)} = 3.3$ V; $V_{DD(1V8)} = 1.8$ V; $V_{DD(3V3)} = V_{DDA} = 3.3$ V.

Fig 7. Battery supply current I_{BAT} measured at different temperatures and conditions

9. Dynamic characteristics

Table 7. Dynamic characteristics

T_{amb} = 0 °C to 70 °C for commercial applications, −40 °C to +85 °C for industrial applications, $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges[1].

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
External clock						
f_{osc}	oscillator frequency		10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	100	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0.2 and P0.3)						
$t_{r(o)}$	output rise time		-	10	-	ns
$t_{f(o)}$	output fall time		-	10	-	ns
I^2C-bus pins (P0.2 and P0.3)						
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	$20 + 0.1 \times C_b$[3]	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.

10. Application information

10.1 XTAL1 input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV (RMS) is needed. For more details see the *LPC2101/02/03 User manual UM10161*.

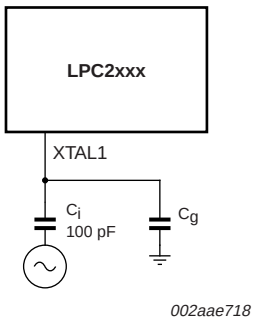
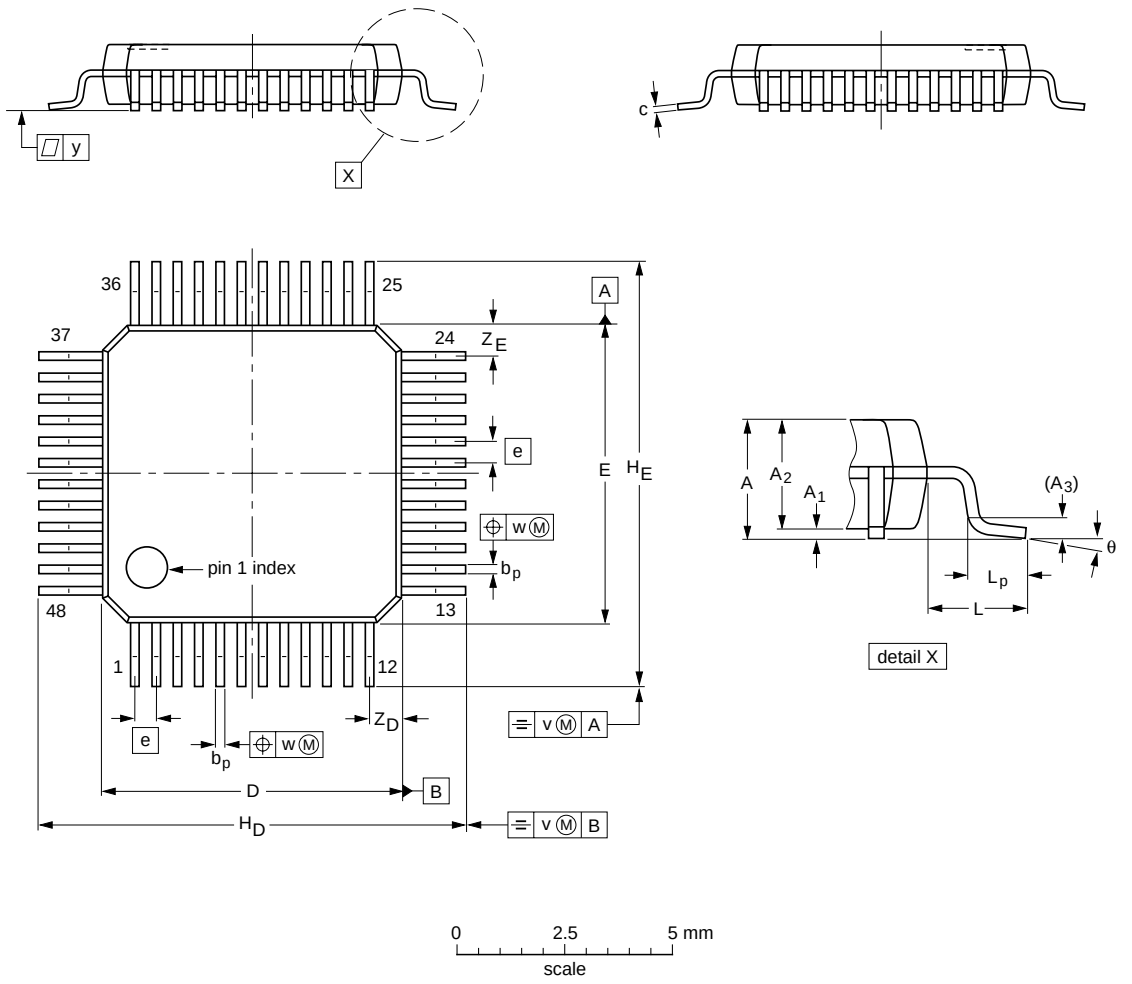


Fig 9. Slave mode operation of the on-chip oscillator

11. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

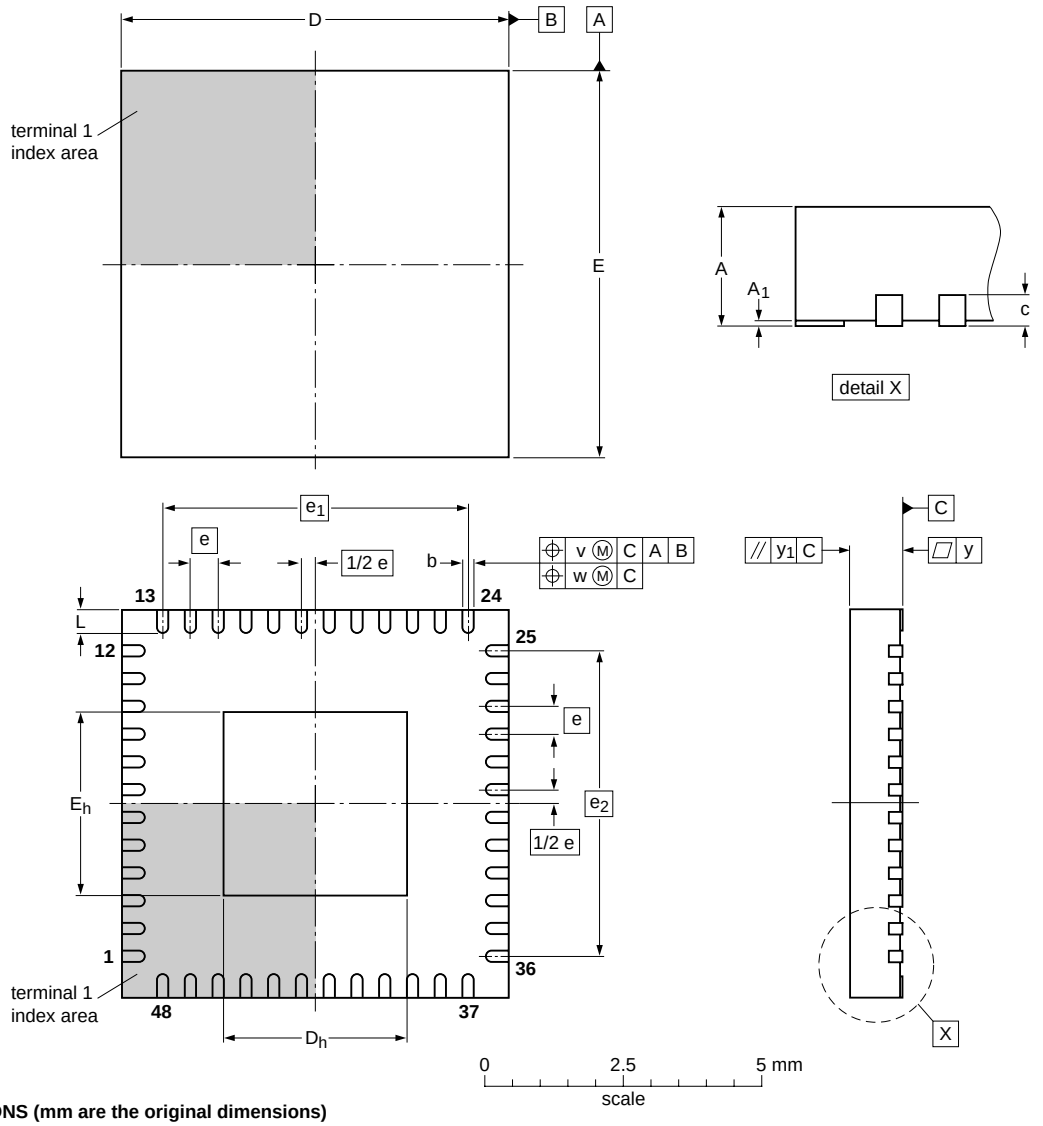
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 10. Package outline SOT313-2 (LQFP48)

HVQFN48: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 x 7 x 0.85 mm **SOT619-7**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	7.1 6.9	3.45 3.15	7.1 6.9	3.45 3.15	0.5	5.5	5.5	0.5 0.3	0.1	0.05	0.05	0.1

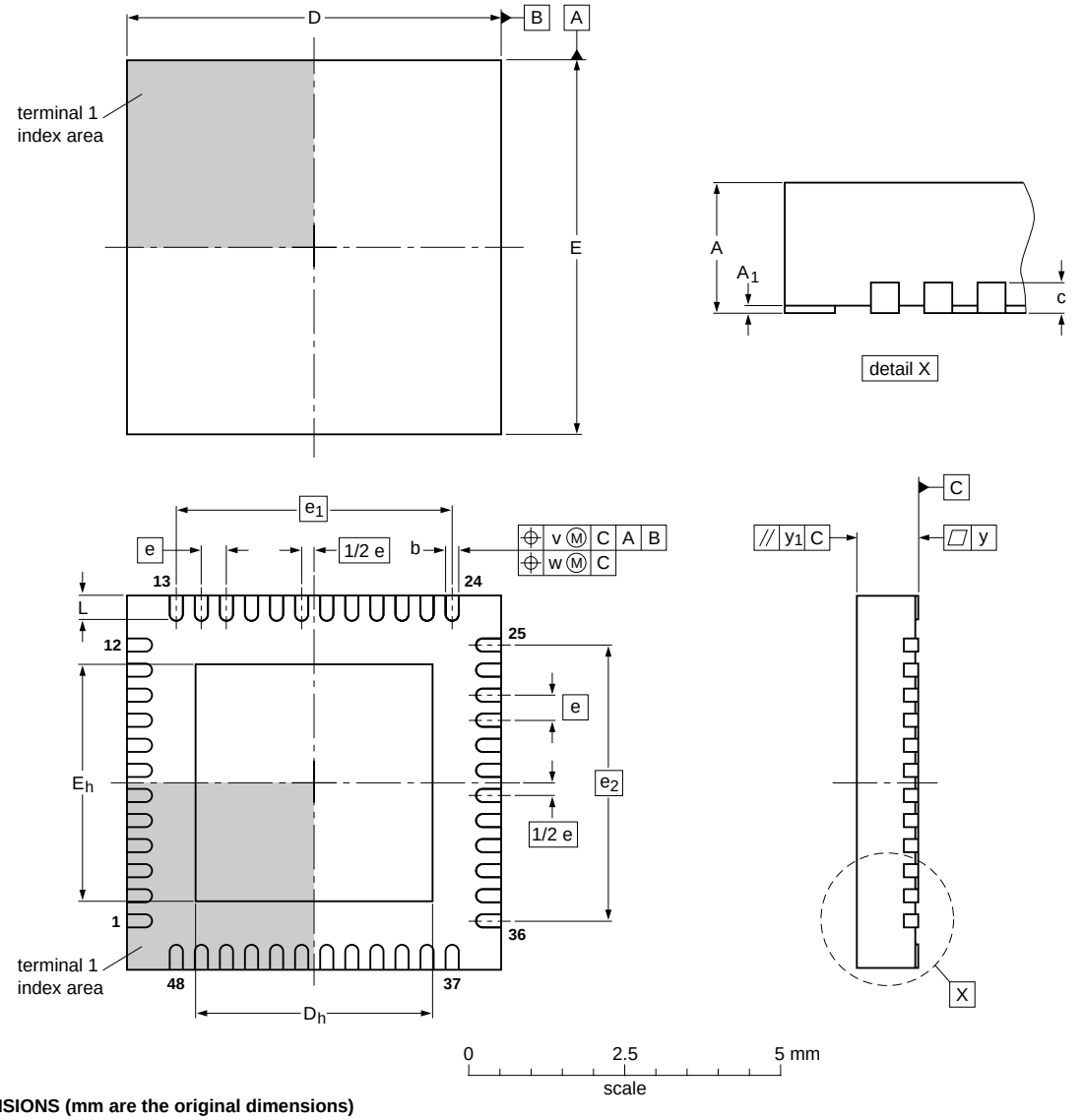
Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT619-7	- - -	MO-220	- - -			~~05-10-24~~ 05-10-25

Fig 11. Package outline SOT619-7 (HVQFN48)

HVQFN48: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 6 x 6 x 0.85 mm **SOT778-3**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.25 0.15	0.2	6.1 5.9	3.95 3.65	6.1 5.9	3.95 3.65	0.4	4.4	4.4	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT778-3	- - -	- - -	- - -			~~04-06-16~~ 04-06-23

Fig 12. Package outline SOT778-3 (HVQFN48)

12. Abbreviations

Table 8. Acronym list

Acronym	Description
ADC	Analog-to-Digital Converter
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
DCC	Debug Communications Channel
DSP	Digital Signal Processor
FIFO	First In, First Out
FIQ	Fast Interrupt reQuest
GPIO	General Purpose Input/Output
IAP	In-Application Programming
IRQ	Interrupt Request
ISP	In-System Programming
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSI	Synchronous Serial Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
VIC	Vectored Interrupt Controller

16. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

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