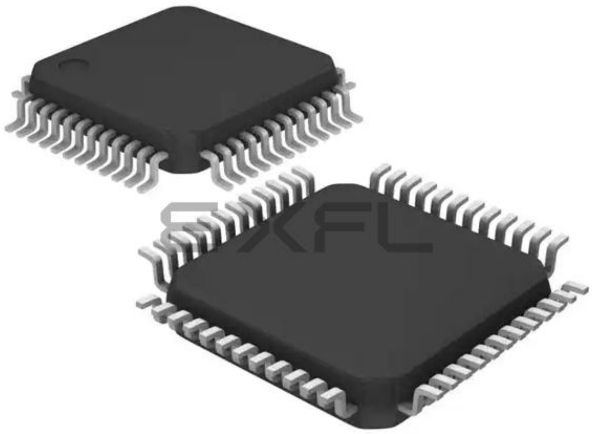

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	70MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2102fbd48-151

5. Pinning information

5.1 Pinning

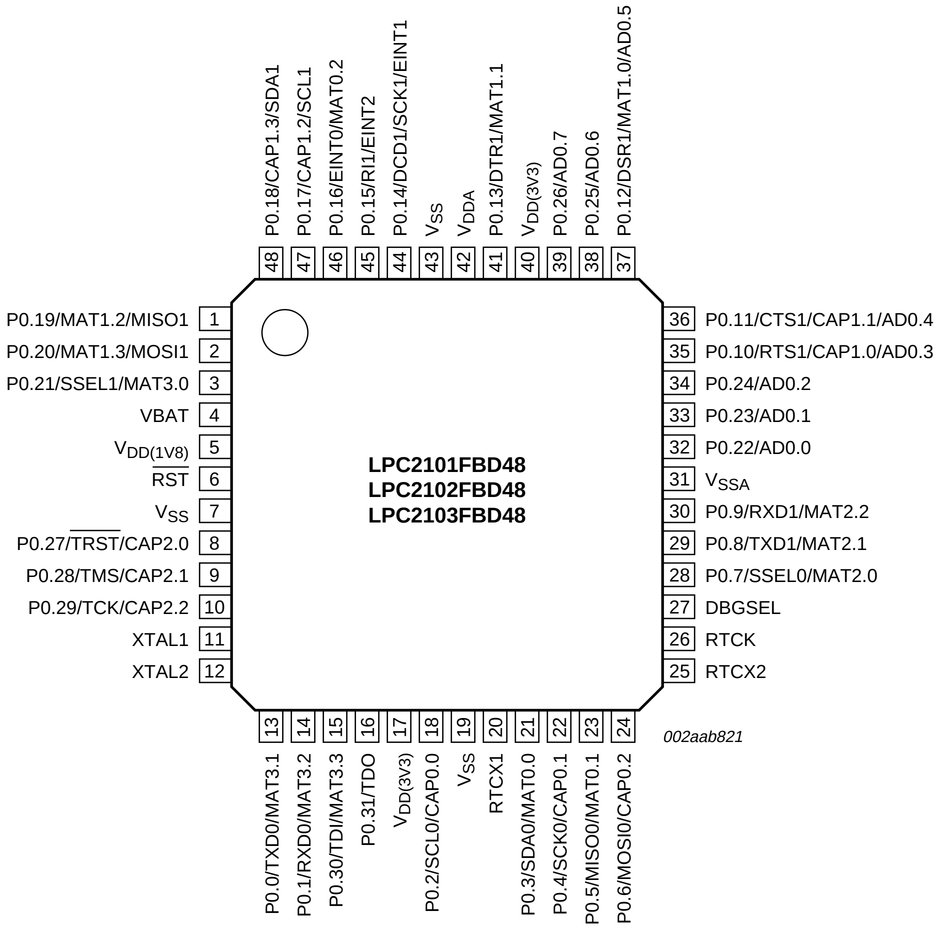

Fig 2. Pin configuration (LQFP48)

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5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
P0.0 to P0.31		I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. A total of 31 pins of the Port 0 can be used as general purpose bidirectional digital I/Os while P0.31 is an output only pin. The operation of port 0 pins depends upon the pin function selected via the pin connect block.
P0.0/TXD0/ MAT3.1	13[1]	I/O	**P0.0** — General purpose input/output digital pin.
		O	**TXD0** — Transmitter output for UART0.
		O	**MAT3.1** — PWM output 1 for Timer 3.
P0.1/RXD0/ MAT3.2	14[1]	I/O	**P0.1** — General purpose input/output digital pin.
		I	**RXD0** — Receiver input for UART0.
		O	**MAT3.2** — PWM output 2 for Timer 3.
P0.2/SCL0/ CAP0.0	18[2]	I/O	**P0.2** — General purpose input/output digital pin. Output is open-drain.
		I/O	**SCL0** — I^2C0 clock Input/output. Open-drain output (for I^2C-bus compliance).
		I	**CAP0.0** — Capture input for Timer 0, channel 0.
P0.3/SDA0/ MAT0.0	21[2]	I/O	**P0.3** — General purpose input/output digital pin. Output is open-drain.
		I/O	**SDA0** — I^2C0 data input/output. Open-drain output (for I^2C-bus compliance).
		O	**MAT0.0** — PWM output for Timer 0, channel 0. Output is open-drain.
P0.4/SCK0/ CAP0.1	22[1]	I/O	**P0.4** — General purpose input/output digital pin.
		I/O	**SCK0** — Serial clock for SPI0. SPI clock output from master or input to slave.
		I	**CAP0.1** — Capture input for Timer 0, channel 1.
P0.5/MISO0/ MAT0.1	23[1]	I/O	**P0.5** — General purpose input/output digital pin.
		I/O	**MISO0** — Master In Slave Out for SPI0. Data input to SPI master or data output from SPI slave.
		O	**MAT0.1** — PWM output for Timer 0, channel 1.
P0.6/MOSI0/ CAP0.2	24[1]	I/O	**P0.6** — General purpose input/output digital pin.
		I/O	**MOSI0** — Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
		I	**CAP0.2** — Capture input for Timer 0, channel 2.
P0.7/SSEL0/ MAT2.0	28[1]	I/O	**P0.7** — General purpose input/output digital pin.
		I	**SSEL0** — Slave Select for SPI0. Selects the SPI interface as a slave.
		O	**MAT2.0** — PWM output for Timer 2, channel 0.
P0.8/TXD1/ MAT2.1	29[1]	I/O	**P0.8** — General purpose input/output digital pin.
		O	**TXD1** — Transmitter output for UART1.
		O	**MAT2.1** — PWM output for Timer 2, channel 1.
P0.9/RXD1/ MAT2.2	30[1]	I/O	**P0.9** — General purpose input/output digital pin.
		I	**RXD1** — Receiver input for UART1.
		O	**MAT2.2** — PWM output for Timer 2, channel 2.
P0.10/RTS1/ CAP1.0/AD0.3	35[3]	I/O	**P0.10** — General purpose input/output digital pin.
		O	**RTS1** — Request to Send output for UART1.
		I	**CAP1.0** — Capture input for Timer 1, channel 0.
		I	**AD0.3** — ADC 0, input 3.

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Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
P0.11/CTS1/ CAP1.1/AD0.4	36[3]	I/O	**P0.11** — General purpose input/output digital pin.
		I	**CTS1** — Clear to Send input for UART1.
		I	**CAP1.1** — Capture input for Timer 1, channel 1.
		I	**AD0.4** — ADC 0, input 4.
P0.12/DSR1/ MAT1.0/AD0.5	37[3]	I/O	**P0.12** — General purpose input/output digital pin.
		I	**DSR1** — Data Set Ready input for UART1.
		O	**MAT1.0** — PWM output for Timer 1, channel 0.
		I	**AD0.5** — ADC 0, input 5.
P0.13/DTR1/ MAT1.1	41[1]	I/O	**P0.13** — General purpose input/output digital pin.
		O	**DTR1** — Data Terminal Ready output for UART1.
		O	**MAT1.1** — PWM output for Timer 1, channel 1.
P0.14/DCD1/ SCK1/EINT1	44[4][5]	I/O	**P0.14** — General purpose input/output digital pin.
		I	**DCD1** — Data Carrier Detect input for UART1.
		I/O	**SCK1** — Serial Clock for SPI1. SPI clock output from master or input to slave.
		I	**EINT1** — External interrupt 1 input.
P0.15/RI1/ EINT2	45[4]	I/O	**P0.15** — General purpose input/output digital pin.
		I	**RI1** — Ring Indicator input for UART1.
		I	**EINT2** — External interrupt 2 input.
P0.16/EINT0/ MAT0.2	46[4]	I/O	**P0.16** — General purpose input/output digital pin.
		I	**EINT0** — External interrupt 0 input.
		O	**MAT0.2** — PWM output for Timer 0, channel 2.
P0.17/CAP1.2/ SCL1	47[6]	I/O	**P0.17** — General purpose input/output digital pin. The output is not open-drain.
		I	**CAP1.2** — Capture input for Timer 1, channel 2.
		I/O	**SCL1** — I^2C1 clock Input/output. This pin is an open-drain output if I^2C1 function is selected in the pin connect block.
P0.18/CAP1.3/ SDA1	48[6]	I/O	**P0.18** — General purpose input/output digital pin. The output is not open-drain.
		I	**CAP1.3** — Capture input for Timer 1, channel 3.
		I/O	**SDA1** — I^2C1 data Input/output. This pin is an open-drain output if I^2C1 function is selected in the pin connect block.
P0.19/MAT1.2/ MISO1	1[1]	I/O	**P0.19** — General purpose input/output digital pin.
		O	**MAT1.2** — PWM output for Timer 1, channel 2.
		I/O	**MISO1** — Master In Slave Out for SSP. Data input to SSP master or data output from SSP slave.
P0.20/MAT1.3/ MOSI1	2[1]	I/O	**P0.20** — General purpose input/output digital pin.
		O	**MAT1.3** — PWM output for Timer 1, channel 3.
		I/O	**MOSI1** — Master Out Slave for SSP. Data output from SSP master or data input to SSP slave.
P0.21/SSEL1/ MAT3.0	3[1]	I/O	**P0.21** — General purpose input/output digital pin.
		I	**SSEL1** — Slave Select for SPI1. Selects the SPI interface as a slave.
		O	**MAT3.0** — PWM output for Timer 3, channel 0.

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6. Functional description

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers (CISC). This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set.
- A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

The particular flash implementation in the LPC2101/02/03 allows for full speed execution also in ARM mode. It is recommended to program performance critical and short code sections in ARM mode. The impact on the overall code size will be minimal but the speed can be increased by 30 % over Thumb mode.

6.2 On-chip flash program memory

The LPC2101/02/03 incorporate a 8 kB, 16 kB or 32 kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed in system via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. The entire flash memory is available for user code as the bootloader resides in a separate memory.

The LPC2101/02/03 flash memory provides a minimum of 100,000 erase/write cycles and 20 years of data-retention memory.

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6.5 Interrupt controller

The VIC accepts all of the interrupt request inputs and categorizes them as FIQ, vectored IRQ, and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQ has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine does not need to branch into the interrupt service routine but can run from the interrupt vector location. If more than one request is assigned to the FIQ class, the FIQ service routine will read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the lowest.

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are pending, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

6.5.1 Interrupt sources

Each peripheral device has one interrupt line connected to the Vectored Interrupt Controller, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

6.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

The pin control module with its pin select registers defines the functionality of the microcontroller in a given hardware environment.

After reset all pins of Port 0 are configured as input with the following exceptions: If the DBGSEL pin is HIGH (Debug mode enabled), the JTAG pins will assume their JTAG functionality for use with EmbeddedICE and cannot be configured via the pin connect block.

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6.7 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

LPC2101/02/03 introduce accelerated GPIO functions over prior LPC2000 devices:

- GPIO registers are relocated to the ARM local bus for the fastest possible I/O timing.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte addressable.
- Entire port value can be written in one instruction.

6.7.1 Features

- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.8 10-bit ADC

The LPC2101/02/03 contain one ADC. It is a single 10-bit successive approximation ADC with eight channels.

6.8.1 Features

- Measurement range of 0 V to 3.3 V.
- Each converter capable of performing more than 400,000 10-bit samples per second.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or Timer Match signal.
- Every analog input has a dedicated result register to reduce interrupt overhead.

6.9 UARTs

The LPC2101/02/03 each contain two UARTs. In addition to standard transmit and receive data lines, UART1 also provides a full modem control handshake interface.

Compared to previous LPC2000 microcontrollers, UARTs in LPC2101/02/03 include a fractional baud rate generator for both UARTs. Standard baud rates such as 115200 can be achieved with any crystal frequency above 2 MHz.

6.9.1 Features

- 16 byte Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1, 4, 8, and 14 bytes

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- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTs.
- UART1 is equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).

6.10 I^{2}C-bus serial I/O controllers

The LPC2101/02/03 each contain two I^{2}C-bus controllers.

The I^{2}C-bus is bidirectional, for inter-IC control using only two wires: a Serial Clock Line (SCL), and a Serial Data Line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., LCD driver) or a transmitter with the capability to both receive and send information such as serial memory. Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^{2}C-bus is a multi-master bus, it can be controlled by more than one bus master connected to it.

The I^{2}C-bus implemented in LPC2101/02/03 supports bit rates up to 400 kbit/s (Fast I^{2}C-bus).

6.10.1 Features

- Compliant with standard I^{2}C-bus interface.
- Easy to configure as Master, Slave, or Master/Slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^{2}C-bus can also be used for test and diagnostic purposes.

6.11 SPI serial I/O controller

The LPC2101/02/03 each contain one SPI controller. The SPI is a full duplex serial interface, designed to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends 8 bits to 16 bits of data to the slave, and the slave always sends 8 bits to 16 bits of data to the master.

6.11.1 Features

- Compliant with SPI specification.
- Synchronous, Serial, Full Duplex, Communication.

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- Combined SPI master and slave.
- Maximum data bit rate of one eighth of the input clock rate.

6.12 SSP serial I/O controller

The LPC2101/02/03 each contain one SSP. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. However, only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with data frames of 4 bits to 16 bits flowing from the master to the slave and from the slave to the master. Often only one of these data streams carries meaningful data.

6.12.1 Features

- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor's Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- Four bits to 16 bits per frame

6.13 General purpose 32-bit timers/external event counters

The Timer/Counter is designed to count cycles of the Peripheral Clock (PCLK) or an externally supplied clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with 'or' and 'and', as well as 'broadcast' functions among them.

The LPC2101/02/03 can count external events on one of the capture inputs if the minimum external pulse is equal or longer than a period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs or used as external interrupts.

6.13.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- External event counter or timer operation.
- Four 32-bit capture channels per timer/counter that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Four external outputs per timer/counter corresponding to match registers, with the following capabilities:
  - Set LOW on match.

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6.17.4 Code security (Code Read Protection - CRP)

This feature of the LPC2101/02/03 allows user to enable different levels of security in the system so that access to the on-chip flash and use of the JTAG and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

Implemented in bootloader code version 2.21 are three levels of the Code Read Protection:

1. CRP1 disables access to chip via the JTAG and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to chip via the JTAG and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to chip via the JTAG pins and the ISP. This mode effectively disables ISP override using P0.14 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART0.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

Remark: Parts LPC2101/02/03 Revision '-' have CRP2 enabled only (bootloader code version 2.2).

6.17.5 External interrupt inputs

The LPC2101/02/03 include up to three edge or level sensitive external interrupt inputs as selectable pin functions. When the pins are combined, external events can be processed as three independent interrupt signals. The external interrupt inputs can optionally be used to wake-up the processor from Power-down mode and Deep power-down mode.

Additionally all 10 capture input pins can also be used as external interrupts without the option to wake the device up from Power-down mode.

6.17.6 Memory mapping control

The memory mapping control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the on-chip flash memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

6.17.7 Power control

The LPC2101/02/03 supports three reduced power modes: Idle mode, Power-down mode, and Deep power-down mode.

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In Idle mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers, and internal buses.

In Power-down mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Power-down mode and the logic levels of chip output pins remain static. The Power-down mode can be terminated and normal operation resumed by either a reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Power-down mode reduces chip power consumption to nearly zero.

Selecting an external 32 kHz clock instead of the PCLK as a clock-source for the on-chip RTC will enable the microcontroller to have the RTC active during Power-down mode. Power-down current is increased with RTC active. However, it is significantly lower than in Idle mode.

In Deep-power down mode all power is removed from the internal chip logic except for the RTC module, the I/O ports, the SRAM, and the 32 kHz external oscillator. For additional power savings, SRAM and the 32 kHz oscillator can be powered down individually. The Deep power-down mode produces the lowest possible power consumption without actually removing power from the entire chip. In Deep power-down mode, the contents of registers and memory are not preserved except for SRAM, if selected, and three general purpose registers. Therefore, to resume operations, a full chip reset process is required.

A power selector module switches the RTC power supply from VBAT to $V_{DD(1V8)}$ whenever the core voltage is present on pin $V_{DD(1V8)}$ to conserve battery power.

A power control for peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings during Active and Idle mode.

6.17.8 APB

The APB divider determines the relationship between the processor clock (CCLK) and the clock used by peripheral devices (PCLK). The APB divider serves two purposes. The first is to provide peripherals with the desired PCLK via APB so that they can operate at the speed chosen for the ARM processor. In order to achieve this, the APB may be slowed down to $\frac{1}{2}$ to $\frac{1}{4}$ of the processor clock rate. Because the APB must work properly at power-up (and its timing cannot be altered if it does not work since the APB divider control registers reside on the APB), the default condition at reset is for the APB to run at $\frac{1}{4}$ of the processor clock rate. The second purpose of the APB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the APB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

6.18 Emulation and debugging

The LPC2101/02/03 support emulation and debugging via a JTAG serial port.

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6.18.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol converter. The EmbeddedICE protocol converter converts the remote debug protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a debug communication channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The debug communication channel is accessed as a coprocessor 14 by the program running on the ARM7TDMI-S core. The debug communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic. The JTAG clock (TCK) must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.

6.18.2 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC, which is present in the EmbeddedICE logic. The LPC2101/02/03 contain a specific configuration of RealMonitor software programmed into the on-chip boot ROM memory.

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8. Static characteristics

Table 5. Static characteristics

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	1.65	1.8	1.95	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	2.6[4]	3.3	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage			2.6[5]	3.3	3.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT			2.0[6]	3.3	3.6	V
Standard port pins, $\overline{RST}$, RTCK							
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	3	μA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; no pull-down		-	-	3	μA
I_{OZ}	OFF-state output current	V_O = 0 V, $V_O = V_{DD(3V3)}$; no pull-up/down		-	-	3	μA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; T_j < 125 °C		-	-	100	mA
V_I	input voltage	pin configured to provide a digital function; $V_{DD(3V3)}$ and $V_{DDA} \geq 3.0$ V	[7][8][9]	0	-	5.5	V
		pin configured to provide a digital function; $V_{DD(3V3)}$ and $V_{DDA} < 3.0$ V	[7][8][9]	0		$V_{DD(3V3)}$	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	[10]	$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = −4 mA	[10]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V	[10]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[10]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[11]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DDA}$	[11]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V[12]		10	50	150	μA

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Table 5. Static characteristics *...continued*

T_{amb}= −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$V_{o(XTAL2)}$	output voltage on pin XTAL2		0	-	1.8	V
$V_{i(RTCX1)}$	input voltage on pin RTCX1		0	-	1.8	V
$V_{o(RTCX2)}$	output voltage on pin RTCX2		0	-	1.8	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Core and internal rail.

[3] External rail.

[4] If $V_{DD(3V3)}$ < 3.0 V, the I/O pins are not 5 V tolerant, and the ADC input voltage is limited to V_{DDA} = 3.0 V.

[5] If V_{DDA} < 3.0 V, the I/O pins are not 5 V tolerant.

[6] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[7] Including voltage on outputs in 3-state mode.

[8] $V_{DD(3V3)}$ supply voltages must be present.

[9] 3-state outputs go into 3-state mode when $V_{DD(3V3)}$ is grounded.

[10] Accounts for 100 mV voltage drop in all supply lines.

[11] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[12] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V. V_{DDA} ≥ 3.0 V and $V_{DD(3V3)}$ ≥ 3.0 V.

[13] Applies to P0.25:16.

[14] Battery supply current on pin VBAT.

[15] Input leakage current to V_{SS}.

Table 6. ADC static characteristics

V_{DDA} = 2.5 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified. ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DDA}	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	[1][2][3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity	[1][4]	-	-	±2	LSB
E_O	offset error	[1][5]	-	-	±3	LSB
E_G	gain error	[1][6]	-	-	±0.5	%
E_T	absolute error	[1][7]	-	-	±4	LSB

[1] Conditions: V_{SSA} = 0 V, V_{DDA} = 3.3 V and $V_{DD(3V3)}$ = 3.3 V for 10-bit resolution at full speed; V_{DDA} = 2.6 V, $V_{DD(3V3)}$ = 2.6 V for 8-bit resolution at full speed.

[2] The ADC is monotonic, there are no missing codes.

[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 5.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 5.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 5.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 5.

[7] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 5.

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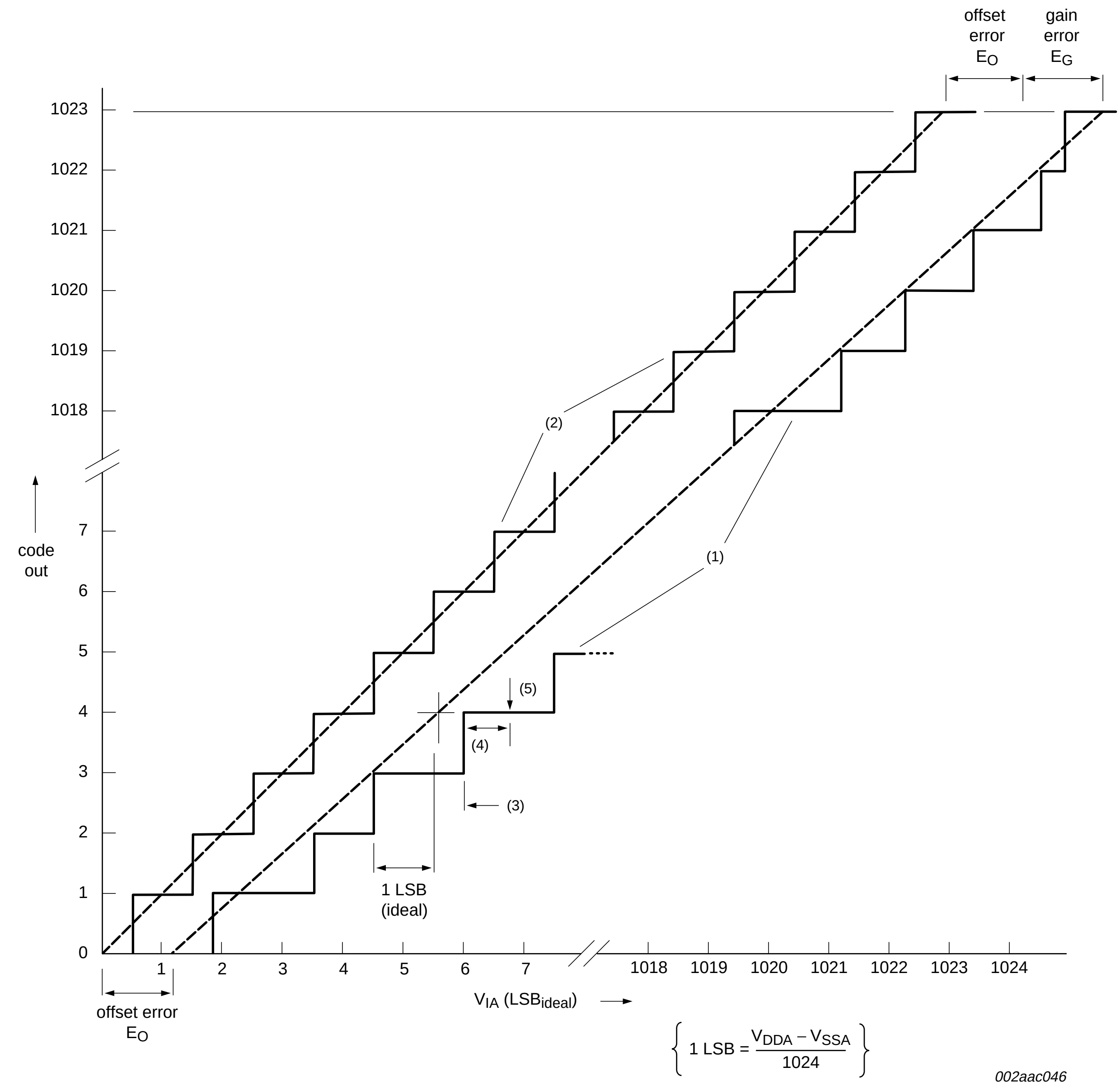

(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 5. ADC conversion characteristics

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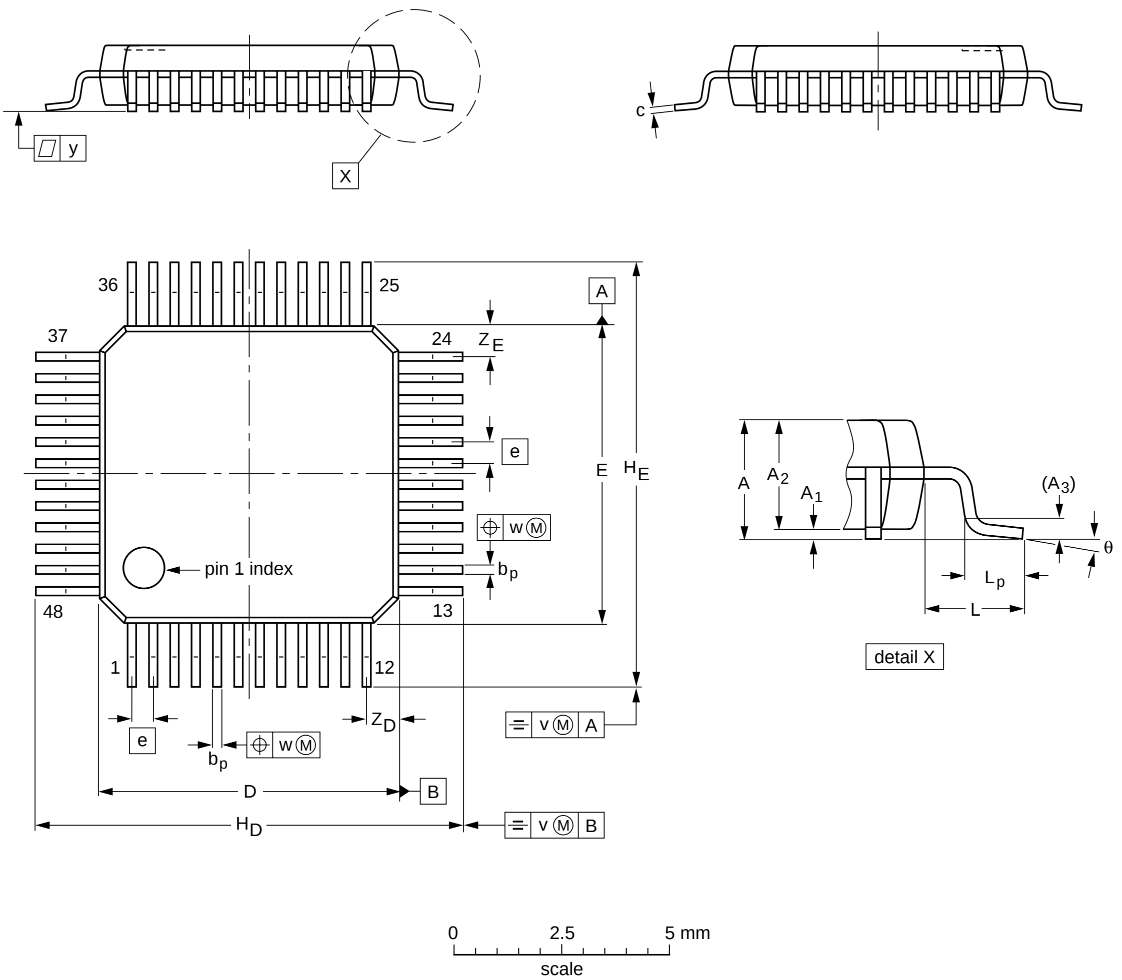
11. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 10. Package outline SOT313-2 (LQFP48)

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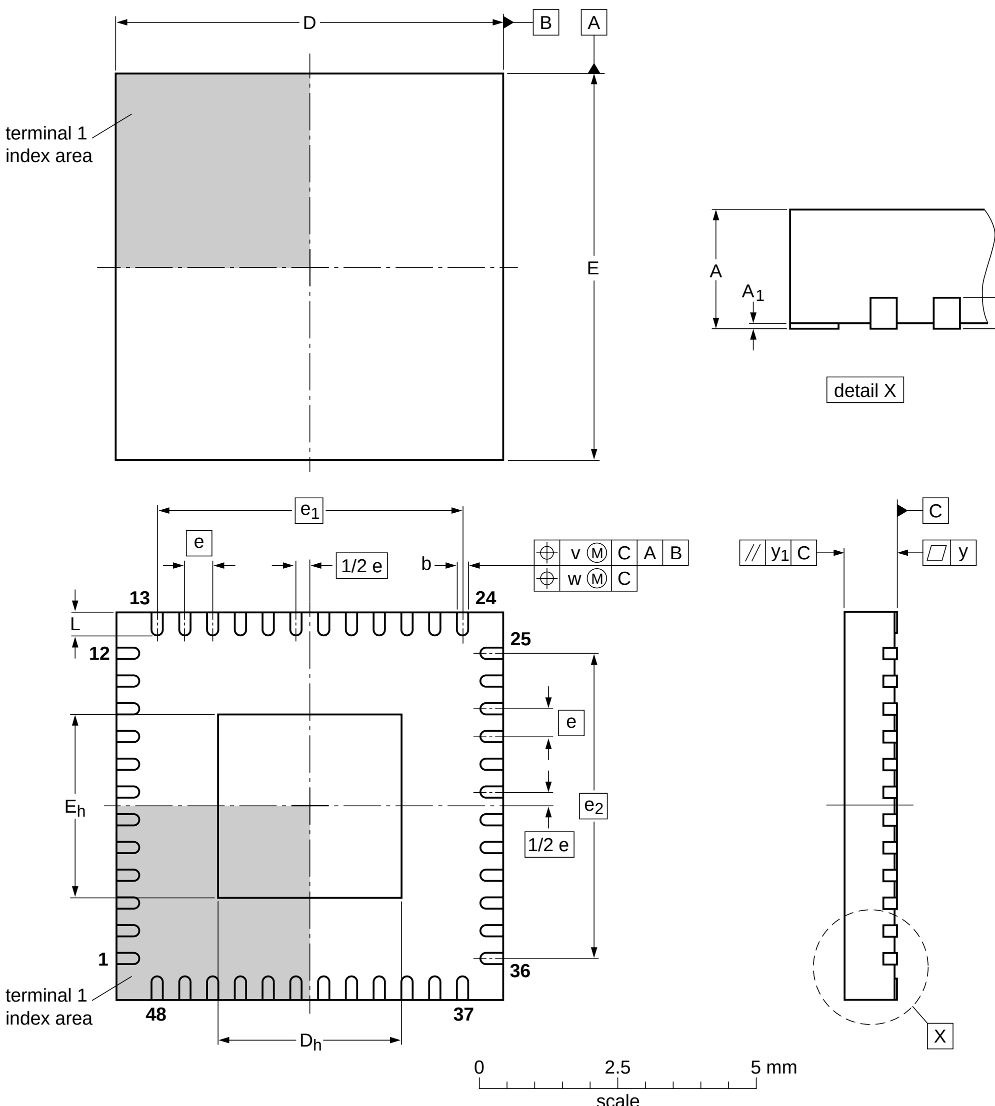
HVQFN48: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 x 7 x 0.85 mm **SOT619-7**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	7.1 6.9	3.45 3.15	7.1 6.9	3.45 3.15	0.5	5.5	5.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT619-7	- - -	MO-220	- - -			~~05-10-24~~ 05-10-25

Fig 11. Package outline SOT619-7 (HVQFN48)

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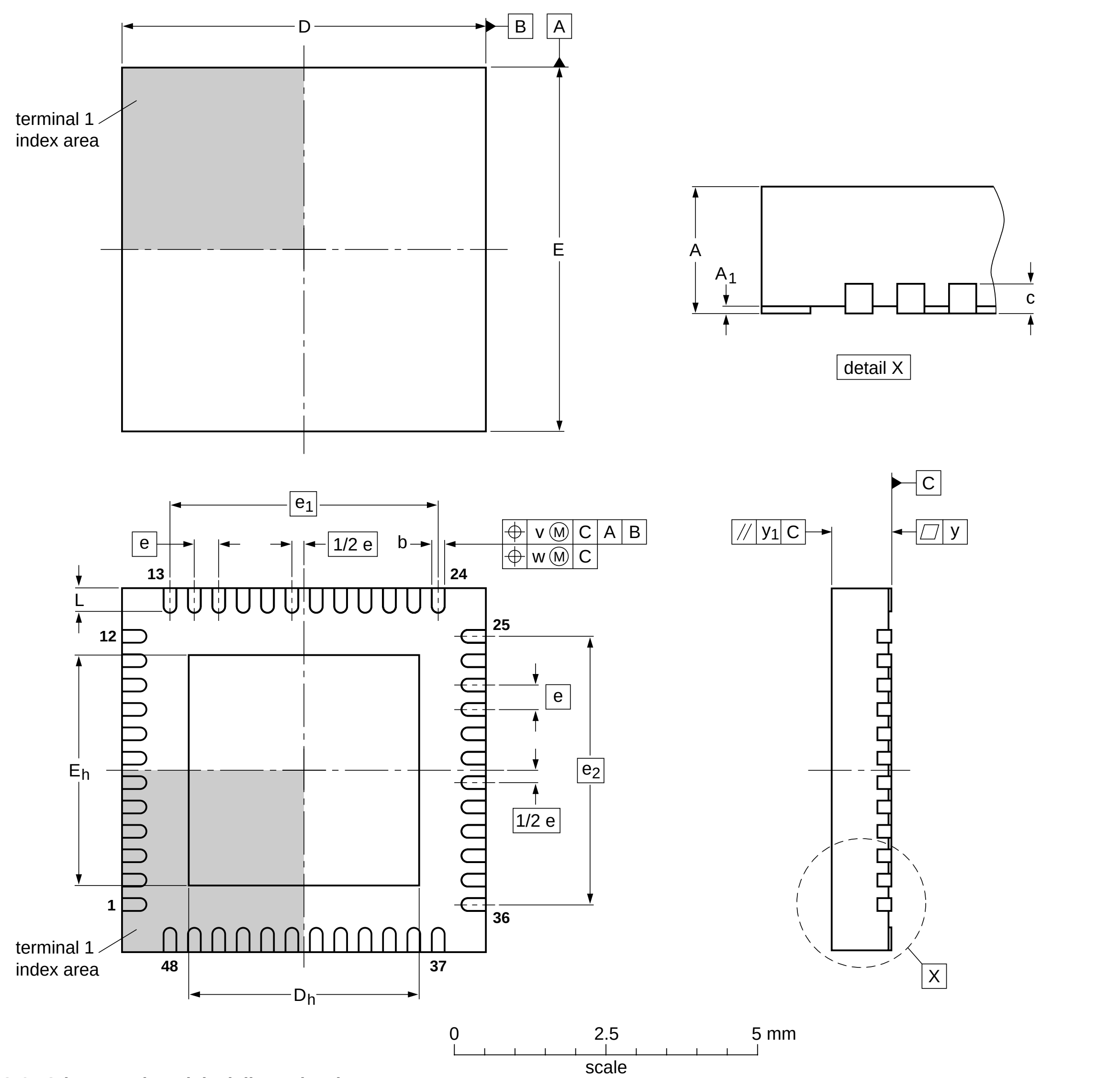
HVQFN48: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 6 x 6 x 0.85 mm **SOT778-3**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.25 0.15	0.2	6.1 5.9	3.95 3.65	6.1 5.9	3.95 3.65	0.4	4.4	4.4	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT778-3	- - -	- - -	- - -			~~04-06-16~~ 04-06-23

Fig 12. Package outline SOT778-3 (HVQFN48)

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12. Abbreviations

Table 8. Acronym list

Acronym	Description
ADC	Analog-to-Digital Converter
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
DCC	Debug Communications Channel
DSP	Digital Signal Processor
FIFO	First In, First Out
FIQ	Fast Interrupt reQuest
GPIO	General Purpose Input/Output
IAP	In-Application Programming
IRQ	Interrupt Request
ISP	In-System Programming
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSI	Synchronous Serial Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
VIC	Vectored Interrupt Controller

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13. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2101_02_03_4	20090602	Product data sheet		LPC2101_02_03_3
Modifications:	• Section 6.17.4 "Code security (Code Read Protection - CRP)": added description of three CRP levels (applicable to Revision A and higher). • Section 6.17.7 "Power control": added description of Deep power-down mode (applicable to Revision A and higher). • Section 10.1 "XTAL1 input" added. • Section 10.2 "XTAL and RTC Printed Circuit Board (PCB) layout guidelines" added. • Figure 6, Figure 7, Figure 8: added power consumption data for Deep power-down mode (applicable to Revision A and higher). • Table 3: added table note 7. • Table 3: modified description of P0.14, RTCX1, RTCX2, XTAL1, XTAL2, JTAG, and DBGSEL pins. • Table 4: modified value for $V_{DD(3V3)}$. • Table 5: added and modified values for V_{hys}. • Table 5: Voltage range for pins $V_{DD(3V3)}$ and V_{DDA} extended to 2.6 V.			
LPC2101_02_03_3	20081007	Product data sheet	-	LPC2101_02_03_2
Modifications:	• Updated data sheet status to Product data sheet. • Table 1 and Table 2: added LPC2102FHN48 and LPC2103FHN48. • Table 1, Table 2, Table 3 and related figures: removed LPC2103FA44. • Table 3: updated pad descriptions. • Table 3: updated description of pin 47, SCL1. • Table 3: updated description of pins V_{DDA} and $V_{DD(1V8)}$. • Table 4: changed storage temperature range from –40 °C/125 °C to –65 °C/150 °C. • Table 5: added or modified values for $I_{DD(act)}$, $I_{DD(pd)}$, I_{BATpd}, I_{BATact}. • Table 5: removed "CCLK = 10 MHz" and associated values for $I_{DD(act)}$. • Section 5: added Figure 3. • Section 11: added Figure 11.			
LPC2101_02_03_2	20071218	Preliminary data sheet	-	LPC2101_02_03_1
LPC2101_02_03_1	20060118	Preliminary data sheet	-	-

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16. Contents

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