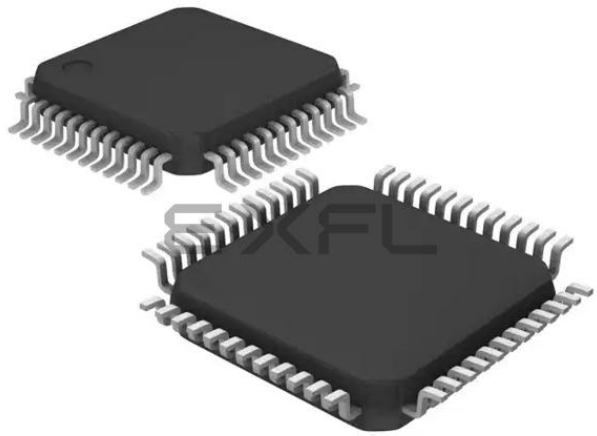


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	70MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2103fbd48-151

- Two 16-bit timers/external event counters with combined three capture and seven compare channels.
- Low power Real-Time Clock (RTC) with independent power and dedicated 32 kHz clock input.
- Multiple serial interfaces including two UARTs (16C550), two Fast I^2C-buses (400 kbit/s), SPI and SSP with buffering and variable data length capabilities.
- Vectored interrupt controller with configurable priorities and vector addresses.
- Up to thirty-two, 5 V tolerant fast general purpose I/O pins.
- Up to 13 edge or level sensitive external interrupt pins available.
- 70 MHz maximum CPU clock available from programmable on-chip PLL with a possible input frequency of 10 MHz to 25 MHz and a settling time of 100 µs.
- On-chip integrated oscillator operates with an external crystal in the range from 1 MHz to 25 MHz.
- Power saving modes include Idle mode, Power-down mode with RTC active, and Power-down mode.
- Individual enable/disable of peripheral functions as well as peripheral clock scaling for additional power optimization.
- Processor wake-up from Power-down and Deep power-down (Revision A and higher) mode via external interrupt or RTC.

3. Ordering information

Table 1. Ordering information

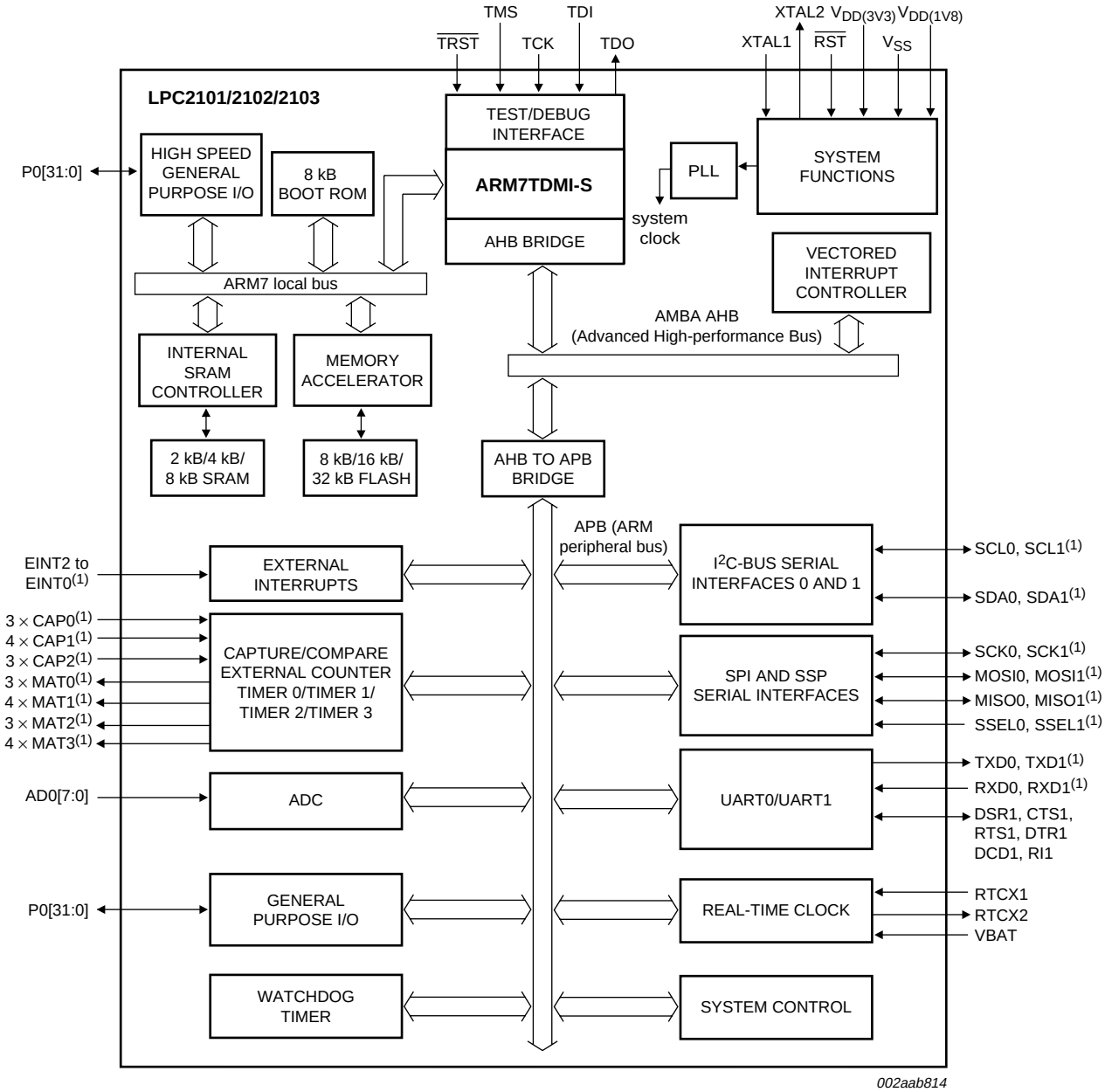
Type number	Package		
	Name	Description	Version
LPC2101FBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2102FBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2103FBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2102FHN48	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 × 7 × 0.85 mm	SOT619-7
LPC2103FHN48	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 × 7 × 0.85 mm	SOT619-7
LPC2103FHN48H	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 6 × 6 × 0.85 mm	SOT778-3

3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	RAM	ADC	Temperature range (°C)
LPC2101FBD48	8 kB	2 kB	8 inputs	–40 to +85
LPC2102FBD48	16 kB	4 kB	8 inputs	–40 to +85
LPC2103FBD48	32 kB	8 kB	8 inputs	–40 to +85
LPC2102FHN48	16 kB	4 kB	8 inputs	–40 to +85
LPC2103FHN48	32 kB	8 kB	8 inputs	–40 to +85
LPC2103FHN48H	32 kB	8 kB	8 inputs	–40 to +85

4. Block diagram



(1) Pins shared with GPIO.

Fig 1. Block diagram

5. Pinning information

5.1 Pinning

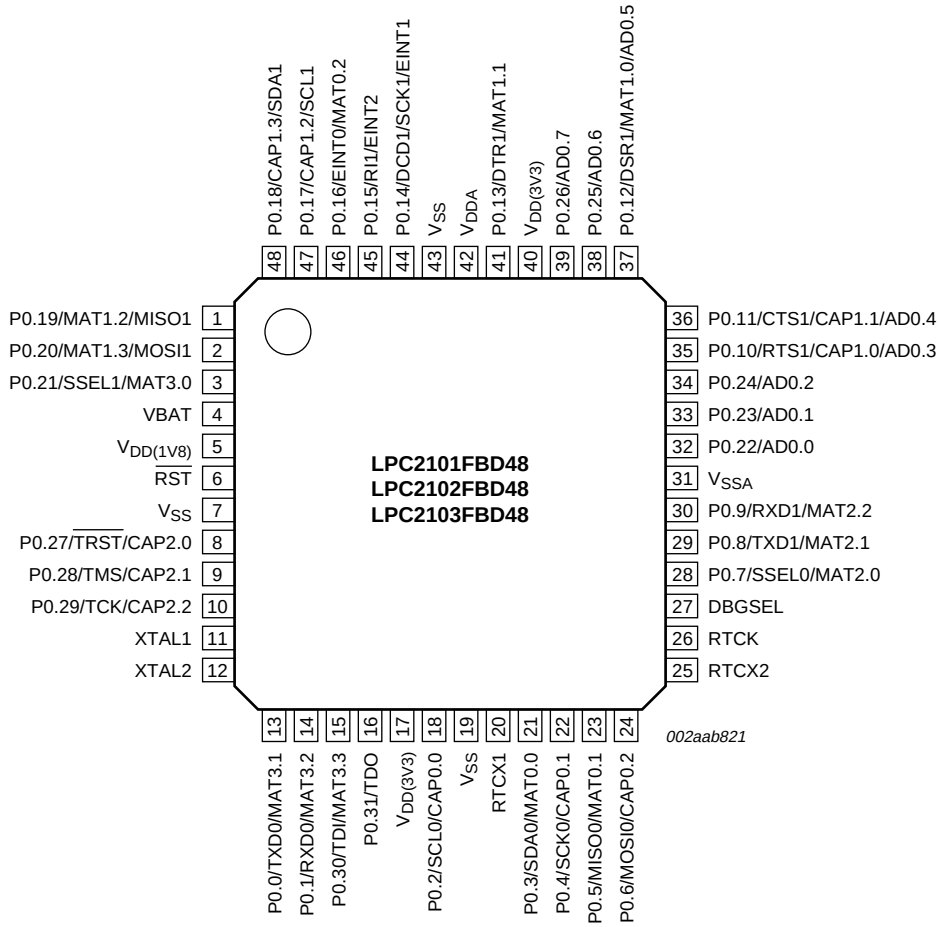


Fig 2. Pin configuration (LQFP48)

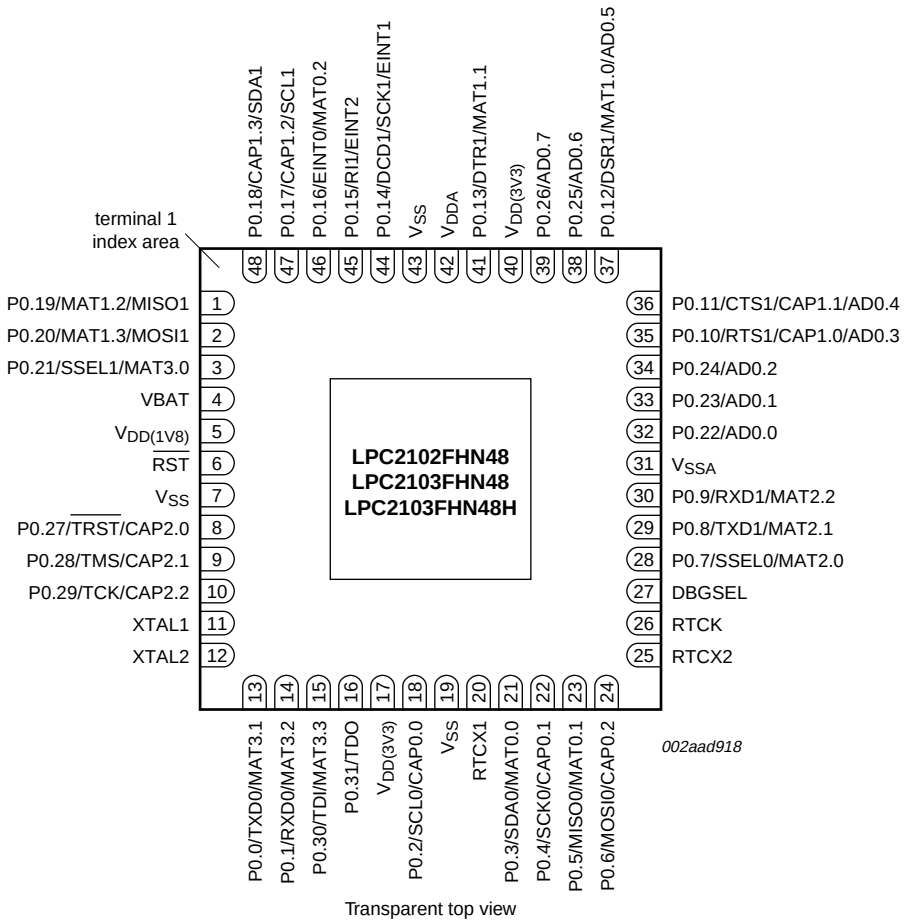


Fig 3. Pin configuration (HVQFN48)

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
P0.22/AD0.0	32[3]	I/O	**P0.22 —** General purpose input/output digital pin.
		I	**AD0.0 —** ADC 0, input 0.
P0.23/AD0.1	33[3]	I/O	**P0.23 —** General purpose input/output digital pin.
		I	**AD0.1 —** ADC 0, input 1.
P0.24/AD0.2	34[3]	I/O	**P0.24 —** General purpose input/output digital pin.
		I	**AD0.2 —** ADC 0, input 2.
P0.25/AD0.6	38[3]	I/O	**P0.25 —** General purpose input/output digital pin.
		I	**AD0.6 —** ADC 0, input 6.
P0.26/AD0.7	39[3]	I/O	**P0.26 —** General purpose input/output digital pin.
		I	**AD0.7 —** ADC 0, input 7.
P0.27/$\overline{\text{TRST}}$/CAP2.0	8[1]	I/O	**P0.27 —** General purpose input/output digital pin.
		I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface. If DBGSEL is HIGH, this pin is automatically configured for use with EmbeddedICE (Debug mode).
		I	**CAP2.0 —** Capture input for Timer 2, channel 0.
P0.28/TMS/CAP2.1	9[1]	I/O	**P0.28 —** General purpose input/output digital pin.
		I	**TMS —** Test Mode Select for JTAG interface. If DBGSEL is HIGH, this pin is automatically configured for use with EmbeddedICE (Debug mode).
		I	**CAP2.1 —** Capture input for Timer 2, channel 1.
P0.29/TCK/CAP2.2	10[1]	I/O	**P0.29 —** General purpose input/output digital pin.
		I	**TCK —** Test Clock for JTAG interface. This clock must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate. If DBGSEL is HIGH, this pin is automatically configured for use with EmbeddedICE (Debug mode).
		I	**CAP2.2 —** Capture input for Timer 2, channel 2.
P0.30/TDI/MAT3.3	15[1]	I/O	**P0.30 —** General purpose input/output digital pin.
		I	**TDI —** Test Data In for JTAG interface. If DBGSEL is HIGH, this pin is automatically configured for use with EmbeddedICE (Debug mode).
		O	**MAT3.3 —** PWM output 3 for Timer 3.
P0.31/TDO	16[1]	O	**P0.31 —** General purpose output only digital pin.
		O	**TDO —** Test Data Out for JTAG interface. If DBGSEL is HIGH, this pin is automatically configured for use with EmbeddedICE (Debug mode).
RTCX1	20[7][8]	I	Input to the RTC oscillator circuit. Input voltage must not exceed 1.8 V.
RTCX2	25[7][8]	O	Output from the RTC oscillator circuit.
RTCK	26[7]	I/O	**Returned test clock output:** Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up.
XTAL1	11	I	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTAL2	12	O	Output from the oscillator amplifier.
DBGSEL	27	I	**Debug select:** When LOW, the part operates normally. When externally pulled HIGH at reset, P0.27 to P0.31 are configured as JTAG port, and the part is in Debug mode[9]. Input with internal pull-down.
$\overline{\text{RST}}$	6	I	**External reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.

6.3 On-chip static RAM

On-chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8-bits, 16-bits, and 32-bits. The LPC2101/02/03 provide 2 kB, 4 kB or 8 kB of static RAM.

6.4 Memory map

The LPC2101/02/03 memory map incorporates several distinct regions, as shown in Figure 4.

In addition, the CPU interrupt vectors may be re-mapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in Section 6.17 "System control".

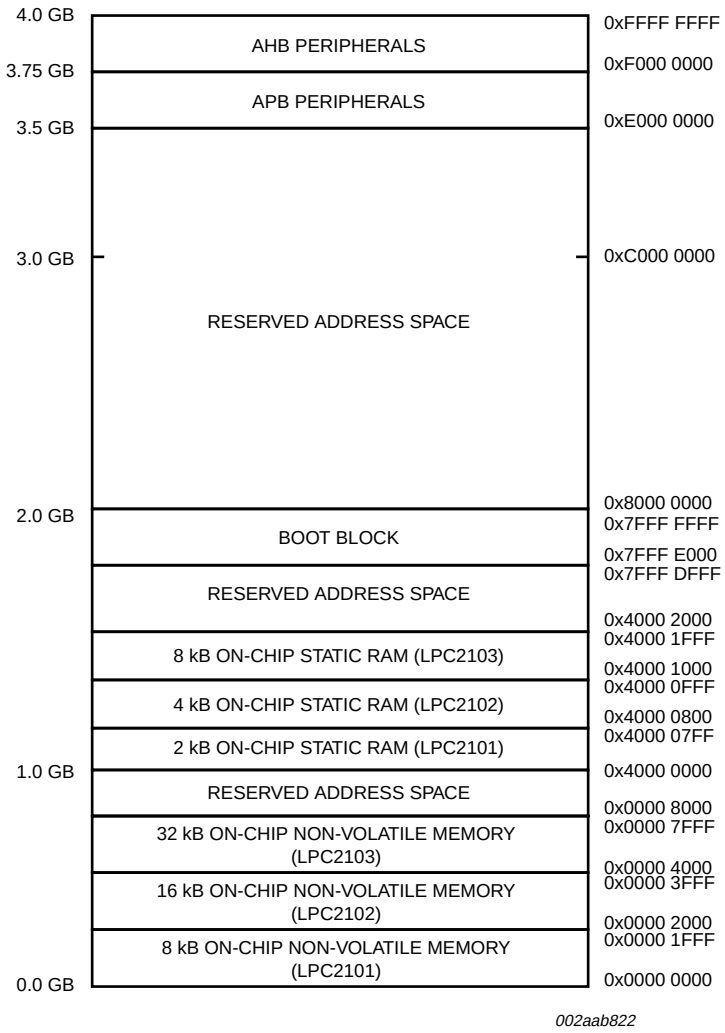


Fig 4. LPC2101/02/03 memory map

6.7 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

LPC2101/02/03 introduce accelerated GPIO functions over prior LPC2000 devices:

- GPIO registers are relocated to the ARM local bus for the fastest possible I/O timing.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte addressable.
- Entire port value can be written in one instruction.

6.7.1 Features

- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.8 10-bit ADC

The LPC2101/02/03 contain one ADC. It is a single 10-bit successive approximation ADC with eight channels.

6.8.1 Features

- Measurement range of 0 V to 3.3 V.
- Each converter capable of performing more than 400,000 10-bit samples per second.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or Timer Match signal.
- Every analog input has a dedicated result register to reduce interrupt overhead.

6.9 UARTs

The LPC2101/02/03 each contain two UARTs. In addition to standard transmit and receive data lines, UART1 also provides a full modem control handshake interface.

Compared to previous LPC2000 microcontrollers, UARTs in LPC2101/02/03 include a fractional baud rate generator for both UARTs. Standard baud rates such as 115200 can be achieved with any crystal frequency above 2 MHz.

6.9.1 Features

- 16 byte Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1, 4, 8, and 14 bytes

- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTs.
- UART1 is equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).

6.10 I^2C-bus serial I/O controllers

The LPC2101/02/03 each contain two I^2C-bus controllers.

The I^2C-bus is bidirectional, for inter-IC control using only two wires: a Serial Clock Line (SCL), and a Serial Data Line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., LCD driver) or a transmitter with the capability to both receive and send information such as serial memory. Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C-bus is a multi-master bus, it can be controlled by more than one bus master connected to it.

The I^2C-bus implemented in LPC2101/02/03 supports bit rates up to 400 kbit/s (Fast I^2C-bus).

6.10.1 Features

- Compliant with standard I^2C-bus interface.
- Easy to configure as Master, Slave, or Master/Slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can also be used for test and diagnostic purposes.

6.11 SPI serial I/O controller

The LPC2101/02/03 each contain one SPI controller. The SPI is a full duplex serial interface, designed to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends 8 bits to 16 bits of data to the slave, and the slave always sends 8 bits to 16 bits of data to the master.

6.11.1 Features

- Compliant with SPI specification.
- Synchronous, Serial, Full Duplex, Communication.

- Combined SPI master and slave.
- Maximum data bit rate of one eighth of the input clock rate.

6.12 SSP serial I/O controller

The LPC2101/02/03 each contain one SSP. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. However, only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with data frames of 4 bits to 16 bits flowing from the master to the slave and from the slave to the master. Often only one of these data streams carries meaningful data.

6.12.1 Features

- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor's Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- Four bits to 16 bits per frame

6.13 General purpose 32-bit timers/external event counters

The Timer/Counter is designed to count cycles of the Peripheral Clock (PCLK) or an externally supplied clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with 'or' and 'and', as well as 'broadcast' functions among them.

The LPC2101/02/03 can count external events on one of the capture inputs if the minimum external pulse is equal or longer than a period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs or used as external interrupts.

6.13.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- External event counter or timer operation.
- Four 32-bit capture channels per timer/counter that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Four external outputs per timer/counter corresponding to match registers, with the following capabilities:
  - Set LOW on match.

- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal pre-scaler.
- Selectable time period from ($T_{PCLK} \times 256 \times 4$) to ($T_{PCLK} \times 2^{32} \times 4$) in multiples of $T_{PCLK} \times 4$.

6.16 Real-time clock

The Real-Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.16.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra-low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Can use either the RTC dedicated 32 kHz oscillator input or clock derived from the external crystal/oscillator input at XTAL1. The programmable reference clock divider allows fine adjustment of the RTC.
- Dedicated power supply pin can be connected to a battery or the main 3.3 V.

6.17 System control

6.17.1 Crystal oscillator

The on-chip integrated oscillator operates with external crystal in range of 1 MHz to 25 MHz. The oscillator output frequency is called f_{osc} and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. f_{osc} and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.17.2 “PLL” and Section 10.1 “XTAL1 input” for additional information.

6.17.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 70 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 µs.

6.17.4 Code security (Code Read Protection - CRP)

This feature of the LPC2101/02/03 allows user to enable different levels of security in the system so that access to the on-chip flash and use of the JTAG and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

Implemented in bootloader code version 2.21 are three levels of the Code Read Protection:

1. CRP1 disables access to chip via the JTAG and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to chip via the JTAG and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to chip via the JTAG pins and the ISP. This mode effectively disables ISP override using P0.14 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART0.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

Remark: Parts LPC2101/02/03 Revision '-' have CRP2 enabled only (bootloader code version 2.2).

6.17.5 External interrupt inputs

The LPC2101/02/03 include up to three edge or level sensitive external interrupt inputs as selectable pin functions. When the pins are combined, external events can be processed as three independent interrupt signals. The external interrupt inputs can optionally be used to wake-up the processor from Power-down mode and Deep power-down mode.

Additionally all 10 capture input pins can also be used as external interrupts without the option to wake the device up from Power-down mode.

6.17.6 Memory mapping control

The memory mapping control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the on-chip flash memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

6.17.7 Power control

The LPC2101/02/03 supports three reduced power modes: Idle mode, Power-down mode, and Deep power-down mode.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	–0.5	+2.5	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	–0.5	+4.6	V
V_{DDA}	analog 3.3 V pad supply voltage			–0.5	+4.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT	for the RTC		–0.5	+4.6	V
V_{IA}	analog input voltage		[4]	–0.5	+5.1	V
V_I	input voltage	5 V tolerant I/O pins	[5][6]	–0.5	+6.0	V
		other I/O pins	[5]	–0.5	V_{DD} + 0.5[7]	V
I_{DD}	supply current		[8]	-	100[9]	mA
I_{SS}	ground current		[10]	-	100[9]	mA
T_{stg}	storage temperature		[11]	–65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM)		–4000	+4000	V[12]
		Machine Model (MM)		–200	+200	V[13]
		Charged Device Model (CDM)		–800	+800	V[14]

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Core and internal rail.

[3] External rail.

[4] On ADC related pins.

[5] Including voltage on outputs in 3-state mode.

[6] Only valid when the $V_{DD(3V3)}$ supply voltage is present.

[7] Not to exceed 4.6 V.

[8] Per supply pin.

[9] The peak current is limited to 25 times the corresponding maximum current.

[10] Per ground pin.

[11] Dependent on package type.

[12] Performed per AEC-Q100-002.

[13] Performed per AEC-Q100-003.

[14] Performed per AEC-Q100-011.

8. Static characteristics

Table 5. Static characteristics

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	1.65	1.8	1.95	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	2.6[4]	3.3	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage			2.6[5]	3.3	3.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT			2.0[6]	3.3	3.6	V
Standard port pins, $\overline{RST}$, RTCK							
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	3	µA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; no pull-down		-	-	3	µA
I_{OZ}	OFF-state output current	V_O = 0 V, $V_O = V_{DD(3V3)}$; no pull-up/down		-	-	3	µA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; T_j < 125 °C		-	-	100	mA
V_I	input voltage	pin configured to provide a digital function; $V_{DD(3V3)}$ and $V_{DDA} \geq 3.0$ V	[7][8][9]	0	-	5.5	V
		pin configured to provide a digital function; $V_{DD(3V3)}$ and V_{DDA} < 3.0 V	[7][8][9]	0		$V_{DD(3V3)}$	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	[10]	$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = −4 mA	[10]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V	[10]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[10]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[11]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DDA}$	[11]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V[12]		10	50	150	µA

Table 5. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$V_{o(XTAL2)}$	output voltage on pin XTAL2		0	-	1.8	V
$V_{i(RTCX1)}$	input voltage on pin RTCX1		0	-	1.8	V
$V_{o(RTCX2)}$	output voltage on pin RTCX2		0	-	1.8	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Core and internal rail.

[3] External rail.

[4] If $V_{DD(3V3)}$ < 3.0 V, the I/O pins are not 5 V tolerant, and the ADC input voltage is limited to V_{DDA} = 3.0 V.

[5] If V_{DDA} < 3.0 V, the I/O pins are not 5 V tolerant.

[6] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[7] Including voltage on outputs in 3-state mode.

[8] $V_{DD(3V3)}$ supply voltages must be present.

[9] 3-state outputs go into 3-state mode when $V_{DD(3V3)}$ is grounded.

[10] Accounts for 100 mV voltage drop in all supply lines.

[11] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[12] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V. $V_{DDA} \geq 3.0$ V and $V_{DD(3V3)} \geq 3.0$ V.

[13] Applies to P0.25:16.

[14] Battery supply current on pin VBAT.

[15] Input leakage current to V_{SS}.

Table 6. ADC static characteristics

V_{DDA} = 2.5 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified. ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DDA}	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	[1][2][3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity	[1][4]	-	-	±2	LSB
E_O	offset error	[1][5]	-	-	±3	LSB
E_G	gain error	[1][6]	-	-	±0.5	%
E_T	absolute error	[1][7]	-	-	±4	LSB

[1] Conditions: V_{SSA} = 0 V, V_{DDA} = 3.3 V and $V_{DD(3V3)}$ = 3.3 V for 10-bit resolution at full speed; V_{DDA} = 2.6 V, $V_{DD(3V3)}$ = 2.6 V for 8-bit resolution at full speed.

[2] The ADC is monotonic, there are no missing codes.

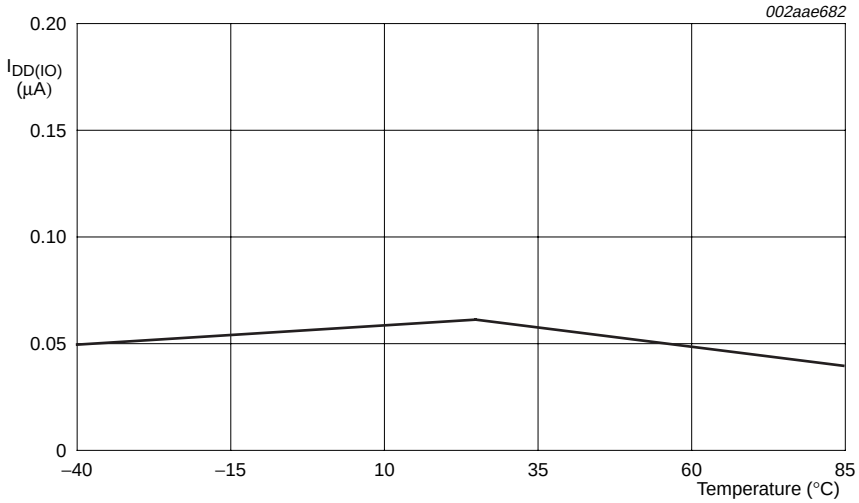
[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 5.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 5.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 5.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 5.

[7] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 5.



Test conditions: Deep power-down mode entered; RTC off; SRAM off; $V_{DD(3V3)}$ = 3.3 V; $V_{DD(1V8)}$ = 1.8 V; $V_{i(BAT)}$ = V_{DDA} = 3.3 V.

Fig 8. I/O supply current $I_{DD(IO)}$ measured at different temperatures

9. Dynamic characteristics

Table 7. Dynamic characteristics

T_{amb} = 0 °C to 70 °C for commercial applications, −40 °C to +85 °C for industrial applications, $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges[1].

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
External clock						
f_{osc}	oscillator frequency		10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	100	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0.2 and P0.3)						
$t_{r(o)}$	output rise time		-	10	-	ns
$t_{f(o)}$	output fall time		-	10	-	ns
I^2C-bus pins (P0.2 and P0.3)						
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	$20 + 0.1 \times C_b$[3]	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.

10. Application information

10.1 XTAL1 input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV (RMS) is needed. For more details see the *LPC2101/02/03 User manual UM10161*.

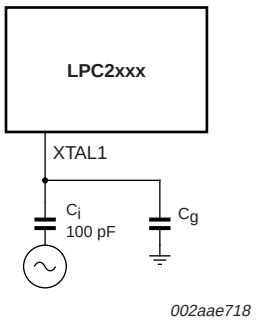
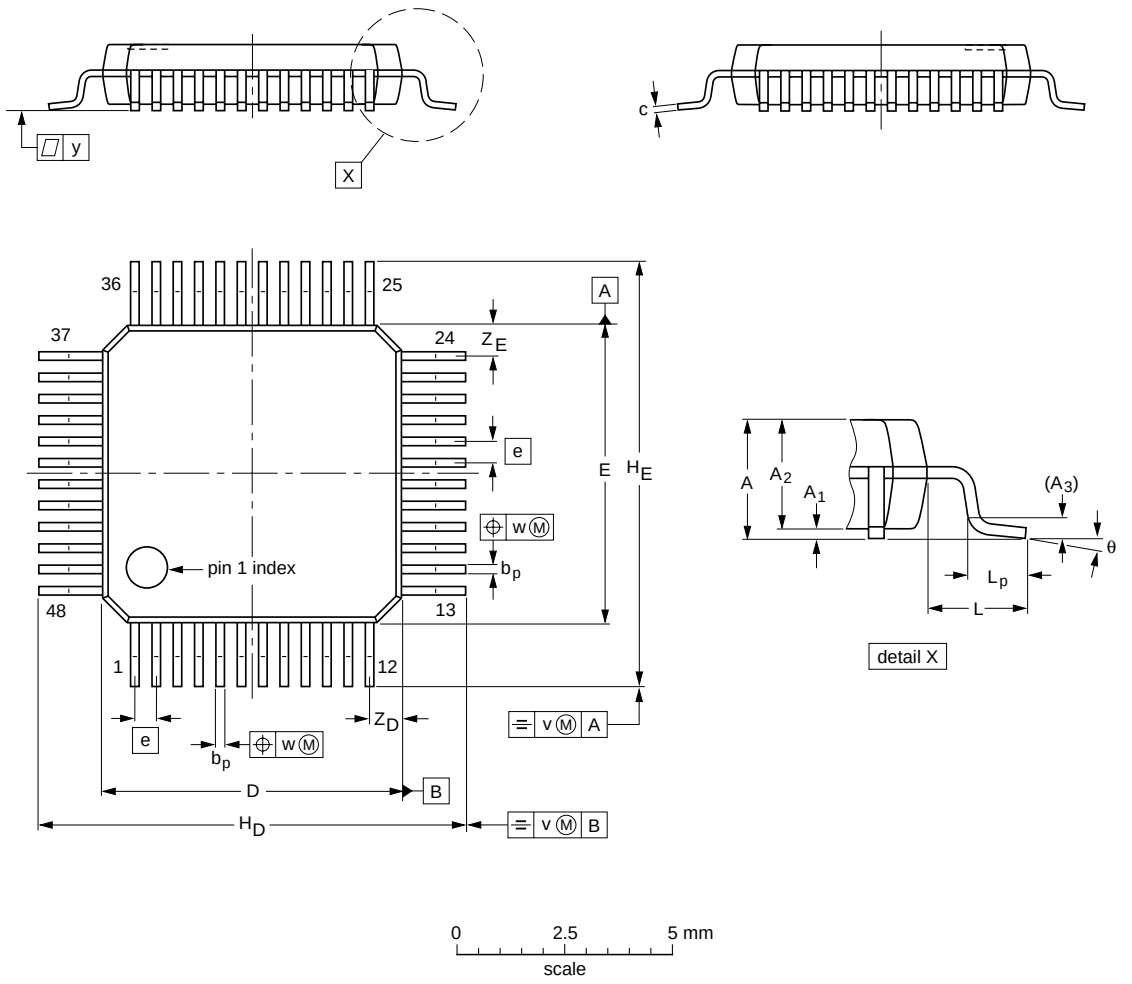


Fig 9. Slave mode operation of the on-chip oscillator

11. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 10. Package outline SOT313-2 (LQFP48)

12. Abbreviations

Table 8. Acronym list

Acronym	Description
ADC	Analog-to-Digital Converter
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
DCC	Debug Communications Channel
DSP	Digital Signal Processor
FIFO	First In, First Out
FIQ	Fast Interrupt reQuest
GPIO	General Purpose Input/Output
IAP	In-Application Programming
IRQ	Interrupt Request
ISP	In-System Programming
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSI	Synchronous Serial Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
VIC	Vectored Interrupt Controller

13. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2101_02_03_4	20090602	Product data sheet		LPC2101_02_03_3
Modifications:	• Section 6.17.4 “Code security (Code Read Protection - CRP)”: added description of three CRP levels (applicable to Revision A and higher). • Section 6.17.7 “Power control”: added description of Deep power-down mode (applicable to Revision A and higher). • Section 10.1 “XTAL1 input” added. • Section 10.2 “XTAL and RTC Printed Circuit Board (PCB) layout guidelines” added. • Figure 6, Figure 7, Figure 8: added power consumption data for Deep power-down mode (applicable to Revision A and higher). • Table 3: added table note 7. • Table 3: modified description of P0.14, RTCX1, RTCX2, XTAL1, XTAL2, JTAG, and DBGSEL pins. • Table 4: modified value for $V_{DD(3V3)}$. • Table 5: added and modified values for V_{hys}. • Table 5: Voltage range for pins $V_{DD(3V3)}$ and V_{DDA} extended to 2.6 V.			
LPC2101_02_03_3	20081007	Product data sheet	-	LPC2101_02_03_2
Modifications:	• Updated data sheet status to Product data sheet. • Table 1 and Table 2: added LPC2102FHN48 and LPC2103FHN48. • Table 1, Table 2, Table 3 and related figures: removed LPC2103FA44. • Table 3: updated pad descriptions. • Table 3: updated description of pin 47, SCL1. • Table 3: updated description of pins V_{DDA} and $V_{DD(1V8)}$. • Table 4: changed storage temperature range from –40 °C/125 °C to –65 °C/150 °C. • Table 5: added or modified values for $I_{DD(act)}$, $I_{DD(pd)}$, I_{BATpd}, I_{BATact}. • Table 5: removed “CCLK = 10 MHz” and associated values for $I_{DD(act)}$. • Section 5: added Figure 3. • Section 11: added Figure 11.			
LPC2101_02_03_2	20071218	Preliminary data sheet	-	LPC2101_02_03_1
LPC2101_02_03_1	20060118	Preliminary data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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