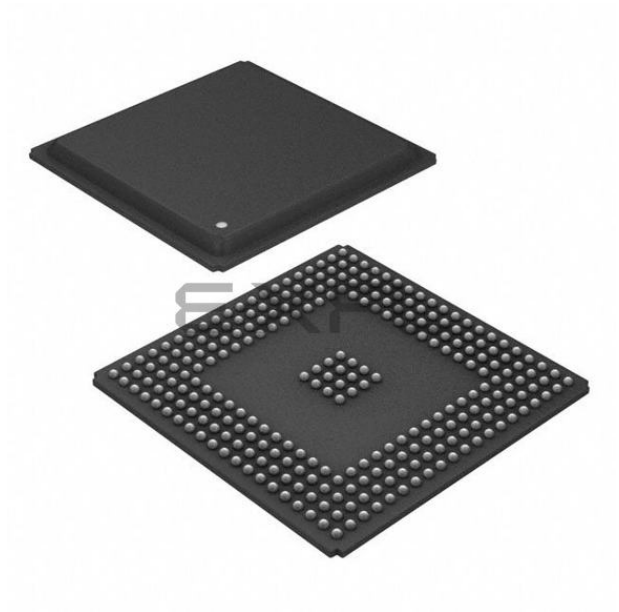

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Not For New Designs
Applications	Network Processor
Core Processor	ARM9®
Program Memory Type	External Program Memory
Controller Series	-
RAM Size	External
Interface	EBI/EMI, Ethernet, DMA, I²C, IEEE 1284, LCD, SPI, UART, USB
Number of I/O	73
Voltage - Supply	1.4V ~ 3.6V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	272-BBGA
Supplier Device Package	272-BGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/digi-international/ns9360b-0-c103

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USB ports

- USB v.2.0 full speed (12 Mbps) and low speed (1.5 Mbps)
- Independent OHCI Host and Device ports
- Internal USB PHY
- External USB PHY interface
- USB device supports one bidirectional control endpoint and 10 unidirectional endpoints
- All endpoints supported by a dedicated DMA channel
- 32 byte FIFO per endpoint

Serial ports

- 4 serial modules, each independently configurable to UART mode, SPI master mode, or SPI slave mode
- Bit rates from 75 bps to 921.6 kbps: asynchronous x16 mode
- Bit rates from 1.2 kbps to 11.25 Mbps: synchronous mode
- UART provides:
  - High-performance hardware and software flow control
  - Odd, even, or no parity
  - 5, 6, 7, or 8 bits
  - 1 or 2 stop bits
  - Receive-side character and buffer gap timers
- Internal or external clock support, digital PLL for RX clock extraction
- 4 receive-side data match detectors
- 2 dedicated DMA channels per module, 8 channels total
- 32 byte TX FIFO and 32 byte RX FIFO per module

I^2C port

- I^2C v.1.0, configurable to master or slave mode
- Bit rates: fast (400 kHz) or normal (100 kHz) with clock stretching
- 7-bit and 10-bit address modes
- Supports I^2C bus arbitration

1284 parallel peripheral port

- All standard modes: ECP, byte, nibble, compatibility (also known as SPP or “Centronix”)
- RLE (run length encoding) decoding of compressed data in ECP mode
- Operating clock from 100 kHz to 2 MHz

High performance multiple-master/distributed DMA system

- Intelligent bus bandwidth allocation (patent pending)
- System bus and peripheral bus

System bus:

- Every system bus peripheral is a bus master with a dedicated DMA engine

Peripheral bus:

- One 12-channel DMA engine supports USB device
  - 2 DMA channels support control endpoint
  - 10 DMA channels support 10 endpoints
- One 12-channel DMA engine supports:
  - 4 serial modules (8 DMA channels)
  - 1284 parallel port (4 DMA channels)
- All DMA channels support fly-by mode

External peripheral:

- One 2-channel DMA engine supports external peripheral connected to memory bus
- Each DMA channel supports memory-to-memory transfers

Reset

Master reset using an external reset pin resets the NS9360. Only the AHB bus error status registers retain their values; software read resets these error status registers. The input reset pin can be driven by a system reset circuit or a simple power-on reset circuit.

RESET_DONE as an input

Used at bootup only:

- When set to 0, the system boots from SDRAM through the serial SPI EEPROM.
- When set to 1, the system boots from Flash/ROM. This is the default.

SPI boot sequence

1. When the system reset turns to inactive, the reset signal to the CPU is still held active.
2. An I/O module on the peripheral bus (BBus) reads from a serial ROM device that contains the memory controller settings and the boot program.
3. The BBus-to-AHB bridge requests and gets the system bus.
4. The memory controller settings are read from the serial EEPROM and used to initialize the memory controller.
5. The BBus-to-AHB bridge loads the boot program into the SDRAM, starting at address 0.
6. The reset signal going to the CPU is released once the boot program is loaded. RESET_DONE is now set to 1.
7. The CPU begins to execute code from address 0x0000 0000.

RESET_DONE as an output

Sets to 1, per Step 6 in the boot sequence:

If the system is booting from serial EEPROM through the SPI port, the boot program must be loaded into the SDRAM before the CPU is released from reset. The memory controller is powered up with dy_cs_n[0] enabled with a default set of SDRAM configurations. The default address range for dy_cs_n[0] is from 0x0000 0000. The other chip selects are disabled.

You can use one of these software resets to reset NS9360. Select the reset by setting the appropriate bit in the appropriate register:

- Watchdog timer can issue reset upon Watchdog timer expiration.
- Software reset can reset individual internal modules or all modules except memory and CPU.
- The system is reset whenever software sets the PLL SW change bit, in the PLL Configuration register, to 1.

Hardware reset duration is 4ms for PLL to stabilize. Software reset duration depends on speed grade, as shown:

Speed grade	CPU clock cycles	Duration
177 MHz	128	723 ns
155 MHz	128	826 ns
103 MHz	128	1243 ns

Table 3: Software reset duration

The minimum reset pulse width is 10 crystal clocks.

System Clock

The system clock is provided to NS9360 by either a crystal or an external oscillator; this table shows sample clock frequency settings for each chip speed grade.

Speed	cpu_clk	ahb_clk (main bus)	bbus_clk
177 MHz	176.9472	88.4736	44.2368
155 MHz	154.8288	77.4144	38.7072
103 MHz	103.2192	51.6096	24.8048

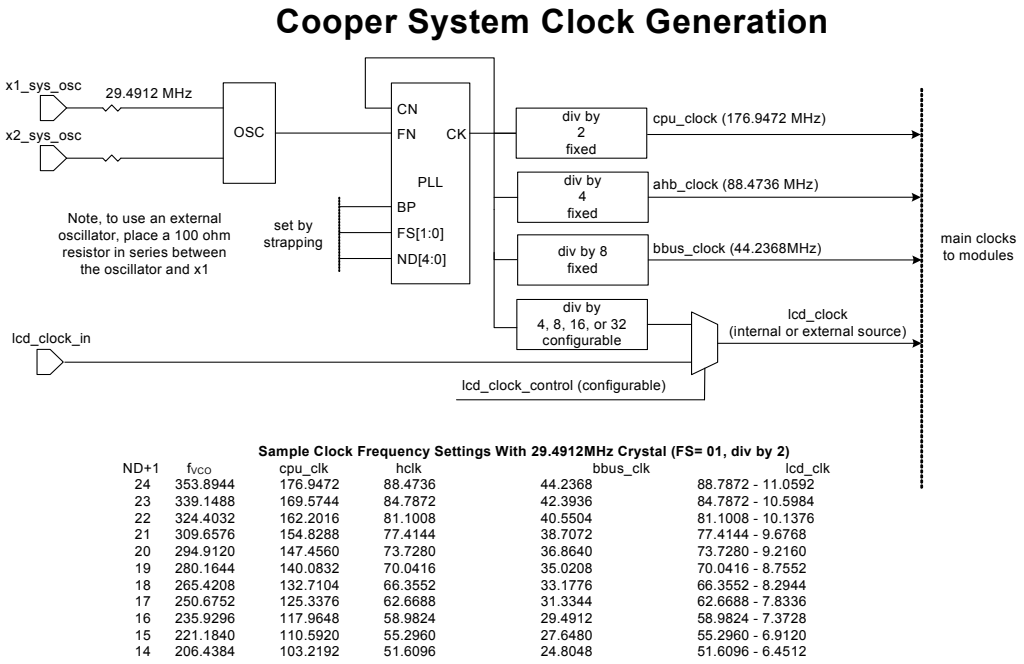
Table 4: Sample clock frequency settings with 29.4912 MHz crystal

Pulldowns are required as follows:

- To produce 176.9472 MHz, pull down gpio[12], gpio[10], gpio[4].
- To produce 154.8288 MHz, pull down gpio[12], gpio[10], gpio[8].
- To produce 103.2192 MHz, pull down gpio[17], gpio[10], gpio[8], gpio[4].

Using an oscillator

If an oscillator is used, it must be connected to the x1_sys_osc input (C8 pin) on the NS9360. If a crystal is used, it must be connected with a circuit such as the one shown in Figure 2, "NS9360 system clock".



Sample Clock Frequency Settings With 29.4912MHz Crystal (FS= 01, div by 2)

ND+1	f_{vco}	cpu_clk	hclk	bbus_clk	lcd_clk
24	353.8944	176.9472	88.4736	44.2368	88.7872 - 11.0592
23	339.1488	169.5744	84.7872	42.3936	84.7872 - 10.5984
22	324.4032	162.2016	81.1008	40.5504	81.1008 - 10.1376
21	309.6576	154.8288	77.4144	38.7072	77.4144 - 9.6768
20	294.9120	147.4560	73.7280	36.8640	73.7280 - 9.2160
19	280.1644	140.0832	70.0416	35.0208	70.0416 - 8.7552
18	265.4208	132.7104	66.3552	33.1776	66.3552 - 8.2944
17	250.6752	125.3376	62.6688	31.3344	62.6688 - 7.8336
16	235.9296	117.9648	58.9824	29.4912	58.9824 - 7.3728
15	221.1840	110.5920	55.2960	27.6480	55.2960 - 6.9120
14	206.4384	103.2192	51.6096	24.8048	51.6096 - 6.4512

Figure 3: NS9360 system clock generation (PLL)

You can use this formula to calculate the system clock frequencies if a different

system oscillator frequency is used:

You can use this formula to calculate the system clock frequencies if a different system oscillator frequency is used:

f_{vco} = (f_{osc} x (ND + 1) / FS)

f_{cpu_clk} = f_{vco} / 2

f_{hclk} = f_{vco} / 4

f_{bbuys_clk} = f_{vco} / 8

f_{lcd_clk} = programmable, f_{vco} / 4, 8, 16, or 32

USB clock

USB is clocked by a separate PLL driven by an external 48 MHz crystal, or it can be driven directly by an external 48 MHz oscillator.

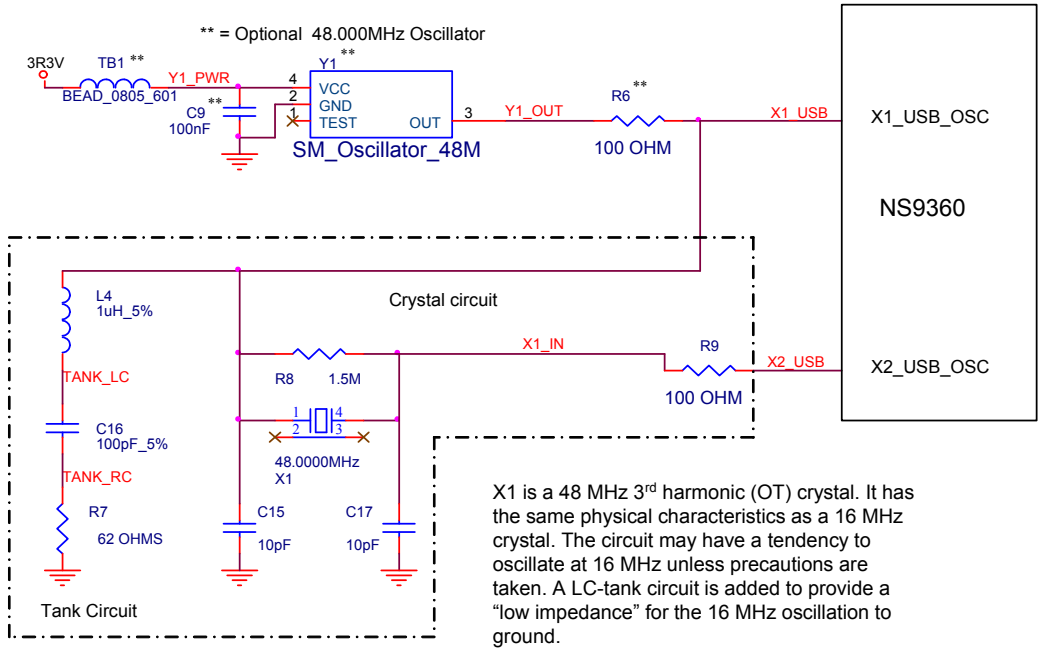


Figure 4: USB clock

Pin #	Signal Name / muxed behind	U/D	OD (mA)	I/O	Description
B14	data[4]		8	I/O	Data bus signal
A14	data[5]		8	I/O	Data bus signal
C13	data[6]		8	I/O	Data bus signal
B13	data[7]		8	I/O	Data bus signal
A13	data[8]		8	I/O	Data bus signal
C12	data[9]		8	I/O	Data bus signal
B12	data[10]		8	I/O	Data bus signal
B11	data[11]		8	I/O	Data bus signal
C11	data[12]		8	I/O	Data bus signal
A11	data[13]		8	I/O	Data bus signal
A10	data[14]		8	I/O	Data bus signal
C10	data[15]		8	I/O	Data bus signal
B10	data[16]		8	I/O	Data bus signal
A9	data[17]		8	I/O	Data bus signal
B9	data[18]		8	I/O	Data bus signal
C9	data[19]		8	I/O	Data bus signal
A8	data[20]		8	I/O	Data bus signal
B8	data[21]		8	I/O	Data bus signal
C8	data[22]		8	I/O	Data bus signal
B7	data[23]		8	I/O	Data bus signal
A6	data[24]		8	I/O	Data bus signal
C7	data[25]		8	I/O	Data bus signal
B6	data[26]		8	I/O	Data bus signal
A5	data[27]		8	I/O	Data bus signal
C6	data[28]		8	I/O	Data bus signal
B5	data[29]		8	I/O	Data bus signal
A4	data[30]		8	I/O	Data bus signal
C5	data[31]		8	I/O	Data bus signal
F2	data_mask[0]		8	O	SDRAM data mask signal
G3	data_mask[1]		8	O	SDRAM data mask signal
F1	data_mask[2]		8	O	SDRAM data mask signal
G2	data_mask[3]		8	O	SDRAM data mask signal

Table 5: System Memory interface pinout

Pin #	Signal name		U/D	OD (mA)	I/O	Description	
	MII / muxed behind	RMII				MII	RMII
P1	enet_phy_int_n / gpio[65]	enet_phy_ int_n	U		I	Ethernet PHY interrupt	Ethernet PHY interrupt
L2	mdc	mdc		4	O	MII management interface clock	MII management interface clock
K2	mdio / gpio[50]	mdio		2	I/O	MII management data	MII management data
V4	rx_clk	ref_clk			I	Receive clock	Reference clock
U3	rx_dv / gpio[51]	N/C			I	Receive data valid	Pull low external to NS9360
V1	rx_er / gpio[52]	rx_er			I	Receive error	Optional signal; pull low external to NS9360 if not used
N3	rxd[0] / gpio[53]	rxd[0]			I	Receive data bit 0	Receive data bit 0
N2	rxd[1] / gpio[54]	rxd[1]			I	Receive data bit 1	Receive data bit 1
N1	rxd[2] / gpio[55]	N/C			I	Receive data bit 2	Pull low external to NS9360
M3	rxd[3] / gpio[56]	N/C			I	Receive data bit 3	Pull low external to NS9360
V2	tx_clk	N/C			I	Transmit clock	Pull low external to NS9360
M2	tx_en / gpio[57]	tx_en		2	O	Transmit enable	Transmit enable
M1	tx_er / gpio[58]	N/C		2	O	Transmit error	N/A
L3	txd[0] / gpio[59]	txd[0]		2	O	Transmit data bit 0	Transmit data bit 0
L1	txd[1] / gpio[60]	txd[1]		2	O	Transmit data bit 1	Transmit data bit 1
K1	txd[2] / gpio[61]	N/C		2	O	Transmit data bit 2	N/A
K3	txd[3] / gpio[62]	N/C		2	O	Transmit data bit 3	N/A

Table 7: Ethernet interface pinout

Clock generation/system pins

Pin #	Signal name	U/D	OD (mA)	I/O	Description
R2	x1_sys_osc			I	System clock crystal oscillator circuit input
P3	x2_sys_osc			O	System clock crystal oscillator circuit output
T1	sys_osc_vdd				System oscillator 3.3V power
F18	x1_usb_osc			I	USB clock crystal oscillator circuit input. (Connect to GND if USB is not used.)

Table 8: Clock generation/system pins pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Description
E20	x2_usb_osc			O	USB clock crystal oscillator circuit output
E19	usb_osc_vdd				USB oscillator 3.3V power
W4	reset_done	U	2	I/O	CPU is enabled once the boot program is loaded. Reset_done is set to 1.
U5	reset_n	U		I	System reset input signal
W3	sreset_n	U		I	System reset. sreset_n is the same as reset but does *not* reset the system PLL.
V5	bist_en_n			I	Enable internal BIST operation
U6	pll_test_n			I	Enable PLL testing
Y3	scan_en_n			I	Enable internal scan testing
R3	sys_pll_dvdd				System clock PLL 1.5V digital power
T2	sys_pll_dvss				System clock PLL digital ground
U2	sys_pll_avdd				System clock PLL 3.3V analog power
U1	sys_pll_avss				System clock PLL analog ground
T3	pll_lpf			O	PLL diagnostic output
V10	lcdclk / gpio[15]	U		I	External LCD clock input (muxed behind gpio[15])

Table 8: Clock generation/system pins pinout

bist_en_n, pll_test_n, and scan_en_n

Table 9 is a truth/termination table for bist_en_n, pll_test_n, and scan_en_n.

	Normal operation	Arm debug	
pll_test_n	pull up	pull up	10K recommended
bist_en_n	pull down	pull up	10K pullup = debug 2.4K pulldown = normal
scan_en_n	pull down	pull down	2.4K recommended

Table 9: bist_en_n, pll_test_n, & scan_en_n truth/termination table

GPIO MUX

- The BBus utility contains the control pins for each GPIO MUX bit. Each pin can be selected individually; that is, you can select any option (00, 01, 02, 03) for any pin, by setting the appropriate bit in the appropriate register.
- Some signals are muxed to two different GPIO pins, to maximize the number of possible applications. These duplicate signals are marked as such in the Descriptions column in the table. Selecting the primary GPIO pin and the duplicate GPIO pin for the same function is not

- If not pulled low; populate R1

R1 and U1 can be eliminated by selecting the ENABLE_n polarity of the USB power IC to match the bootstrap state.

2 Code initializes USB registers. USP_PWR driven by USB IP.

3 Code sets gpio[16] and gpio[17] to mode 0 — USB.
- Sets the INV function for USB_OVR;
- If R2 and U1 are populated, set the INV function for USB_PWR

LCD module signals

The LCD module signals are multiplexed with GPIO pins. They include six control signals and up to 18 data signals. Table 11 describes the control signals.

Signal name	Type	Description
CLPOWER	Output	LCD panel power enable
CLLP	Output	Line synchronization pulse (STN) / horizontal synchronization pulse (TFT)
CLCP	Output	LCD panel clock
CLFP	Output	Frame pulse (STN) / vertical synchronization pulse (TFT)
CLAC	Output	STN AC bias drive or TFT data enable output
CLD[17:0]	Output	LCD panel data
CLLE	Output	Line end signal

Table 11: LCD module signal descriptions

The CLD[17:0] signal has seven modes of operation:

- TFT 18-bit interface
- Color STN single panel
- Color STN dual panel
- 4-bit mono STN single panel
- 4-bit mono STN dual panel
- 8-bit mono STN single panel
- 8-bit mono STN dual panel

Table 12 shows which CLD[17:0] pins provide the pixel data to the STN panel for each mode of operation.

Legend:
- Ext pin = External pin
- CUSTN = Color upper panel STN, dual and/or single panel
- CLSTN = Color lower panel STN, dual
- MUSTN = Mono upper panel STN, dual and/or single panel
- MLSTN = Mono lower panel STN, dual
- N/A = not used

– 01 and 02 = The option number/position in the Description field of the GPIO mux pinout. See "GPIO MUX" on page 21 for more information.

Ext pin	GPIO pin & description	Color STN single panel	Color STN dual panel	4-bit mono STN single panel	4-bit mono STN dual panel	8-bit mono STN single panel	8-bit mono STN dual panel
CLD[17]	W18=LCD data bit 17 (02)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[16]	V17=LCD data bit16 (02)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[15]	U16=LCD data bit 15 (02)	N/A	CLSTN[0][1]	N/A	N/A	N/A	MLSTN[0][1]
CLD[14]	Y18=LCD data bit 14 (02)	N/A	CLSTN[1]	N/A	N/A	N/A	MLSTN[1]
CLD[13]	W17=LCD data bit 13 (02)	N/A	CLSTN[2]	N/A	N/A	N/A	MLSTN[2]
CLD[12]	V16=LCD data bit 12 (02)	N/A	CLSTN[3]	N/A	N/A	N/A	MLSTN[3]
CLD[11]	U15=LCD data bit 11 (02) Y16=LCD data bit 11 (02)	N/A	CLSTN[4]	N/A	MLSTN[0][1]	N/A	MLSTN[4]
CLD[10]	Y17=LCD data bit 10 (02) W15=LCD data bit 10 (02)	N/A	CLSTN[5]	N/A	MLSTN[1]	N/A	MLSTN[5]
CLD[9]	W16=LCD data bit 9 (02) V14=LCD data bit 9 (02)	N/A	CLSTN[6]	N/A	MLSTN[2]	N/A	MLSTN[6]
CLD[8]	V15=LCD data bit 8 (02) Y15=LCD data bit 8 (02)	N/A	CLSTN[7]	N/A	MLSTN[3]	N/A	MLSTN[7]
CLD[7]	Y16=LCD data bit 7 (01)	CUSTN[0][1]	CUSTN[0][1]	N/A	N/A	MUSTN[0]	MUSTN[0][1]
CLD[6]	W15=LCD data bit 6 (01)	CUSTN[1]	CUSTN[1]	N/A	N/A	MUSTN[1]	MUSTN[1]
CLD[5]	V14=LCD data bit 5 (01)	CUSTN[2]	CUSTN[2]	N/A	N/A	MUSTN[2]	MUSTN[2]
CLD[4]	Y15=LCD data bit 4 (01)	CUSTN[3]	CUSTN[3]	N/A	N/A	MUSTN[3]	MUSTN[3]
CLD[3]	W14=LCD data bit 3 (01)	CUSTN[4]	CUSTN[4]	MUSTN[0]	MUSTN[0][1]	MUSTN[4]	MUSTN[4]
CLD[2]	Y14=LCD data bit 2 (01)	CUSTN[5]	CUSTN[5]	MUSTN[1]	MUSTN[1]	MUSTN[5]	MUSTN[5]
CLD[1]	V13=LCD data bit 1 (01)	CUSTN[6]	CUSTN[6]	MUSTN[2]	MUSTN[2]	MUSTN[6]	MUSTN[6]
CLD[0]	W13=LCD data bit 0 (01)	CUSTN[7]	CUSTN[7]	MUSTN[3]	MUSTN[3]	MUSTN[7]	MUSTN[7]

1 This data bit corresponds to the first “pixel position.” For example, for an 8-bit mono STN display, CUSTN[0] is the leftmost pixel on the panel and CUSTN[7] is the rightmost pixel within the 8-bit data. For a color STN display, bits [7, 6, 5] form the leftmost pixel.

Table 12: CLD[17:0] pin descriptions for STN display

Table 13 shows which CLD[17:0] pins provide the pixel data to the TFT panel for each of the multiplexing modes of operation.

External pin	TFT 15 bit
CLD[17]	BLUE[4]
CLD[16]	BLUE[3]
CLD[15]	BLUE[2]
CLD[14]	BLUE[1]
CLD[13]	BLUE[0]
CLD[12]	Intensity bit
CLD[11]	GREEN[4]
CLD[10]	GREEN[3]
CLD[9]	GREEN[2]
CLD[8]	GREEN[1]
CLD[7]	GREEN[0]
CLD[6]	Intensity bit
CLD[5]	RED[4]
CLD[4]	RED[3]
CLD[3]	RED[2]
CLD[2]	RED[1]
CLD[1]	RED[0]
CLD[0]	Intensity bit

Table 13: CLD[17:0] pin descriptions for TFT display

This LCD TFT panel signal multiplexing table shows the RGB alignment to a 15-bit TFT with the intensity bit not used. The intensity bit, if used, should be connected to the LSB (that is, RED[0], GREEN[0], BLUE[0]) input of an 18-bit LCD TFT panel as shown in the next table.

	4	3	2	1	0	Intensity
18-bit TFT	5	4	3	2	1	0
15-bit TFT	4	3	2	1	0	x
12-bit TFT	3	2	1	0	x	x
9-bit TFT	2	1	0	x	x	x

Table 14: RGB bit alignment according to TFT interface size (one color shown)

If you want reduced resolution, the least significant color bits can be dropped, starting with Red[0], Green[0], and Blue[0].

Address and register maps

System address map

The system memory address is divided to allow access to the internal and external resources on the system bus, as shown in Table 20.

Address range	Size	System functions
0x0000 0000 – 0x0FFF FFFF	256 MB	System memory chip select 0 - Dynamic memory (default)
0x1000 0000 – 0x1FFF FFFF	256 MB	System memory chip select 1 - Dynamic memory (default)
0x2000 0000 – 0x2FFF FFFF	256 MB	System memory chip select 2 - Dynamic memory (default)
0x3000 0000 – 0x3FFF FFFF	256 MB	System memory chip select 3 - Dynamic memory (default)
0x4000 0000 – 0x4FFF FFFF	256 MB	System memory chip select 0 - Static memory (default)
0x5000 0000 – 0x5FFF FFFF	256 MB	System memory chip select 1 - Static memory (default)
0x6000 0000 – 0x6FFF FFFF	256MB	System memory chip select 2 - Static memory (default)
0x7000 0000 – 0x7FFF FFFF	256 MB	System memory chip select 3 - Static memory (default)
0x8000 0000 – 0x8FFF FFFF	256 MB	Reserved
0x9000 0000 – 0x9FFF FFFF	256 MB	BBus peripherals
0xA000 0000 – 0xA03F FFFF	4 MB	Reserved
0xA040 0000 – 0xA04F FFFF	1 MB	BBus-to-AHB bridge
0xA050 0000 – 0xA05F FFFF	1 MB	Reserved
0xA060 0000 – 0xA06F FFFF	1 MB	Ethernet Communication module
0xA070 0000 – 0xA07F FFFF	1 MB	Memory controller
0xA080 0000 – 0xA08F FFFF	1 MB	LCD controller
0xA090 0000 – 0xA09F FFFF	1 MB	System Control module
0xA0A0 0000 – 0xFFFF FFFF	1526 MB	Reserved

Table 20: System address memory map

Electrical characteristics

The NS9360 operates at a 1.5V core, with 3.3V I/O ring voltages.

Absolute maximum ratings

Important: Permanent device damage can occur if the absolute maximum ratings are exceeded even for an instant.

Parameter	Symbol†	Rating	Unit
DC supply voltage	V_{DDA}	-0.3 to +3.9	V
DC input voltage	V_{INA}	-0.3 to V_{DDA}+0.3	V
DC output voltage	V_{OUTA}	-0.3 to V_{DDA}+0.3	V
DC input current	I_{IN}	±10	mA
Storage temperature	T_{STG}	-40 to +125	^{o}C
† V_{DDA}, V_{INA}, V_{OUTA}: Ratings of I/O cells for 3.3V interface			

Recommended operating conditions

Recommended operating conditions specify voltage and temperature ranges over which a circuit's correct logic function is guaranteed. The specified DC electrical characteristics (see "DC electrical characteristics" on page 41) are satisfied over these ranges.

Parameter	Symbol†	Rating	Unit
DC supply voltage	V_{DDA}	3.0 to 3.6	V
	V_{DDC} (core) V_{DDC} (PLL)	1.4 to 1.6 1.425 to 1.575	V
Maximum junction temperature	T_J	125	^{o}C

† V_{DDA}: Ratings of I/O cells for 3.3V interface
V_{DDC}: Ratings of internal cells

Power dissipation

This table shows the *maximum power dissipation* for I/O and core:

CPU clock		Full	No LCD	No LCD, no serial
Total @ 177 MHz		639 mW	599 mW	599 mW
	Core	276 mW	269 mW	269 mW
	I/O	363 mW	330 mW	330 mW
Total @ 155 MHz		593 mW	564 mW	564 mW
	Core	243 mW	237 mW	237 mW
	I/O	350 mW	327 mW	327 mW
Total @ 103 MHz		475 mW	450 mW	450 mW
	Core	164 mW	159 mW	159 mW
	I/O	311 mW	291 mW	291 mW

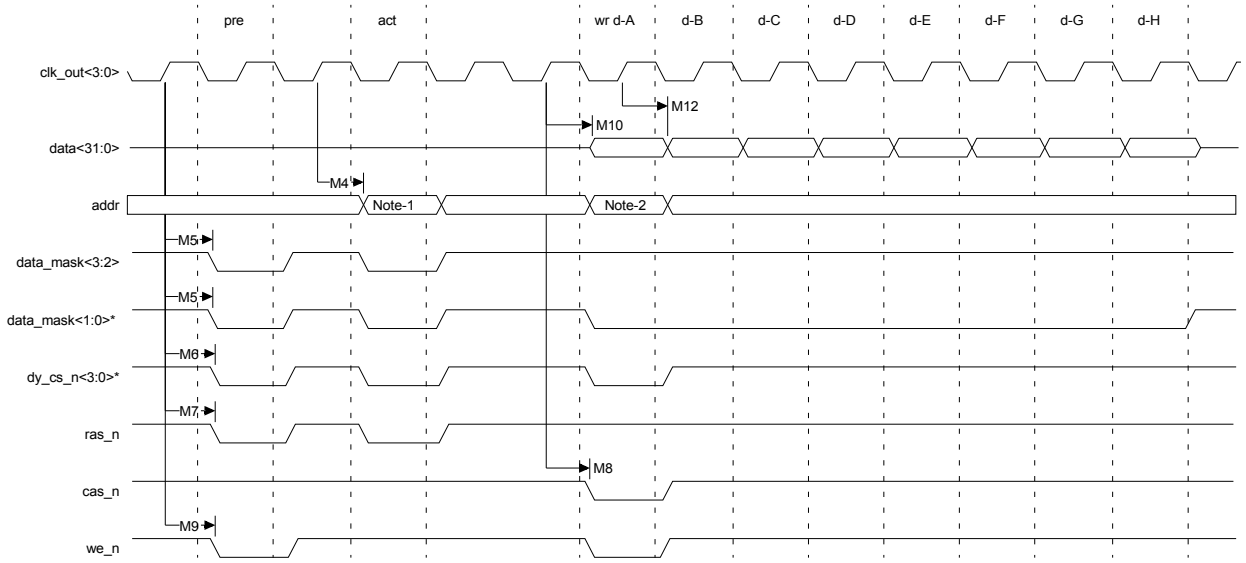
Table 22: NS9360 power dissipation

This table shows the *refresh only* power dissipation for I/O and core.

CPU clock		Refresh only
Total @ 177 MHz		255.5 mW
	Core	61.5 mW
	I/O	194 mW
Total @ 155 MHz		237.5 mW
	Core	54 mW
	I/O	183.5 mW
Total @ 103 MHz		197.4 mW
	Core	39 mW
	I/O	158.4 mW

Table 23: Refresh only mode

SDRAM burst write (16-bit)

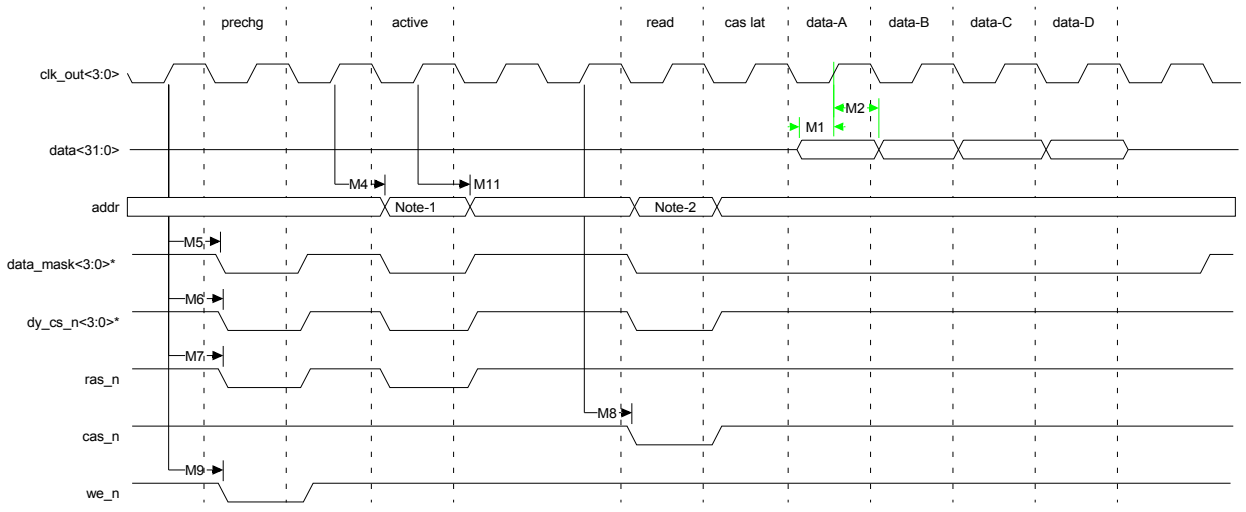


Notes:

1 This is the bank and RAS address.

2 This is the CAS address.

SDRAM burst read (32-bit)

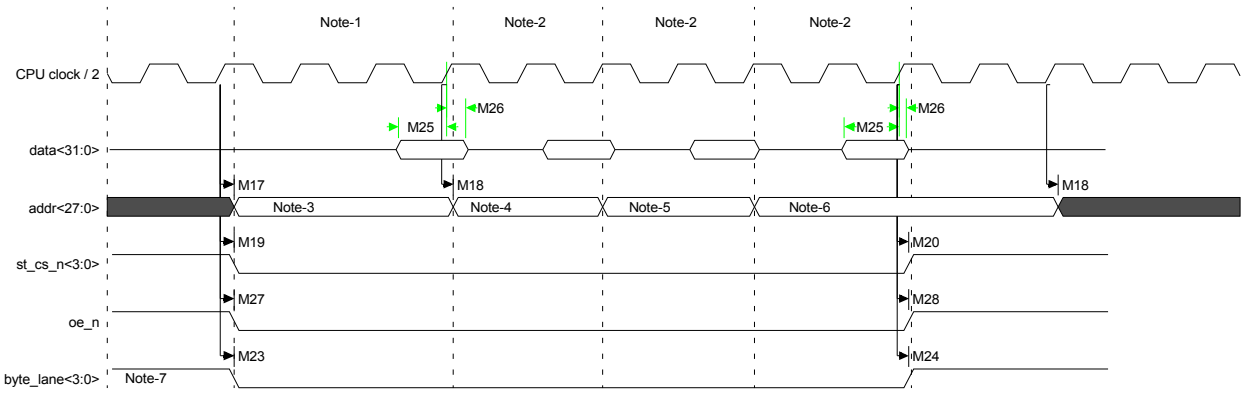


Notes:

1 This is the bank and RAS address.

2 This is the CAS address.

Static RAM asynchronous page mode read, WTPG = 1



- WTPG = 1
  WTRD = 2
- If the PB field is set to 1, all four byte_lane signals will go low for 32-bit, 16-bit, and 8-bit read cycles.
- The asynchronous page mode will read 16 bytes in a page cycle. A 32-bit bus will do four 32-bit reads, as shown (3-2-2-2). A 16-bit bus will do eight 16-bit reads (3-2-2-2-3-2-2-2) per page cycle, and an 8-bit bus will do sixteen reads (3-2-2-2-3-2-2-2-3-2-2-2-3-2-2-2) per page cycle. 3-2-2-2 is the example used here, but the WTRD and WTPG field can set them differently.

Notes:

1 The length of the first cycle in the page is determined by the WTRD field.

2 The length of the 2nd, 3rd, and 4th cycles is determined by the WTPG field.

3 This is the starting address. The least significant two bits will always be ‘00.’

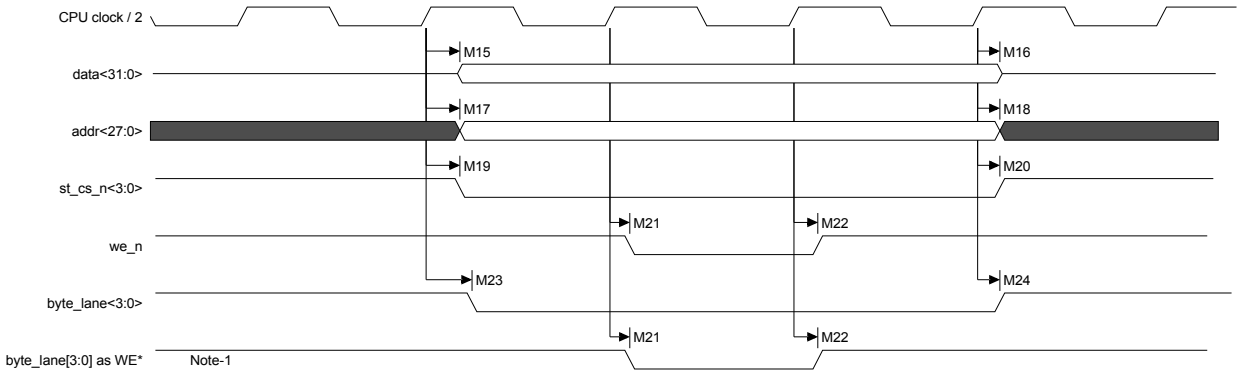
4 The least significant two bits in the second cycle will always be ‘01.’

5 The least significant bits in the third cycle will always be ‘10.’

6 The least significant two bits in the fourth cycle will always be ‘11.’

7 If the PB field is set to 0, the byte_lane signal will always be high during a read cycle.

Static RAM write cycle

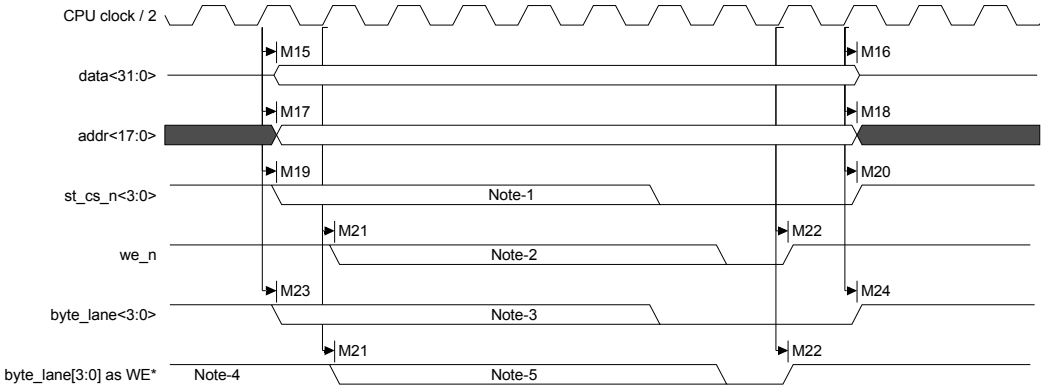


- WTWR = 0
  WWEN = 0
- During a 32-bit transfer, all four byte_lane signals will go low.
- During a 16-bit transfer, two byte_lane signals will go low.
- During an 8-bit transfer, only one byte_lane signal will go low.

Note:

1 If the PB field is set to 0, the byte_lane signals will function as write enable signals and the we_n signal will always be high.

Static write cycle with configurable wait states



- WTWR = from 0 to 15
  WWEN = from 0 to 15
- The WTWR field determines the length on the write cycle.
- During a 32-bit transfer, all four byte_lane signals will go low.
- During a 16-bit transfer, two byte_lane signals will go low.
- During an 8-bit transfer, only one byte_lane signal will go low.

Notes:

1 Timing of the st_cs_n signal is determined with a combination of the WTWR and WWEN fields. The st_cs_n signal will always go low at least one clock before we_n goes low, and will go high one clock after we_n goes high.

2 Timing of the we_n signal is determined with a combination of the WTWR and WWEN fields.

3 Timing of the byte_lane signals is determined with a combination of the WTWR and WWEN fields. The byte_lane signals will always go low one clock before we_n goes low, and will go one clock high after we_n goes high.

4 If the PB field is set to 0, the byte_lane signals will function as the write enable signals and the we_n signal will always be high.

5 If the PB field is set to 0, the timing for the byte_lane signals is set with the WTWR and WWEN fields.

USB internal PHY timing

Table 32 and Table 33 describe the values shown in the USB internal PHY timing diagrams.

Parameter	Description	Min	Max	Unit	Notes
U1	Rise time (10%–90%)	4	20	ns	1
U2	Fall time (10%–90%)	4	20	ns	1
U3	Differential rise and fall time matching	90	111.11	%	1, 2, 5
U4	Driver output resistance	28	44	ohms	3

Table 32: USB internal PHY full speed timing parameters

Parameter	Description	Min	Max	Unit	Notes
U1	Rise time (10%–90%)	75	300	ns	4
U2	Fall time (10%–90%)	75%	300	ns	4
U3	Differential rise and fall time matching	80	125	%	2, 4, 5

Table 33: USB internal PHY low speed timing parameters

Notes:

1 Load shown in "USB internal PHY full speed load."

2 U1/U2.

3 Includes resistance of 27 ohm ±2 ohm external series resistor.

4 Load shown in "USB internal PHY low speed load."

5 Excluding the first transition from the idle state.

USB internal PHY differential data timing