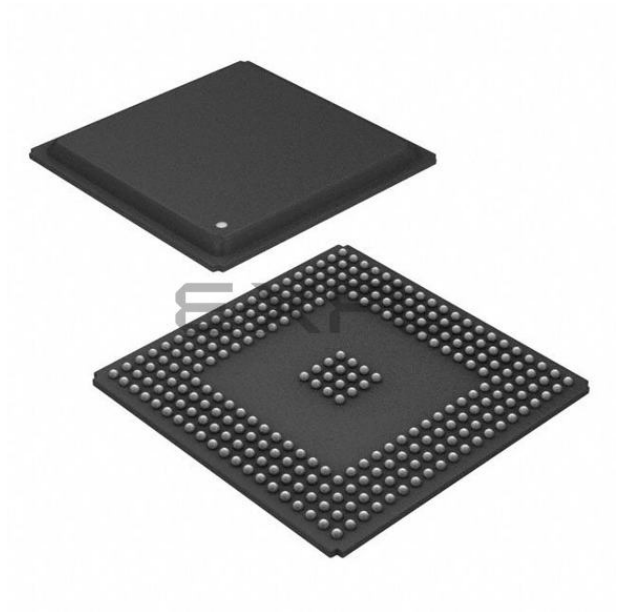


Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Not For New Designs
Applications	Network Processor
Core Processor	ARM9®
Program Memory Type	External Program Memory
Controller Series	-
RAM Size	External
Interface	EBI/EMI, Ethernet, DMA, I²C, IEEE 1284, LCD, SPI, UART, USB
Number of I/O	73
Voltage - Supply	1.4V ~ 3.6V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	272-BBGA
Supplier Device Package	272-BGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/digi-international/ns9360b-0-c177

NS9360 Features

32-bit ARM926EJ-S RISC processor

- 103 to 177 MHz
- 5-stage pipeline with interlocking
- Harvard architecture
- 8 kB instruction cache and 4 kB data cache
- 32-bit ARM and 16-bit Thumb instruction sets. Can be mixed for performance/code density tradeoffs
- MMU to support virtual memory-based OSs such as Linux, WinCE/Pocket PC, VxWorks, others
- DSP instruction extensions, improved divide, single cycle MAC
- ARM Jazelle, 1200CM (coffee marks) Java accelerator
- EmbeddedICE-RT debug unit
- JTAG boundary scan, BSDL support

External system bus interface

- 32-bit data, 32-bit internal address bus, 28-bit external address bus
- Glueless interface to SDRAM, SRAM, EEPROM, buffered DIMM, Flash
- 4 static and 4 dynamic memory chip selects
- 1-32 wait states per chip select

  A shared Static Extended Wait register allows transfers to have up to 16368 wait states that can be externally terminated.
- Self-refresh during system sleep mode
- Automatic dynamic bus sizing to 8 bits, 16 bits, 32 bits
- Burst mode support with automatic data width adjustment
- Two external DMA channels for external peripheral support

System Boot

- High-speed boot from 8-bit, 16-bit, or 32-bit ROM or Flash
- Hardware-supported low cost boot from serial EEPROM through SPI port (patent pending)

High performance 10/100 Ethernet MAC

- 10/100 Mbps MII/RMII PHY interfaces
- Full-duplex or half-duplex
- Station, broadcast, or multicast address filtering
- 2 kB RX FIFO
- 256 byte TX FIFO with on-chip buffer descriptor ring
  - Eliminates underruns and decreases bus traffic
- Separate TX and RX DMA channels
- Intelligent receive-side buffer size selection
- Full statistics gathering support
- External CAM filtering support

Flexible LCD controller

- Supports most commercially available displays:
  - 18-bit active Matrix color TFT displays
  - Single and dual panel color STN displays
  - Single and dual-panel monochrome STN displays
- Formats image data and generates timing control signals
- Internal programmable palette LUT and grayscaler support different color techniques
- Programmable panel-clock frequency

Power management (patent pending)

- Power save during normal operation
  - Disables unused modules
- Power save during sleep mode
  - Sets memory controller to refresh
  - Disables all modules except selected wakeup modules
  - Wakeup on valid packets or characters

Vector interrupt controller

- Decreased bus traffic and rapid interrupt service
- Hardware interrupt prioritization

General purpose timers/counters

- 8 independent 16-bit or 32-bit programmable timers or counters
  - Each with an I/O pin
- Mode selectable into:
  - Internal timer mode
  - External gated timer mode
  - External event counter
- Can be concatenated
- Resolution to measure minute-range events
- Source clock selectable: internal clock or external pulse event
- Each can be individually enabled/disabled

System timers

- Watchdog timer
- System bus monitor timer
- System bus arbiter timer
- Peripheral bus monitor timer

General purpose I/O

- 73 programmable GPIO pins (muxed with other functions)
- Software-readable powerup status registers for every pin for customer-defined bootstrapping

External interrupts

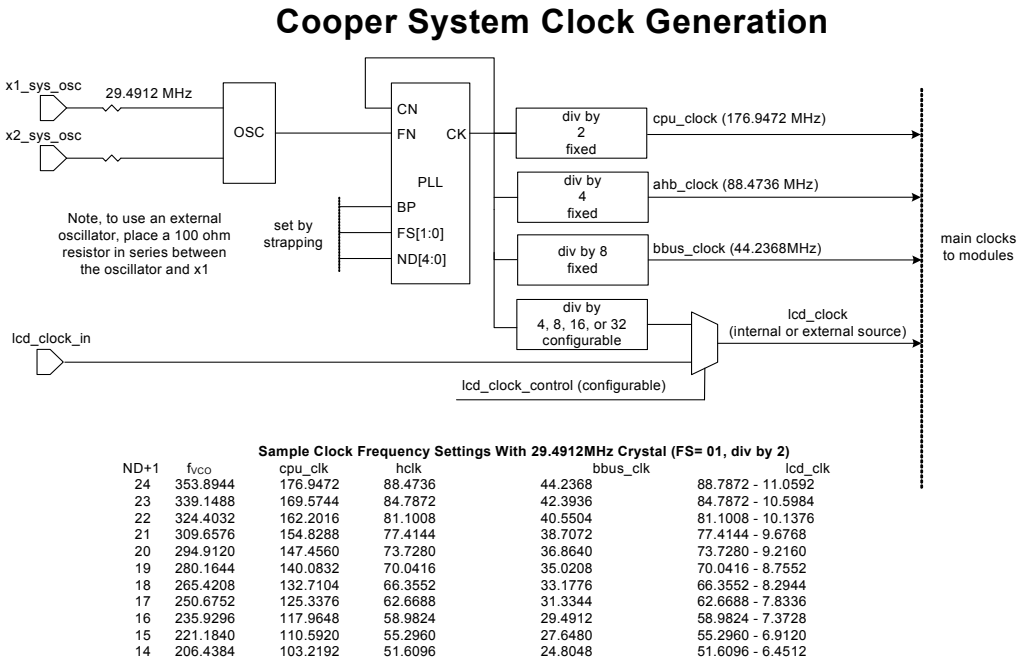
- 4 external programmable interrupts
  - Rising or falling edge-sensitive
  - Low level- or high level-sensitive

Clock generator

- Low cost external crystal
- On-chip phase locked loop (PLL)
- Software programmable PLL parameters
- Optional external oscillator
- Separate PLL for USB

Operating grades/Ambient temperatures

- 177 MHz: 0 – 70° C
- 155 MHz: -40 – +85° C
- 103 MHz: 0 – 70° C



Sample Clock Frequency Settings With 29.4912MHz Crystal (FS= 01, div by 2)

ND+1	f_{vco}	cpu_clk	hclk	bbus_clk	lcd_clk
24	353.8944	176.9472	88.4736	44.2368	88.7872 - 11.0592
23	339.1488	169.5744	84.7872	42.3936	84.7872 - 10.5984
22	324.4032	162.2016	81.1008	40.5504	81.1008 - 10.1376
21	309.6576	154.8288	77.4144	38.7072	77.4144 - 9.6768
20	294.9120	147.4560	73.7280	36.8640	73.7280 - 9.2160
19	280.1644	140.0832	70.0416	35.0208	70.0416 - 8.7552
18	265.4208	132.7104	66.3552	33.1776	66.3552 - 8.2944
17	250.6752	125.3376	62.6688	31.3344	62.6688 - 7.8336
16	235.9296	117.9648	58.9824	29.4912	58.9824 - 7.3728
15	221.1840	110.5920	55.2960	27.6480	55.2960 - 6.9120
14	206.4384	103.2192	51.6096	24.8048	51.6096 - 6.4512

Figure 3: NS9360 system clock generation (PLL)

You can use this formula to calculate the system clock frequencies if a different

system oscillator frequency is used:

You can use this formula to calculate the system clock frequencies if a different system oscillator frequency is used:

f_{vco} = (f_{osc} x (ND + 1) / FS)

f_{cpu_clk} = f_{vco} / 2

f_{hclk} = f_{vco} / 4

f_{bbuys_clk} = f_{vco} / 8

f_{lcd_clk} = programmable, f_{vco} / 4, 8, 16, or 32

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)	
V13	gpio[25]	U	4	I/O	00	Ser port D DSR
					01	LCD data bit 1
					02	Reserved
					03	GPIO 25
Y14	gpio[26]	U	4	I/O	00	Ser port D RI / SPI port D clk
					01	LCD data bit 2
					02	Timer 3
					03	GPI0 26
W14	gpio[27]	U	4	I/O	00	Ser port D DCD / SPI port D enable
					01	LCD data bit 3
					02	Timer 4
					03	GPIO 27
Y15	gpio[28]	U	4	I/O	00	Ext IRQ 1 (duplicate)
					01	LCD data bit 4
					02	LCD data bit 8 (duplicate)
					03	GPIO 28
V14	gpio[29]	U	4	I/O	00	Timer 5
					01	LCD data bit 5
					02	LCD data bit 9 (duplicate)
					03	GPIO 29
W15	gpio[30]	U	4	I/O	00	Timer 6
					01	LCD data bit 6
					02	LCD data bit 10 (duplicate)
					03	GPIO 30
Y16	gpio[31]	U	4	I/O	00	Timer 7
					01	LCD data bit 7
					02	LCD data bit 11 (duplicate)
					03	GPIO 31
V15	gpio[32]	U	4	I/O	00	Ext IRQ 2
					01	1284 Data 1 (bidirectional)
					02	LCD data bit 8
					03	GPIO 32
W16	gpio[33]	U	4	I/O	00	Reserved
					01	1284 Data 2 (bidirectional)
					02	LCD data bit 9
					03	GPIO 33
Y17	gpio[34]	U	4	I/O	00	iic_scl
					01	1284 Data 3 (bidirectional)
					02	LCD data bit 10
					03	GPIO 34

Table 10: GPIO MUX pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)	
U19	gpio[44][1]	U	2	I/O	00	Ser port D TXData / SPI port D dout
					01	1284 Select (peripheral-driven)
					02	USB phy tx output enable
					03	GPIO 44
U20	gpio[45]	U	2	I/O	0	Ser port D RXData / SPI port D din
					01	1284 nStrobe (host-driven)
					02	USB phy rx data
					03	GPIO 45
T19	gpio[46]	U	2	I/O	00	Ser port D RTS
					01	1284 nAutoFd (host-driven)
					02	USB phy rx data + (unidirectional phy only; for bidirectional USB PHY applications, do not configure for option 02)
					03	GPIO 46
R18	gpio[47]	U	2	I/O	00	Ser port D CTS
					01	1284 nInit (host-driven)
					02	USB phy rx data - (unidirectional phy only; for bidirectional USB PHY applications, do not configure for option 02)
					03	GPIO 47
T20	gpio[48]	U	2	I/O	00	USB phy suspend
					01	1284 nSelectIn (host-driven)
					02	DMA ch 2 req
					03	GPIO 48
R19	gpio[49][1]	U	2	I/O	00	USB phy speed
					01	1284 peripheral logic high (peripheral-driven)
					02	DMA ch 2 done
					03	GPIO 49
K2	gpio[50]		2	I/O	00	MII/RMII management data
					01	USB phy data + (duplicate) (TX and RX data for bidirectional PHY or TX data only for unidirectional PHY)
					02	Reserved
					03	GPIO 50
U3	gpio[51]		2	I/O	00	MII rx data valid
					01	USB phy data - (duplicate) (TX and RX data for bidirectional PHY or TX data only for unidirectional PHY)
					02	Reserved
					03	GPIO 51

Table 10: GPIO MUX pinout

– 01 and 02 = The option number/position in the Description field of the GPIO mux pinout. See "GPIO MUX" on page 21 for more information.

Ext pin	GPIO pin & description	Color STN single panel	Color STN dual panel	4-bit mono STN single panel	4-bit mono STN dual panel	8-bit mono STN single panel	8-bit mono STN dual panel
CLD[17]	W18=LCD data bit 17 (02)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[16]	V17=LCD data bit16 (02)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[15]	U16=LCD data bit 15 (02)	N/A	CLSTN[0][1]	N/A	N/A	N/A	MLSTN[0][1]
CLD[14]	Y18=LCD data bit 14 (02)	N/A	CLSTN[1]	N/A	N/A	N/A	MLSTN[1]
CLD[13]	W17=LCD data bit 13 (02)	N/A	CLSTN[2]	N/A	N/A	N/A	MLSTN[2]
CLD[12]	V16=LCD data bit 12 (02)	N/A	CLSTN[3]	N/A	N/A	N/A	MLSTN[3]
CLD[11]	U15=LCD data bit 11 (02) Y16=LCD data bit 11 (02)	N/A	CLSTN[4]	N/A	MLSTN[0][1]	N/A	MLSTN[4]
CLD[10]	Y17=LCD data bit 10 (02) W15=LCD data bit 10 (02)	N/A	CLSTN[5]	N/A	MLSTN[1]	N/A	MLSTN[5]
CLD[9]	W16=LCD data bit 9 (02) V14=LCD data bit 9 (02)	N/A	CLSTN[6]	N/A	MLSTN[2]	N/A	MLSTN[6]
CLD[8]	V15=LCD data bit 8 (02) Y15=LCD data bit 8 (02)	N/A	CLSTN[7]	N/A	MLSTN[3]	N/A	MLSTN[7]
CLD[7]	Y16=LCD data bit 7 (01)	CUSTN[0][1]	CUSTN[0][1]	N/A	N/A	MUSTN[0]	MUSTN[0][1]
CLD[6]	W15=LCD data bit 6 (01)	CUSTN[1]	CUSTN[1]	N/A	N/A	MUSTN[1]	MUSTN[1]
CLD[5]	V14=LCD data bit 5 (01)	CUSTN[2]	CUSTN[2]	N/A	N/A	MUSTN[2]	MUSTN[2]
CLD[4]	Y15=LCD data bit 4 (01)	CUSTN[3]	CUSTN[3]	N/A	N/A	MUSTN[3]	MUSTN[3]
CLD[3]	W14=LCD data bit 3 (01)	CUSTN[4]	CUSTN[4]	MUSTN[0]	MUSTN[0][1]	MUSTN[4]	MUSTN[4]
CLD[2]	Y14=LCD data bit 2 (01)	CUSTN[5]	CUSTN[5]	MUSTN[1]	MUSTN[1]	MUSTN[5]	MUSTN[5]
CLD[1]	V13=LCD data bit 1 (01)	CUSTN[6]	CUSTN[6]	MUSTN[2]	MUSTN[2]	MUSTN[6]	MUSTN[6]
CLD[0]	W13=LCD data bit 0 (01)	CUSTN[7]	CUSTN[7]	MUSTN[3]	MUSTN[3]	MUSTN[7]	MUSTN[7]

1 This data bit corresponds to the first “pixel position.” For example, for an 8-bit mono STN display, CUSTN[0] is the leftmost pixel on the panel and CUSTN[7] is the rightmost pixel within the 8-bit data. For a color STN display, bits [7, 6, 5] form the leftmost pixel.

Table 12: CLD[17:0] pin descriptions for STN display

Table 13 shows which CLD[17:0] pins provide the pixel data to the TFT panel for each of the multiplexing modes of operation.

BBus peripheral address map

The BBus bridge configuration registers are located at base address 0xA040 0000. The BBus peripherals are located at base address 0x9000 0000 and span a 256 MB address space. Each BBus peripheral, with the exception of the SER port controllers, resides in a separate 1 MB address space. This table shows the address space given to each peripheral.

Base address	Peripheral
0x9000 0000	BBus DMA controller
0x9010 0000	Reserved
0x9020 0000	SER Port B
0x9020 0040	SER Port A
0x9030 0000	SER Port C
0x9030 0040	SER Port D
0x9040 0000	IEEE 1284 controller
0x9050 0000	I^2C controller
0x9060 0000	BBus utility
0x9070 0000	Real Time Clock
0x9080 0000	USB Host
0x9090 0000	USB Device

Table 21: BBus peripheral address map

DC electrical characteristics

DC electrical characteristics specify the worst-case DC electrical performance of the I/O buffers that are guaranteed over the specified temperature range.

Inputs

All electrical inputs are 3.3V interface.

Note: V_{SS} = 0V (GND)

Sym	Parameter	Condition	Value		Unit
V_{IH}	High-level input voltage: LVTTL level		Min	2.0	V
V_{IL}	Low-level input voltage: LVTTL level		Max	0.8	V
I_{IH}	High-level input current (no pulldown) Input buffer with pulldown	$V_{INA}=V_{DDA}$	Min/Max Min/Max	-10/10 10/200	µA µA
I_{IL}	Low-level input current (no pullup) Input buffer with pullup	$V_{INA}=V_{SS}$	Min/Max Min/Max	-10/10 10/200	µA µA
I_{OZ}	High-impedance leakage current	$V_{OUTA}=V_{DDA}$ or V_{SS}	Min/Max	-10/10	µA
I_{DDS}	Quiescent supply current	$V_{INA}=V_{DDA}$ or V_{SS}	Max	TBD	

USB internal PHY DC electrical inputs

Symbol	Parameter	Min	Max	Units	Notes
V_{IH}	Input high level (driven)	2.0		V	
V_{IZ}	Input high level (floating)	2.7	3.6	V	
V_{IL}	Input low level		0.8	V	
V_{DI}	Differential input sensitivity	0.2		V	1
V_{CM}	Differential common mode range	0.8	2.5	V	2

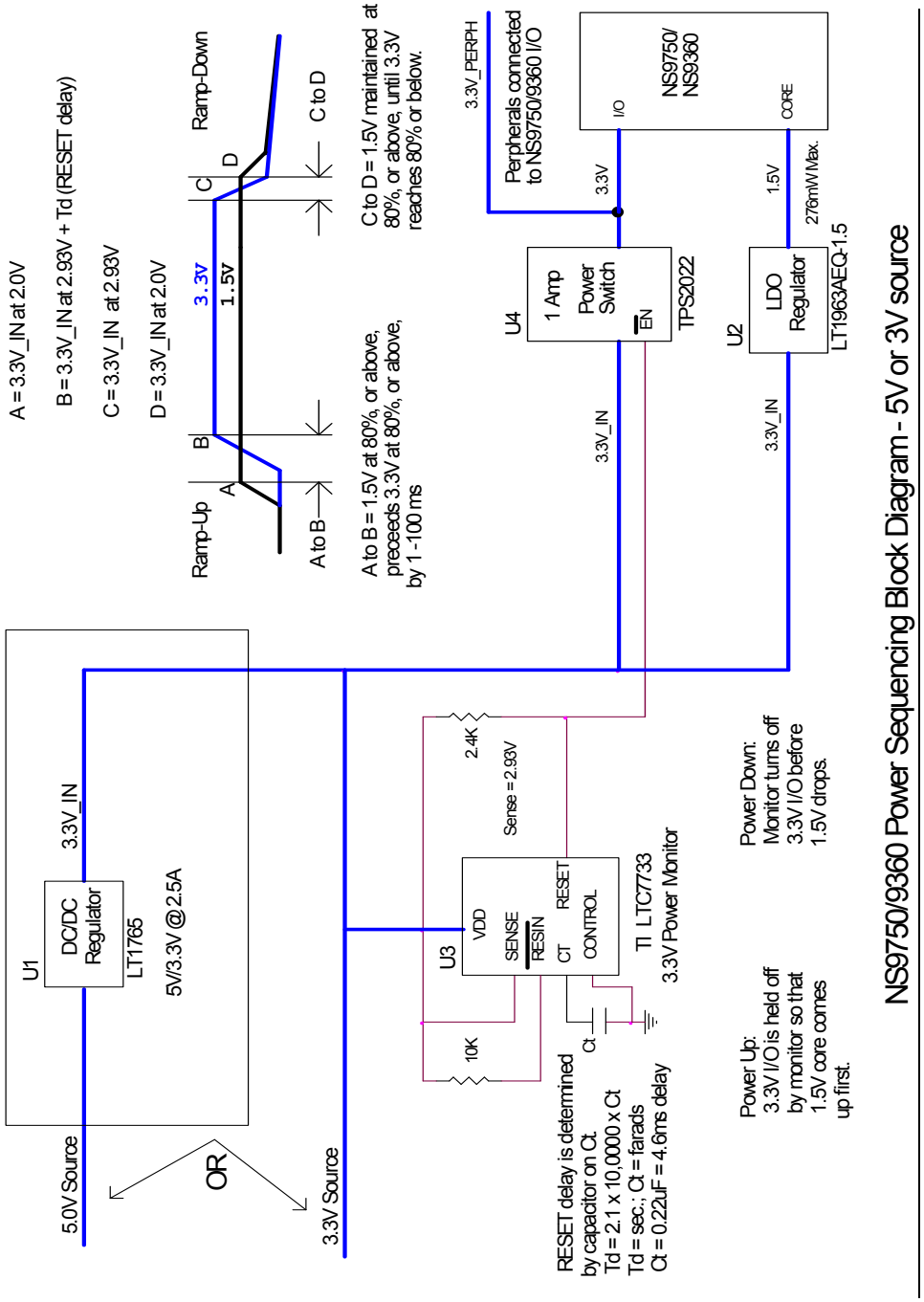
Notes:

1 |(usb_dp) - (usb_dm)|

2 Includes V_{DI} range.

Power sequencing

Use these requirements for power sequencing.



Memory timing

Memory AC characteristics are measured with 35pF.

Memory timing contains parameters and diagrams for both SDRAM and SRAM timing.

SDRAM timing diagrams

Table 24 describes the values shown in the SDRAM timing diagrams.

Parameter	Description	Min	Max	Unit	Notes
M1	data input setup time to rising	1.0		ns	
M2	data input hold time to rising	0.0		ns	
M3	clk_out high to clk_en high		6.4	ns	
M4	clk_out high to address valid		6.4	ns	
M5	clk_out high to data_mask		6.4	ns	1, 2
M6	clk_out high to dy_cs_n low		6.4	ns	3, 4
M7	clk_out high to ras_n low		6.4	ns	
M8	clk_out high to cas_n low		6.4	ns	
M9	clk_out high to we_n low		6.4	ns	
M10	clk_out high to data out		6.6	ns	
M11	address hold time	4.0			
M12	data out hold time	4.0			
M13	clk_en high to sdram access	2	2	clock	
M14	end sdram access to clk_en low	2	2	clocks	

Table 24: SDRAM timing parameters

Notes:

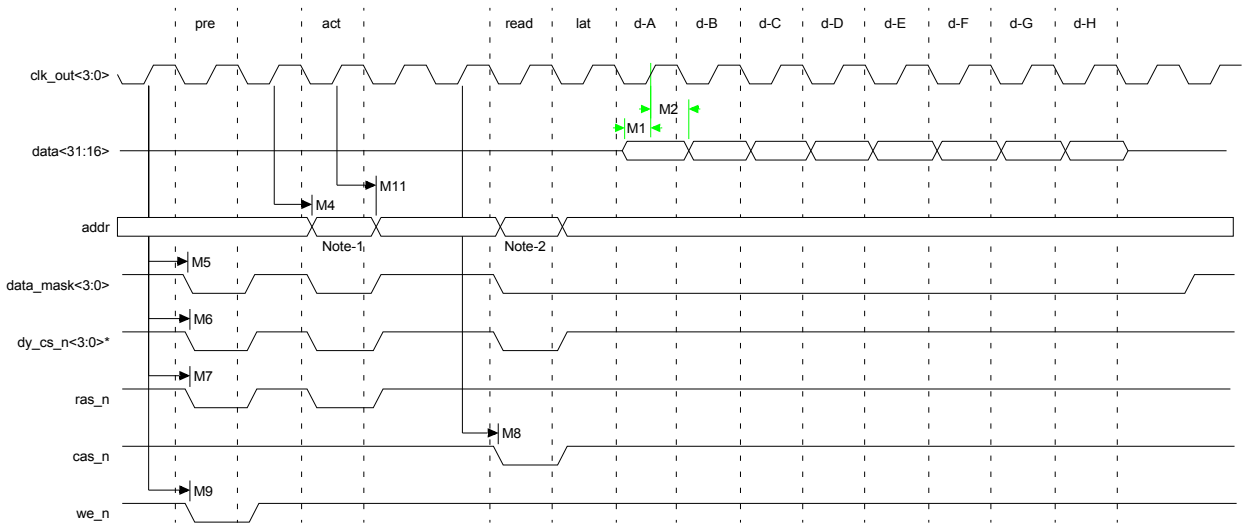
1 All four data_mask signals are used for all transfers.

2 All four data_mask signals will go low during a read cycle, for both 16-bit and 32-bit transfers.

3 Only one of the four clk_out signals is used.

4 Only one of the four dy_cs_n signals is used.

SDRAM burst read (16-bit)

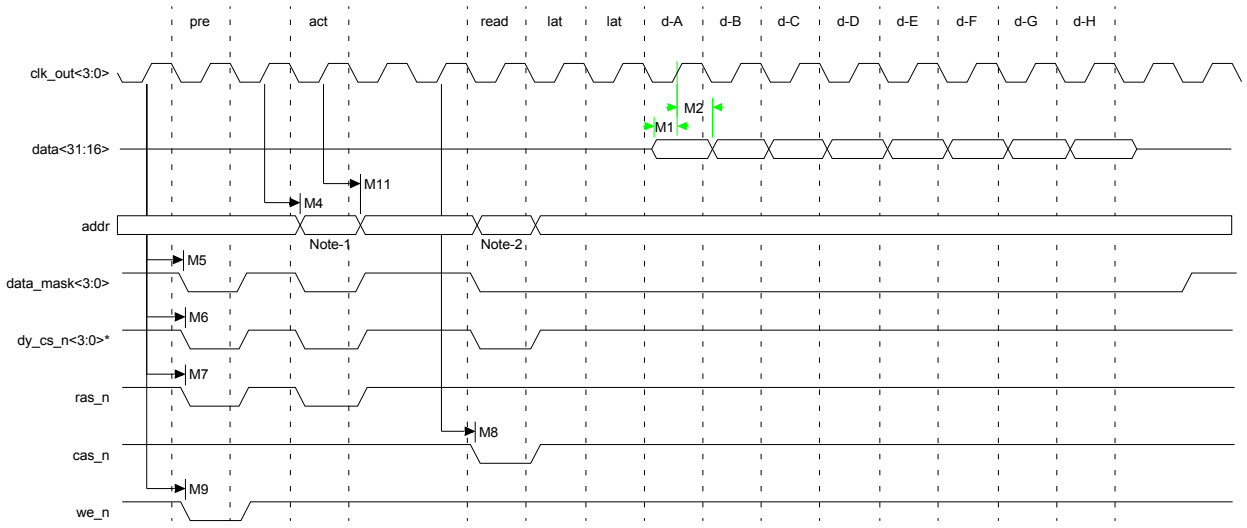


Notes:

1 This is the bank and RAS address.

2 This is the CAS address.

SDRAM burst read (16-bit), CAS latency = 3

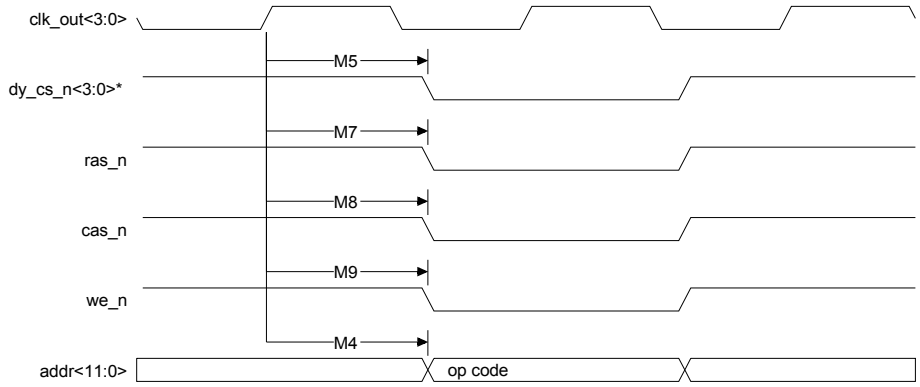


Notes:

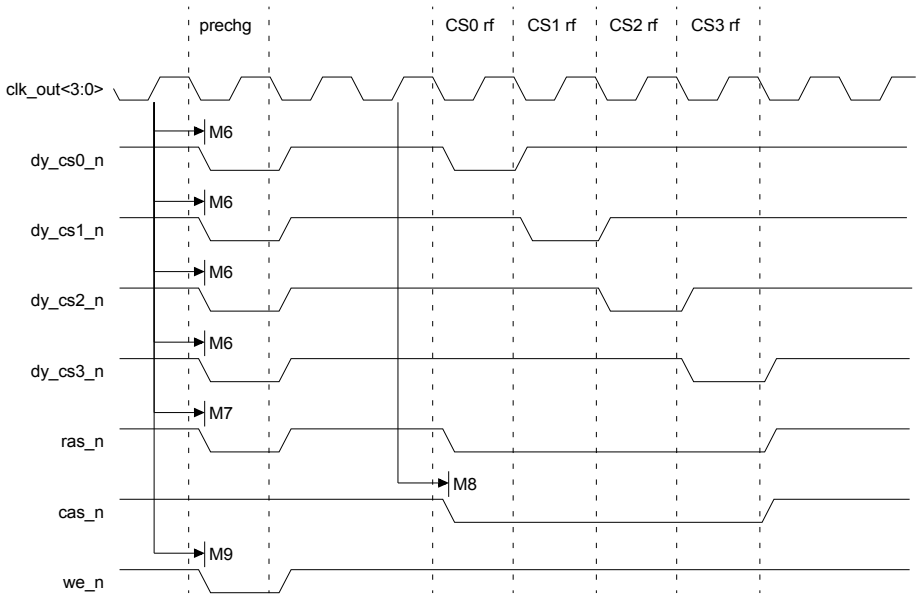
1 This is the bank and RAS address.

2 This is the CAS address.

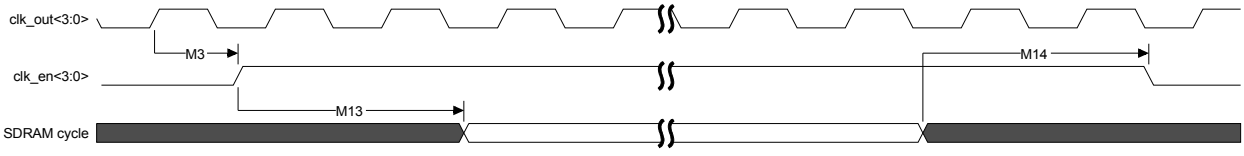
SDRAM load mode



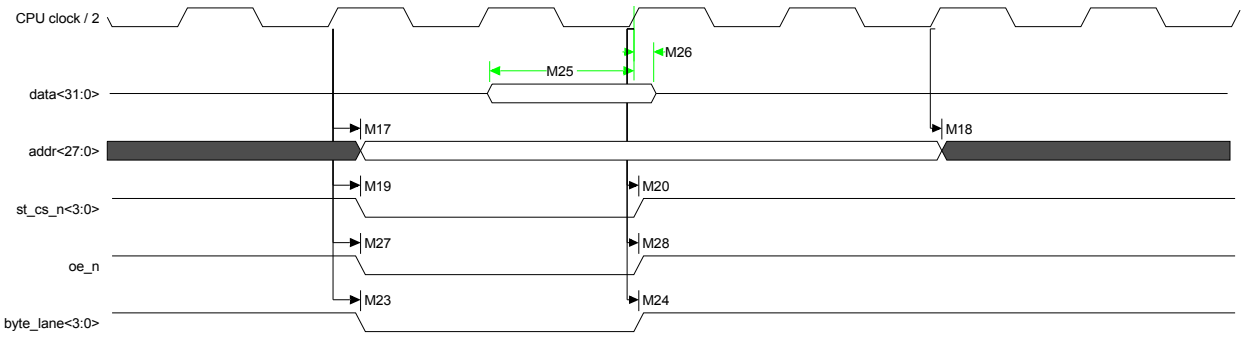
SDRAM refresh mode



Clock enable timing

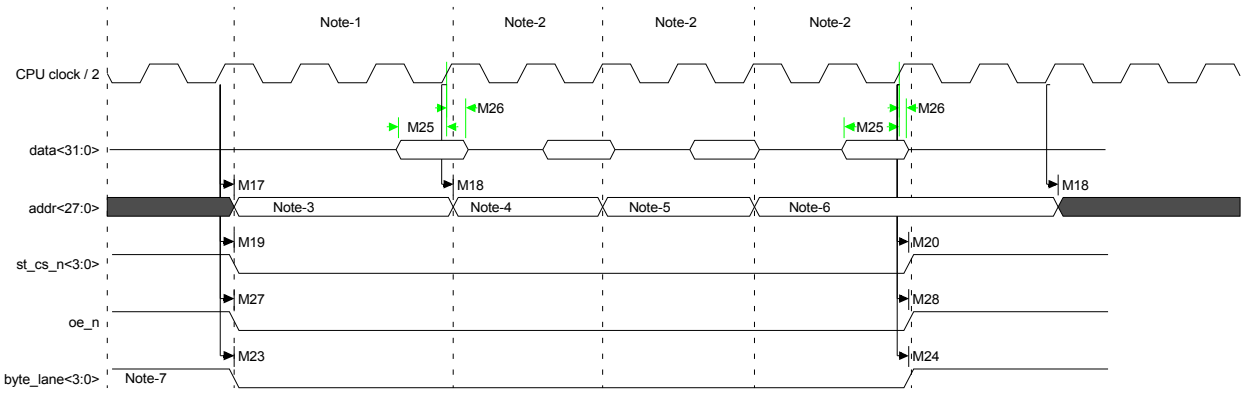


Static RAM read cycles with 1 wait states



- WTRD = 1
  WOEN = 0
- If the PB field is set to 1, all four byte_lane signals will go low for 32-bit, 16-bit, and 8-bit read cycles.
- If the PB field is set to 0, the byte_lane signal will always be high.

Static RAM asynchronous page mode read, WTPG = 1



- WTPG = 1
  WTRD = 2
- If the PB field is set to 1, all four byte_lane signals will go low for 32-bit, 16-bit, and 8-bit read cycles.
- The asynchronous page mode will read 16 bytes in a page cycle. A 32-bit bus will do four 32-bit reads, as shown (3-2-2-2). A 16-bit bus will do eight 16-bit reads (3-2-2-2-3-2-2-2) per page cycle, and an 8-bit bus will do sixteen reads (3-2-2-2-3-2-2-2-3-2-2-2-3-2-2-2) per page cycle. 3-2-2-2 is the example used here, but the WTRD and WTPG field can set them differently.

Notes:

1 The length of the first cycle in the page is determined by the WTRD field.

2 The length of the 2nd, 3rd, and 4th cycles is determined by the WTPG field.

3 This is the starting address. The least significant two bits will always be ‘00.’

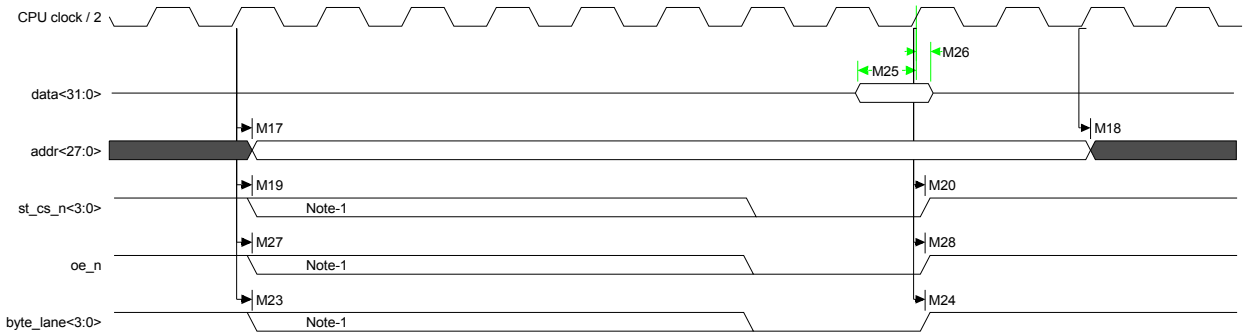
4 The least significant two bits in the second cycle will always be ‘01.’

5 The least significant bits in the third cycle will always be ‘10.’

6 The least significant two bits in the fourth cycle will always be ‘11.’

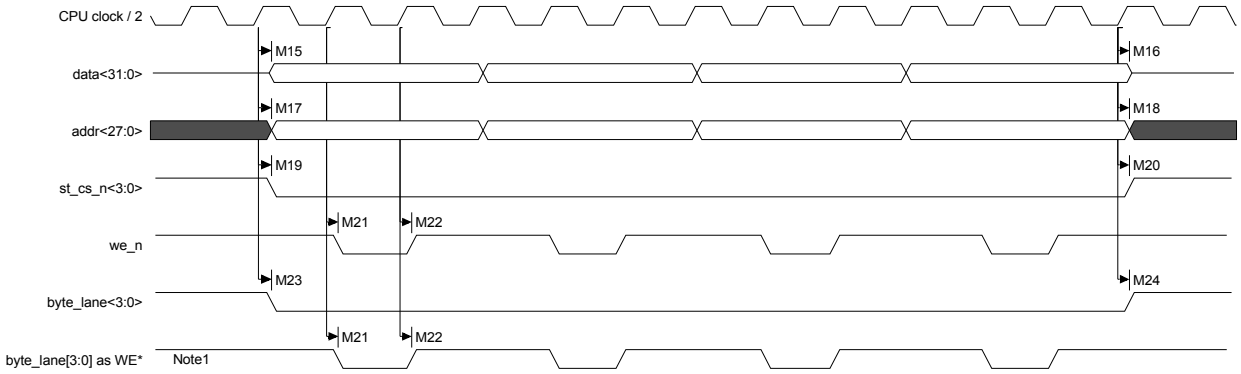
7 If the PB field is set to 0, the byte_lane signal will always be high during a read cycle.

Static RAM read cycle with configurable wait states



- WTRD = from 1 to 15
  WOEN = from 0 to 15
- If the PB field is set to 1, all four byte_lane signals will go low for 32-bit, 16-bit, and 8-bit read cycles.
- If the PB field is set to 0, the byte_lane signal will always be high.

Static RAM sequential write cycles



- WTWR = 0
  WWEN = 0
- During a 32-bit transfer, all four byte_lane signals will go low.
- During a 16-bit transfer, two byte_lane signals will go low.
- During an 8-bit transfer, only one byte_lane signal will go low.

Note:

1 If the PB field is set to 0, the byte_lane signals will function as write enable signals and the we_n signal will always be high.

Slow peripheral acknowledge timing

Table 26 describes the values shown in the slow peripheral acknowledge timing diagrams.

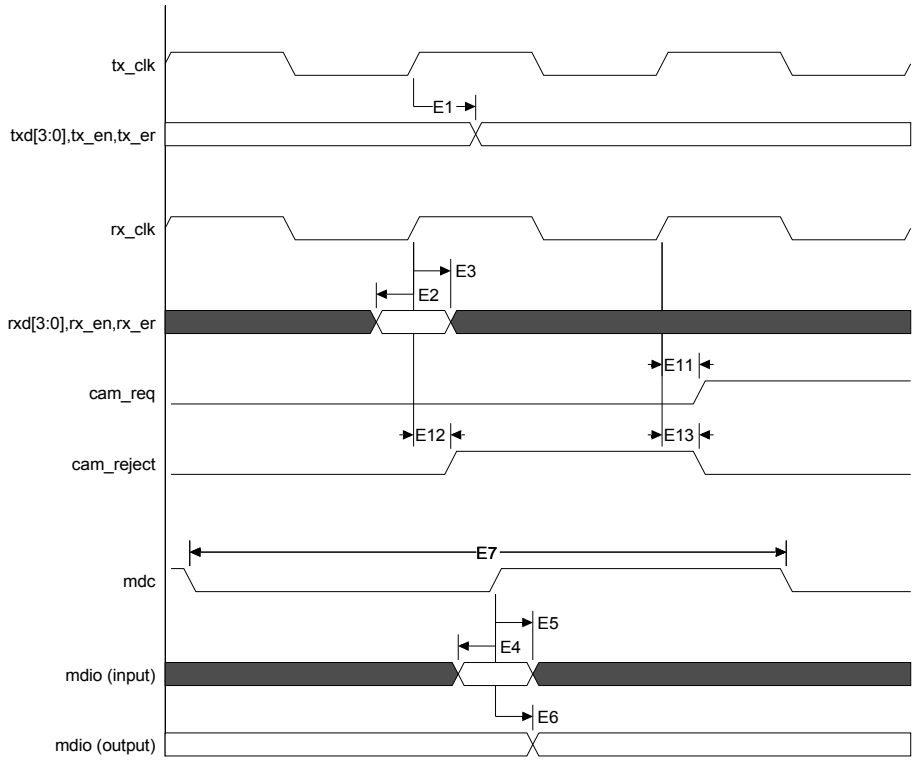
Parameter	Description	Min	Max	Unit	Notes
M15	clock high to data out valid	-2	+2	ns	
M16	data out hold time from clock high	-2	+2	ns	
M17	clock high to address valid	-2	+2	ns	
M18	address hold time from clock high	-2	+2	ns	
M19	clock high to st_cs_n low	-2	+2	ns	1
M20	clock high to st_cs_n high	-2	+2	ns	1
M21	clock high to we_n low	-2	+2	ns	
M22	clock high to we_n high	-2	+2	ns	
M23	clock high to byte_lanes low	-2	+2	ns	
M24	clock high to byte_lanes high	-2	+2	ns	
M26	data input hold time to rising clk	0		ns	
M27	clock high to oe_n low	-2	+2	ns	
M28	clock high to oe_n high	-2	+2	ns	
M29	address/chip select valid to ta_strb high	2		CPU cycles	
M30	ta_strb pulse width	4	8	CPU cycles	
M31	ta_strb rising to chip select/address change	4	10	CPU cycles	
M32	data setup to ta_strb rising	0		ns	

Table 26: Slow peripheral acknowledge

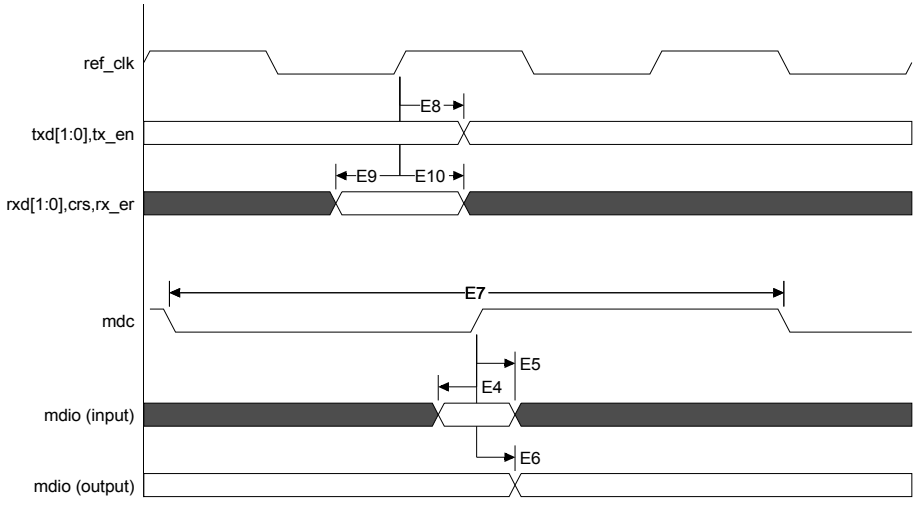
Note:

1 Only one of the four st_cs_n signals is used. The diagrams show the active low configuration, which can be reversed (active high) with PC field.

Ethernet MII timing



Ethernet RMII timing



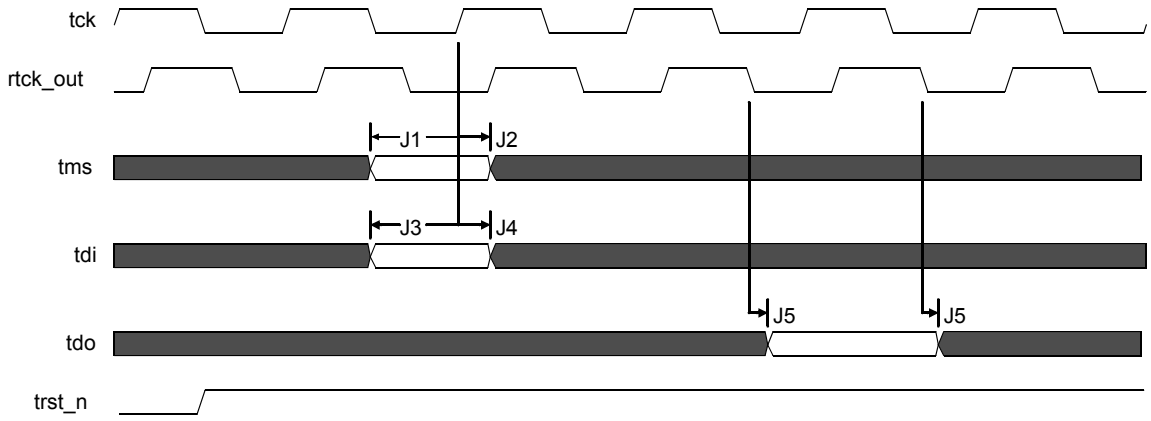
JTAG timing

JTAG AC characteristics are measured with 10pF.

Table 36 describes the values shown in the JTAG timing diagram.

Parameter	Description	Min	Max	Unit
J1	tms (input) setup to tck rising	5		ns
J2	tms (input) hold to tck rising	2		ns
J3	tdi (input) setup to tck rising	5		ns
J4	tdi (input) hold to tck rising	2		ns
J5	tdo (output) to tck falling	2.5	10	ns

Table 36: JTAG timing parameters



- Maximum tck rate is 10 MHz.
- rtck_out is an asynchronous output, driven off of the CPU clock.
- trst_n is an asynchronous input.