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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Not For New Designs
Applications	Network Processor
Core Processor	ARM9®
Program Memory Type	External Program Memory
Controller Series	-
RAM Size	External
Interface	EBI/EMI, Ethernet, DMA, I²C, IEEE 1284, LCD, SPI, UART, USB
Number of I/O	73
Voltage - Supply	1.4V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	272-BBGA
Supplier Device Package	272-BGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/digi-international/ns9360b-0-i155

Contents

USB ports

- USB v.2.0 full speed (12 Mbps) and low speed (1.5 Mbps)
- Independent OHCI Host and Device ports
- Internal USB PHY
- External USB PHY interface
- USB device supports one bidirectional control endpoint and 10 unidirectional endpoints
- All endpoints supported by a dedicated DMA channel
- 32 byte FIFO per endpoint

Serial ports

- 4 serial modules, each independently configurable to UART mode, SPI master mode, or SPI slave mode
- Bit rates from 75 bps to 921.6 kbps: asynchronous x16 mode
- Bit rates from 1.2 kbps to 11.25 Mbps: synchronous mode
- UART provides:
  - High-performance hardware and software flow control
  - Odd, even, or no parity
  - 5, 6, 7, or 8 bits
  - 1 or 2 stop bits
  - Receive-side character and buffer gap timers
- Internal or external clock support, digital PLL for RX clock extraction
- 4 receive-side data match detectors
- 2 dedicated DMA channels per module, 8 channels total
- 32 byte TX FIFO and 32 byte RX FIFO per module

I^2C port

- I^2C v.1.0, configurable to master or slave mode
- Bit rates: fast (400 kHz) or normal (100 kHz) with clock stretching
- 7-bit and 10-bit address modes
- Supports I^2C bus arbitration

1284 parallel peripheral port

- All standard modes: ECP, byte, nibble, compatibility (also known as SPP or “Centronix”)
- RLE (run length encoding) decoding of compressed data in ECP mode
- Operating clock from 100 kHz to 2 MHz

High performance multiple-master/distributed DMA system

- Intelligent bus bandwidth allocation (patent pending)
- System bus and peripheral bus

System bus:

- Every system bus peripheral is a bus master with a dedicated DMA engine

Peripheral bus:

- One 12-channel DMA engine supports USB device
  - 2 DMA channels support control endpoint
  - 10 DMA channels support 10 endpoints
- One 12-channel DMA engine supports:
  - 4 serial modules (8 DMA channels)
  - 1284 parallel port (4 DMA channels)
- All DMA channels support fly-by mode

External peripheral:

- One 2-channel DMA engine supports external peripheral connected to memory bus
- Each DMA channel supports memory-to-memory transfers

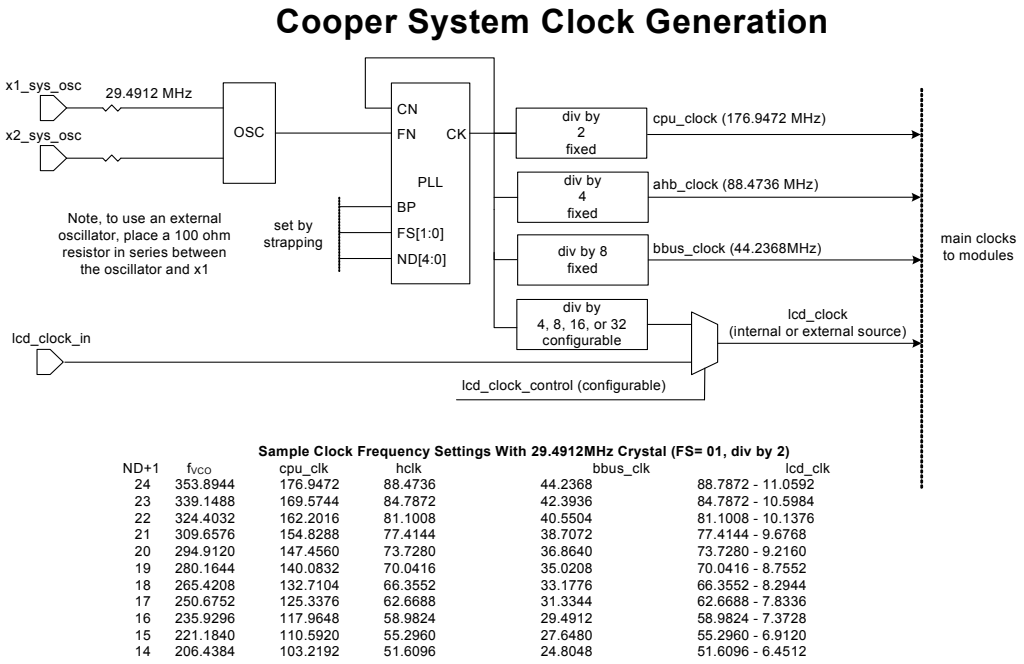
System boot

There are two ways to boot the NS9360 system:

- From a fast Flash over the system memory bus.
- From an inexpensive, but slower, serial EEPROM through SPI port B.

Both boot methods are glueless. The bootstrap pin, RESET_DONEn, indicates where to boot on a system powerup. Flash boot can be done from 8-bit, 16-bit, or 32-bit ROM or Flash.

Serial EEPROM boot is supported by NS9360 hardware. A configuration header in the EEPROM specifies total number of words to be fetched from EEPROM, as well as a system memory configuration and a memory controller configuration. The boot engine configures the memory controller and system memory, fetches data from low-cost serial EEPROM, and writes the data to external system memory, holding the CPU in reset.



Sample Clock Frequency Settings With 29.4912MHz Crystal (FS= 01, div by 2)

ND+1	f_{vco}	cpu_clk	hclk	bbus_clk	lcd_clk
24	353.8944	176.9472	88.4736	44.2368	88.7872 - 11.0592
23	339.1488	169.5744	84.7872	42.3936	84.7872 - 10.5984
22	324.4032	162.2016	81.1008	40.5504	81.1008 - 10.1376
21	309.6576	154.8288	77.4144	38.7072	77.4144 - 9.6768
20	294.9120	147.4560	73.7280	36.8640	73.7280 - 9.2160
19	280.1644	140.0832	70.0416	35.0208	70.0416 - 8.7552
18	265.4208	132.7104	66.3552	33.1776	66.3552 - 8.2944
17	250.6752	125.3376	62.6688	31.3344	62.6688 - 7.8336
16	235.9296	117.9648	58.9824	29.4912	58.9824 - 7.3728
15	221.1840	110.5920	55.2960	27.6480	55.2960 - 6.9120
14	206.4384	103.2192	51.6096	24.8048	51.6096 - 6.4512

Figure 3: NS9360 system clock generation (PLL)

You can use this formula to calculate the system clock frequencies if a different

system oscillator frequency is used:

You can use this formula to calculate the system clock frequencies if a different system oscillator frequency is used:

f_{vco} = (f_{osc} x (ND + 1) / FS)

f_{cpu_clk} = f_{vco} / 2

f_{hclk} = f_{vco} / 4

f_{bbuys_clk} = f_{vco} / 8

f_{lcd_clk} = programmable, f_{vco} / 4, 8, 16, or 32

Name	I/O	Description
clk_en[3:0]	O	SDRAM clock enable. Used for SDRAM devices. These signals are muxed behind gpio[71:68]. Note: The clk_en signals are associated with the dy_cs_n signals. If clock enables are used, a pullup resistor is required to prevent floating during startup, and to avoid SDRAM lockup during manual or brown out conditions. If not used, connect the clock enables in the SDRAM devices directly to 3.3v or a pullup resistor.
clk_out[3:0]	O	SDRAM clocks. Used for SDRAM devices. SDRAM clk_out[1] is connected to clk_in.
data[31:0]	I/O	Read data from memory. Used for the static memory controller and the dynamic memory controller.
data_mask[3:0]	O	Data mask output to SDRAMs. Used for SDRAM devices.
clk_in	I	Feedback clock. Always connects to clk_out[1].
byte_lane_sel_n[3:0]	O	Static memory byte_lane_select, active low, or write_enable_n for byte-wide devices.
cas_n	O	Column address strobe. Used for SDRAM devices.
dy_cs_n[3:0]	O	SDRAM chip selects. Used for SDRAM devices.
st_oe_n	O	Output enable for static memories. Used for static memory devices.
ras_n	O	Row address strobe. Used for SDRAM devices.
st_cs_n[3:0]	O	Static memory chip selects. Default active low. Used for static memory devices.
we_n	O	Write enable. Used for SDRAM and static memories.
ta_strb	I	*Slow peripheral transfer acknowledge* can be used to terminate static memory cycles sooner than the number of wait states programmed in the chip select setup register. This signal is muxed being gpio[72].

Table 6: System Memory interface signal descriptions

Figure 5, "SDRAM clock termination," on page 19, shows an example of NS9360 SDRAM clock termination. clk_out[1] is shown, but you can use any clk_out signal (0, 1, 2, or 3).

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)	
U15	gpio[35]	U	4	I/O	00	iic_sda
					01	1284 Data 4 (bidirectional)
					02	LCD data bit 11
					03	GPIO 35
V16	gpio[36]	U	4	I/O	00	PWM ch 0
					01	1284 Data 5 (bidirectional)
					02	LCD data bit 12
					03	GPIO 36
W17	gpio[37]	U	4	I/O	00	PWM ch 1
					01	1284 Data 6 (bidirectional)
					02	LCD data bit 13
					03	GPIO 37
Y18	gpio[38]	U	4	I/O	00	PWM ch2
					01	1284 Data 7 (bidirectional)
					02	LCD data bit 14
					03	GPIO 38
U16	gpio[39]	U	4	I/O	00	PWM ch3
					01	1284 Data 8 (bidirectional)
					02	LCD data bit 15
					03	GPIO 39
V17	gpio[40]	U	4	I/O	00	Ser port C TXData / SPI port C dout
					01	Ext IRQ 3
					02	LCD data bit 16
					03	GPIO 40
W18	gpio[41]	U	4	I/O	00	Ser port C RXData / SPI port C din
					01	Reserved
					02	LCD data bit 17
					03	GPIO 41
U18	gpio[42]		2	I/O	00	Ser port C RTS
					01	Reserved
					02	USB phy data + (TX and RX data for bidirectional PHY or TX data only for unidirectional PHY)
					03	GPIO 42
V20	gpio[43]		2	I/O	00	Ser port C CTS
					01	1284 transceiver direction control
					02	USB phy data - (TX and RX data for bidirectional PHY or TX data only for unidirectional PHY)
					03	GPIO 43

Table 10: GPIO MUX pinout

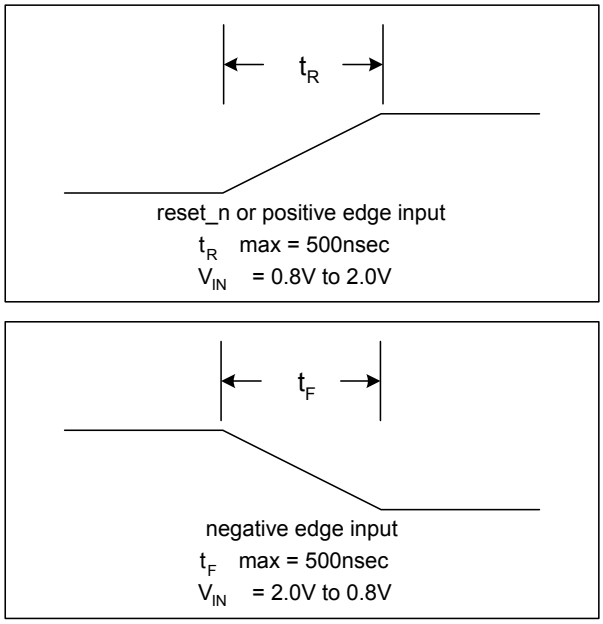
Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)	
K1	gpio[61]		2	I/O	00	MII tx data bit 2
					01	Reserved
					02	Reserved
					03	GPIO 61
K3	gpio[62]		2	I/O	00	MII tx data bit 3
					01	Reserved
					02	Reserved
					03	GPIO 62
P2	gpio[63]		2	I/O	00	MII collision
					01	Reserved
					02	Reserved
					03	GPIO 63
R1	gpio[64]		2	I/O	00	MII/RMII carrier sense
					01	Reserved
					02	Reserved
					03	GPIO 64
P1	gpio[65]	U	2	I/O	00	MII/RMII enet phy interrupt
					01	Reserved
					02	Reserved
					03	GPIO 65
H19	gpio[66]		8	I/O	00	Mem addr[22]
					01	Reserved
					02	Reserved
					03	GPIO 66
E18	gpio[67]		8	I/O	00	Mem addr[23]
					01	Reserved
					02	Reserved
					03	GPIO 67
D19	gpio[68]		8	I/O	00	Mem addr[24]
					01	Mem clk_en[0]
					02	Ext IRQ 0 (duplicate)
					03	GPIO 68
C20	gpio[69]		8	I/O	00	Mem addr[25]
					01	Mem clk_en[1]
					02	Ext IRQ 1 (duplicate)
					03	GPIO 69
A17	gpio[70]		8	I/O	00	Mem addr[26]
					01	Mem clk_en[2]
					02	iic_scl (duplicate)
					03	GPIO 70

Table 10: GPIO MUX pinout

Reset and edge sensitive input timing requirements

The critical timing requirement is the rise and fall time of the input. If the rise time is too slow for the reset input, the hardware strapping options may be registered incorrectly. If the rise time of a positive-edge-triggered external interrupt is too slow, then an interrupt may be detected on both the rising and falling edge of the input signal.

A maximum rise and fall time must be met to ensure that reset and edge sensitive inputs are handled correctly. With Digi processors, the maximum is 500 nanoseconds as shown:



If an external device driving the reset or edge sensitive input on a Digi processor cannot meet the 500ns maximum rise and fall time requirement, the signal must be buffered with a Schmitt trigger device. Here are sample Schmitt trigger device part numbers:

Manufacturer	Part number	Description
Fairchild	NC7SP17	Single Schmitt trigger buffer, available in 5-lead SC70 and 6-lead MicroPak packages
Philips	74LVC1G17GW	Single Schmitt trigger buffer, available in 5-lead SC70 and SOT 353 packages
TI	SN74LVC1G17DCK	Single Schmitt trigger buffer, available in 5-lead SC70 and SOT 353 packages
ON Semi	NL17SZ17DFT2	Single Schmitt trigger buffer, available in 5-lead SC70 and SOT 353 packages.

Memory timing

Memory AC characteristics are measured with 35pF.

Memory timing contains parameters and diagrams for both SDRAM and SRAM timing.

SDRAM timing diagrams

Table 24 describes the values shown in the SDRAM timing diagrams.

Parameter	Description	Min	Max	Unit	Notes
M1	data input setup time to rising	1.0		ns	
M2	data input hold time to rising	0.0		ns	
M3	clk_out high to clk_en high		6.4	ns	
M4	clk_out high to address valid		6.4	ns	
M5	clk_out high to data_mask		6.4	ns	1, 2
M6	clk_out high to dy_cs_n low		6.4	ns	3, 4
M7	clk_out high to ras_n low		6.4	ns	
M8	clk_out high to cas_n low		6.4	ns	
M9	clk_out high to we_n low		6.4	ns	
M10	clk_out high to data out		6.6	ns	
M11	address hold time	4.0			
M12	data out hold time	4.0			
M13	clk_en high to sdram access	2	2	clock	
M14	end sdram access to clk_en low	2	2	clocks	

Table 24: SDRAM timing parameters

Notes:

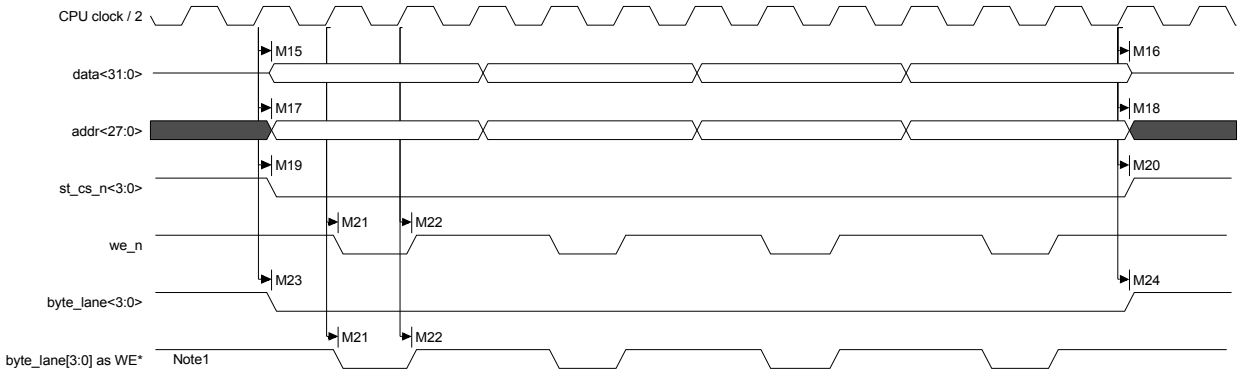
1 All four data_mask signals are used for all transfers.

2 All four data_mask signals will go low during a read cycle, for both 16-bit and 32-bit transfers.

3 Only one of the four clk_out signals is used.

4 Only one of the four dy_cs_n signals is used.

Static RAM sequential write cycles

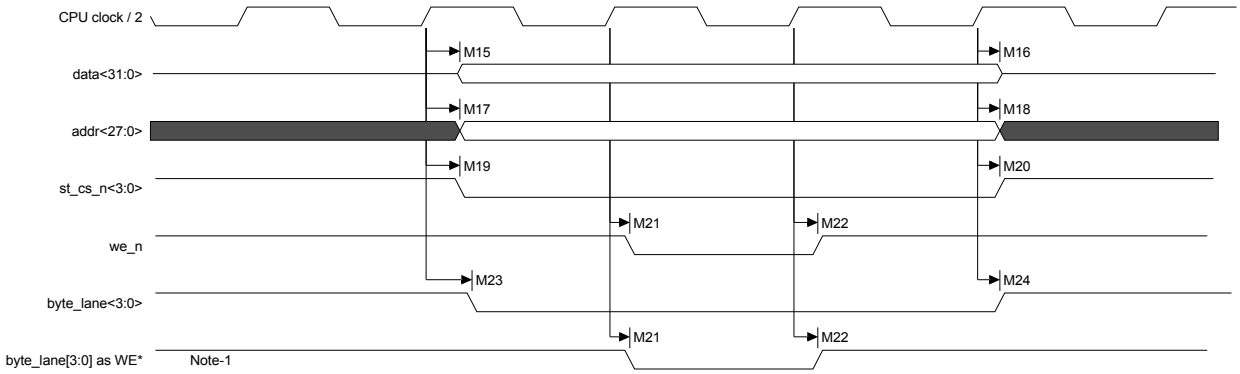


- WTWR = 0
  WWEN = 0
- During a 32-bit transfer, all four byte_lane signals will go low.
- During a 16-bit transfer, two byte_lane signals will go low.
- During an 8-bit transfer, only one byte_lane signal will go low.

Note:

1 If the PB field is set to 0, the byte_lane signals will function as write enable signals and the we_n signal will always be high.

Static RAM write cycle

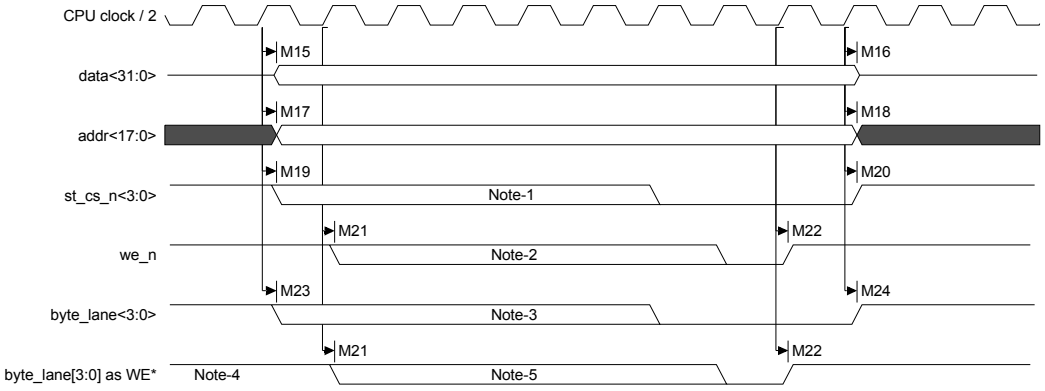


- WTWR = 0
  WWEN = 0
- During a 32-bit transfer, all four byte_lane signals will go low.
- During a 16-bit transfer, two byte_lane signals will go low.
- During an 8-bit transfer, only one byte_lane signal will go low.

Note:

1 If the PB field is set to 0, the byte_lane signals will function as write enable signals and the we_n signal will always be high.

Static write cycle with configurable wait states



- WTWR = from 0 to 15
  WWEN = from 0 to 15
- The WTWR field determines the length on the write cycle.
- During a 32-bit transfer, all four byte_lane signals will go low.
- During a 16-bit transfer, two byte_lane signals will go low.
- During an 8-bit transfer, only one byte_lane signal will go low.

Notes:

1 Timing of the st_cs_n signal is determined with a combination of the WTWR and WWEN fields. The st_cs_n signal will always go low at least one clock before we_n goes low, and will go high one clock after we_n goes high.

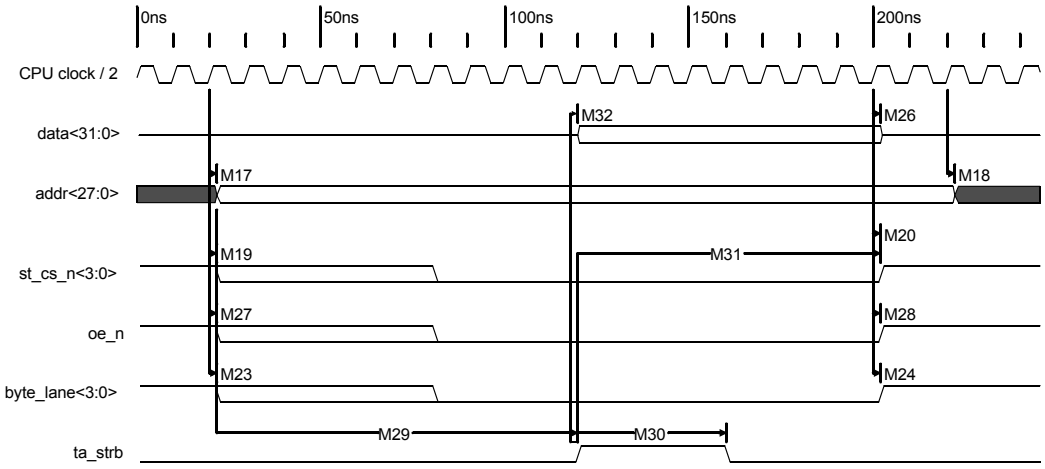
2 Timing of the we_n signal is determined with a combination of the WTWR and WWEN fields.

3 Timing of the byte_lane signals is determined with a combination of the WTWR and WWEN fields. The byte_lane signals will always go low one clock before we_n goes low, and will go one clock high after we_n goes high.

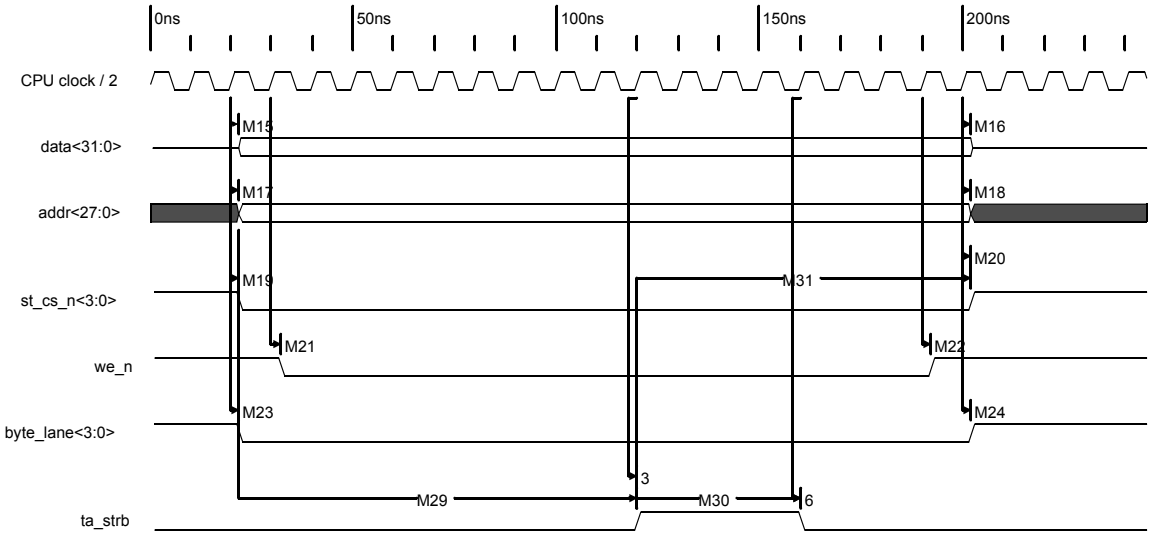
4 If the PB field is set to 0, the byte_lane signals will function as the write enable signals and the we_n signal will always be high.

5 If the PB field is set to 0, the timing for the byte_lane signals is set with the WTWR and WWEN fields.

Slow peripheral acknowledge read



Slow peripheral acknowledge write



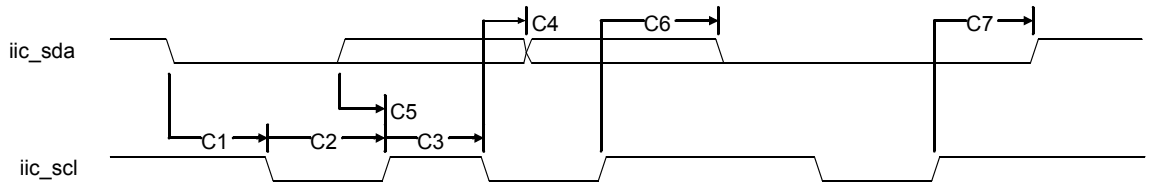
I²C timing

I²C AC characteristics are measured with 10pf.

Table 28 describes the values shown in the I²C timing diagram.

		Standard mode		Fast mode		
Parm	**Description**	**Min**	**Max**	**Min**	**Max**	**Unit**
C1	iic_sda to iic_scl START hold time	4.0		0.6		µs
C2	iic_scl low period	4.7		1.3		µs
C3	iic_scl high period	4.7		1.3		µs
C4	iic_scl to iic_sda DATA hold time	0		0		µs
C5	iic_sda to iic_scl DATA setup time	250		100		ns
C6	iic_scl to iic_sda START setup time	4.7		0.6		µs
C7	iic_scl to iic_sda STOP setup time	4.0		0.6		µs

Table 28: I²C timing parameters



SPI timing

SPI AC characteristics are measured with 10pF, unless otherwise noted.

Table 30 describes the values shown in the SPI timing diagrams.

Parm	Description	Min	Max	Unit	Modes	Notes
SPI master parameters						
SP0	SPI enable low setup to first SPI CLK out rising	$3*T_{BCLK}$-10		ns	0, 3	1, 3
SP1	SPI enable low setup to first SPI CLK out falling	$3*T_{BCLK}$-10		ns	1, 2	1, 3
SP3	SPI data in setup to SPI CLK out rising	30		ns	0, 3	
SP4	SPI data in hold from SPI CLK out rising	0		ns	0, 3	
SP5	SPI data in setup to SPI CLK out falling	30		ns	1, 2	
SP6	SPI data in hold from SPI CLK out falling	0		ns	1, 2	
SP7	SPI CLK out falling to SPI data out valid		10	ns	0, 3	6
SP8	SPI CLK out rising to SPI data out valid		10	ns	1, 2	6
SP9	SPI enable low hold from last SPI CLK out falling	$3*T_{BCLK}$-10		ns	0, 3	1, 3
SP10	SPI enable low hold from last SPI CLK out rising	$3*T_{BCLK}$-10		ns	1, 2	1, 3
SP11	SPI CLK out high time	SP13*45%	SP13*55%	ns	0, 1, 2, 3	4
SP12	SPI CLK out low time	SP13*45%	SP13*55%	ns	0, 1, 2, 3	4
SP13	SPI CLK out period	T_{BCLK}*6		ns	0, 1, 2, 3	3
SPI slave parameters						
SP14	SPI enable low setup to first SPI CLK in rising	30		ns	0, 3	1
SP15	SPI enable low setup to first SPI CLK in falling	30		ns	1, 2	1
SP16	SPI data in setup to SPI CLK in rising	0		ns	0, 3	
SP17	SPI data in hold from SPI CLK in rising	60		ns	0, 3	
SP18	SPI data in setup to SPI CLK in falling	0		ns	1, 2	
SP19	SPI data in hold from SPI CLK in falling	60		ns	1, 2	
SP20	SPI CLK in falling to SPI data out valid	20	70	ns	0, 3	6
SP21	SPI CLK in rising to SPI data out valid	20	70	ns	1, 2	6
SP22	SPI enable low hold from last SPI CLK in falling	15		ns	0, 3	1
SP23	SPI enable low hold from last SPI CLK in rising	15		ns	1, 2	1
SP24	SPI CLK in high time	SP26*40%	SP26*60%	ns	0, 1, 2, 3	5
SP25	SPI CLK in low time	SP26*40%	SP26*60%	ns	0, 1, 2, 3	5

Table 30: SPI timing parameters

Parm	Description	Min	Max	Unit	Modes	Notes
SP26	SPI CLK in period	T_{BCLK}*8		ns	0, 1, 2, 3	

Table 30: SPI timing parameters

Notes:

1 Active level of SPI enable is inverted (that is, 1) if the CSPOL bit in Serial Channel B/A/C/D Control Register B (see the *NS9360 Hardware Reference*) is set to 1. Note that in SPI slave mode, only a value of 0 (low enable) is valid; the SPI slave is fixed to an active low chip select.

2 SPI data order is reversed (that is, LSB last and MSB first) if the BITORDR bit in Serial Channel B/A/C/D Control Register B (see the *NS9360 Hardware Reference*) is set to 0.

3 T_{BCLK} is a period of BBus clock.

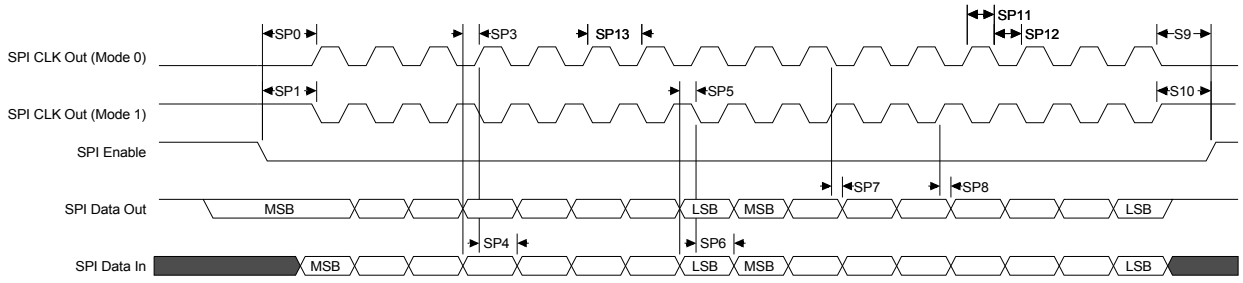
4 ±5% duty cycle skew.

5 ±10% duty cycle skew.

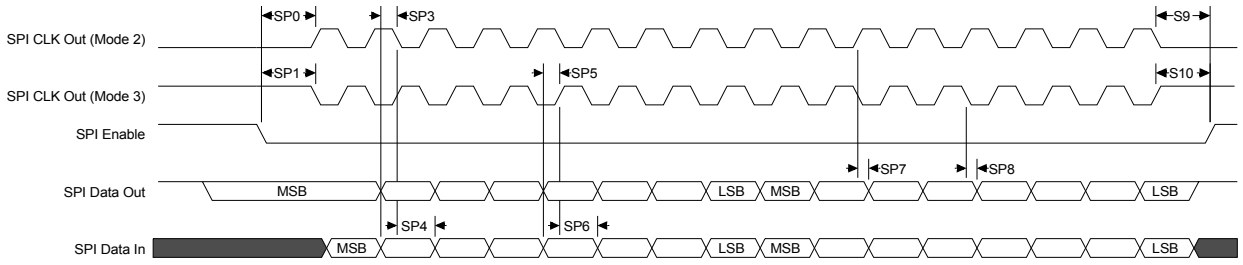
6 C_{load} = 5pf for all outputs.

7 SPI data order can be reversed such that LSB is first. Use the BITORDR bit in Serial Channel B/A/C/D Control Register A.

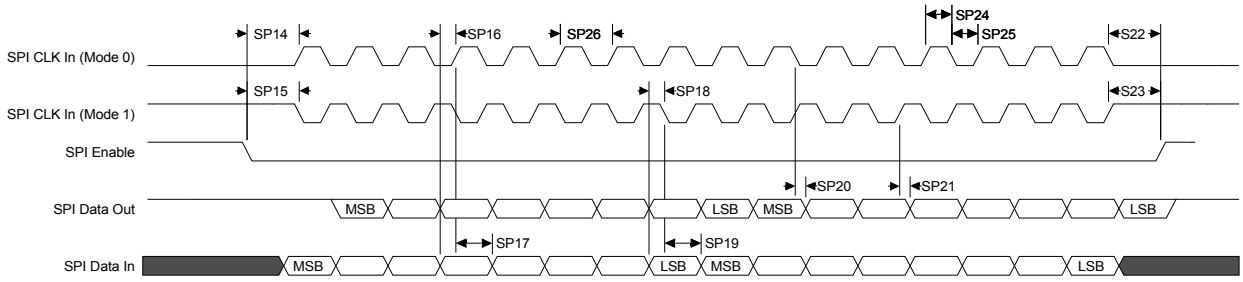
SPI master mode 0 and 1: 2-byte transfer (see note 7)



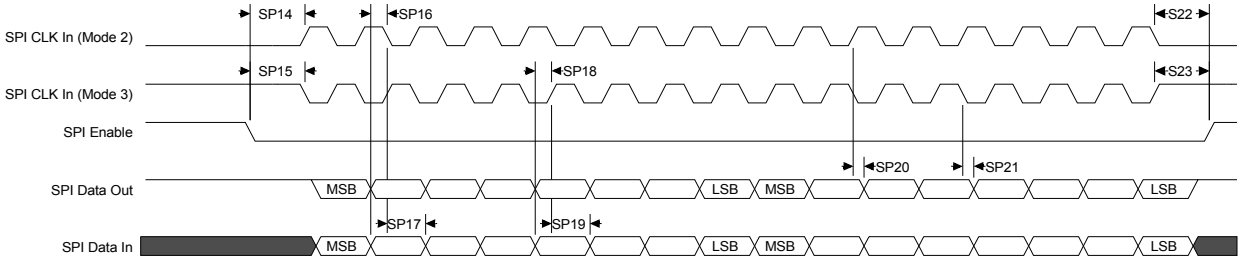
SPI master mode 2 and 3: 2-byte transfer (see note 7)



SPI slave mode 0 and 1: 2-byte transfer *(see note 7)*



SPI slave mode 2 and 3: 2-byte transfer *(see note 7)*



USB internal PHY timing

Table 32 and Table 33 describe the values shown in the USB internal PHY timing diagrams.

Parameter	Description	Min	Max	Unit	Notes
U1	Rise time (10%–90%)	4	20	ns	1
U2	Fall time (10%–90%)	4	20	ns	1
U3	Differential rise and fall time matching	90	111.11	%	1, 2, 5
U4	Driver output resistance	28	44	ohms	3

Table 32: USB internal PHY full speed timing parameters

Parameter	Description	Min	Max	Unit	Notes
U1	Rise time (10%–90%)	75	300	ns	4
U2	Fall time (10%–90%)	75%	300	ns	4
U3	Differential rise and fall time matching	80	125	%	2, 4, 5

Table 33: USB internal PHY low speed timing parameters

Notes:

1 Load shown in "USB internal PHY full speed load."

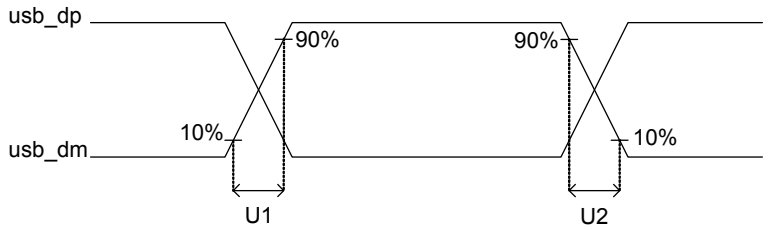
2 U1/U2.

3 Includes resistance of 27 ohm ±2 ohm external series resistor.

4 Load shown in "USB internal PHY low speed load."

5 Excluding the first transition from the idle state.

USB internal PHY differential data timing



Clock timing

Clock AC characteristics are measured with 10pF.

The next timing diagrams pertain to clock timing.

USB crystal/external oscillator timing

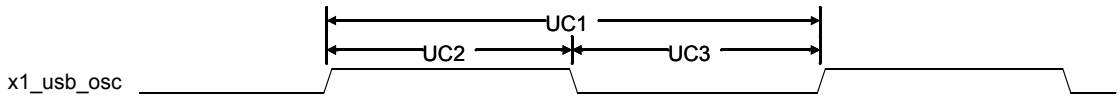
Table 37 describes the values shown in the USB crystal/external oscillator timing diagram.

Parameter	Description	Min	Max	Unit	Notes
UC1	x1_usb_osc cycle time	20.831	20.835	ns	1
UC2	x1_usb_osc high time	(UC1/2) x 0.4	(UC1/2) x 0.6	ns	
UC3	x1_usb_osc low time	(UC1/2) x 0.4	(UC1/2) X 0.6	ns	

Table 37: USB crystal/external oscillator timing parameters

Note:

1 If using a crystal, the tolerance must be ±100 ppm or better.



LCD input clock

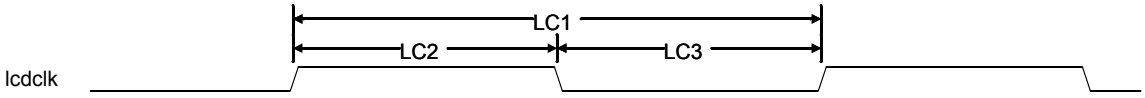
Table 38 describes the values shown for the LCD input clock timing diagram.

Parameter	Description	Min	Max	Unit	Notes
LC1	lcdclk cycle time	11.11		ns	1
LC2	lcdclk high time	(LC1/2) x 0.4	(LC1/2) x 0.6	ns	
LC3	lcdclk low time	(LC1/2) x 0.4	(LC1/2) x 0.6	ns	

Table 38: LCD input clock timing parameters

Note:

1 The clock rate supplied on lcdclk is twice the actual LCD clock rate.



Packaging

The next figures show the top view/dimensions and side and bottom view/dimensions of the NS9360.

The recommended pad size for this package configuration is 0.60 mm.

Top view