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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9, ARM® Cortex®-M4
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	200MHz, 800MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1), USB 2.0 OTG + PHY (2)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.15V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	A-HAB, ARM TZ, CAAM, CSU, SNVS, System JTAG, TVDECODE
Package / Case	400-LFBGA
Supplier Device Package	400-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6x1cvo08abr

- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

NOTE

The actual feature set depends on the part numbers as described in Table 1. Functions, such as display and camera interfaces, connectivity interfaces, video hardware acceleration, and 2D and 3D hardware graphics acceleration may not be enabled for specific part numbers.

3 Modules List

The i.MX 6SoloX processors contain a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX 6SoloX Modules List

Block Mnemonic	Block Name	Subsystem	Brief Description
ADC1 ADC2	Analog to Digital Converter	—	The ADC is a 12-bit general purpose analog to digital converter.
ARM	ARM Platform	ARM	The ARM Core Platform includes 1x Cortex-A9 and 1x Cortex-M4 cores. It also includes associated sub-blocks, such as the Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, watchdog, and CoreSight debug modules.
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
BCH	Binary-BCH ECC Processor	System Control Peripherals	The BCH module provides up to 62-bit ECC for NAND Flash controller (GPMI).
CAAM	Cryptographic accelerator and assurance module	Security	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, and a Pseudo Random Number Generator (PRNG). The pseudo random number generator is certified by Cryptographic Algorithm Validation Program (CAVP) of National Institute of Standards and Technology (NIST). Its DRBG validation number is 94 and its SHS validation number is 1455. CAAM also implements a Secure Memory mechanism. In i.MX 6SoloX processors, the security memory provided is 32 KB.
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.

Table 2. i.MX 6SoloX Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
PXP	PiXel Processing Pipeline	Display Peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP is enhanced with features specifically for gray scale applications.
QSPI	Quad Serial Peripheral Interface	Connectivity Peripherals	The Quad Serial Peripheral Interface (QuadSPI) block acts as an interface to one or two external serial flash devices, each with up to four bidirectional data lines.
ROM 96KB	Boot ROM	Internal Memory	Supports secure and regular boot modes
RDC	Resource Domain Controller	Multicore Isolation/Sharing	RDC module supports domain-based access control to shared resources.
SEMA4	Semaphore	Multicore/Isolation/ Sharing	Supports hardware-enforced semaphores.
SEMA42	Semaphore	Multicore/Isolation/ Sharing	SEMA42 is similar to SEMA4 with the following key differences: SEMA42 increases the number of access domains from 2 to 15 SEMA42 does not have interrupt to indicate semaphore release RDC programming model supports the option to require hardware semaphore for peripherals shared between domains. Signaling between the SEMA42 and RDC binds peripherals to semaphore gates within SEMA42.
SAI1 SAI2	—	—	The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.

Table 2. i.MX 6SoloX Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SSI1 SSI2 SSI3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface, which is used on the AP to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock / frame sync options. The SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream that reduces CPU overhead in use cases where two time slots are being used simultaneously.
TEMPMON	Temperature Monitor	System Control Peripherals	The Temperature sensor IP is used for detecting die temperature. The temperature read out does not reflect case or ambient temperature. It reflects the temperature in proximity of the sensor location on the die. Temperature distribution may not be uniformly distributed, therefore the read out value may not be the reflection of the temperature value of the entire die.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART1 UART2 UART3 UART4 UART5 UART6	UART Interface	Connectivity Peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 5 Mbps. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • Option to operate as 8-pins full UART, DCE, or DTE • UART1/6 support 8-pin, UART2/3/4/5 support 4-pin

Table 2. i.MX 6SoloX Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC1 uSDHC2 uSDHC3 uSDHC4	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX 6SoloX specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.5/4.2/4.3/4.4/4.41/ including high-capacity (size > 2 GB) cards HC MMC. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v3.0. • Conforms to the SD Host Controller Standard Specification version 3.0. All four ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) • All ports can work with 1.8 V and 3.3 V cards. Each port is placed on a separate power domain.
USB	Universal Serial Bus 2.0	Connectivity Peripherals	USBOH3 contains: • Two high-speed OTG 2.0 modules with integrated HS USB PHYs • One high-speed Host module connected to HSIC USB port
WDOG1 WDOG3	Watch Dog	Timer Peripherals	The Watch Dog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG2 (TZ)	Watch Dog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode software.
XTALOSC	Crystal Oscillator Interface	Clocks, Resets, and Power Control	The XTALOSC module connects to an external crystal to provide system clocks.

4.4 PLL Electrical Characteristics

4.4.1 Audio/Video PLL Electrical Parameters

Table 17. Audio/Video PLL Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.2 528 MHz PLL

Table 18. 528 MHz PLL Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.3 Ethernet PLL

Table 19. Ethernet PLL Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.4 480 MHz PLL

Table 20. 480 MHz PLL Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<383 reference cycles

Table 22. OSC32K Main Characteristics

Characteristics	Min	Typ	Max	Comments
Fosc	—	32.768 KHz	—	This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.
Current consumption	—	4 µA	—	The 4 µA is the consumption of the oscillator alone (OSC32K). Total supply consumption will depend on what the digital portion of the RTC consumes. The ring oscillator consumes 1 µA when ring oscillator is inactive, 20 µA when the ring oscillator is running. Another 1.5 µA is drawn from VDD_SNVS_IN in the power_detect block. So, the total current is 6.5 µA on VDD_SNVS_IN when the ring oscillator is not running.
Bias resistor	—	14 MΩ	—	This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Crystal Properties				
Cload	—	10 pF	—	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR	—	50 kΩ	100 kΩ	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3 modes
- LVDS I/O

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output.

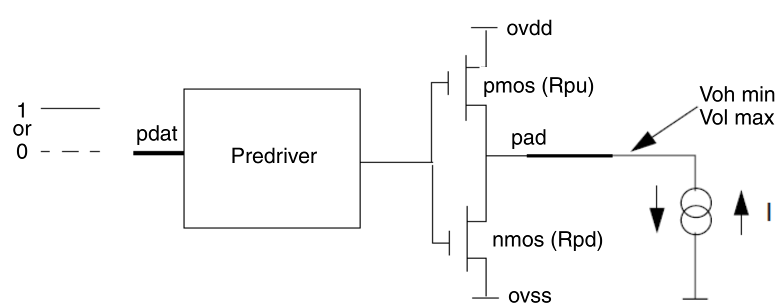

Figure 3. Circuit for Parameters Voh and Vol for I/O Cells

4.9.3.3 Examples of EIM Synchronous Accesses

Table 43. EIM Bus Timing Parameters [1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	EIM_BCLK Cycle time[2]	t	—	2 x t	—	3 x t	—	4 x t	—
WE2	EIM_BCLK Low Level Width	0.4 x t	—	0.8 x t	—	1.2 x t	—	1.6 x t	—
WE3	EIM_BCLK High Level Width	0.4 x t	—	0.8 x t	—	1.2 x t	—	1.6 x t	—
WE4	Clock rise to address valid[3]	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE5	Clock rise to address invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE6	Clock rise to EIM_CSx_B valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE7	Clock rise to EIM_CSx_B invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE8	Clock rise to EIM_WE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE9	Clock rise to EIM_WE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE10	Clock rise to EIM_OE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE11	Clock rise to EIM_OE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE12	Clock rise to EIM_EBx_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE13	Clock rise to EIM_EBx_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE14	Clock rise to EIM_LBA_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE15	Clock rise to EIM_LBA_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE16	Clock rise to Output Data Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE17	Clock rise to Output Data Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE18	Input Data setup time to Clock rise	2	—	4	—	—	—	—	—
WE19	Input Data hold time from Clock rise	2	—	2	—	—	—	—	—
WE20	EIM_WAIT_B setup time to Clock rise	2	—	4	—	—	—	—	—
WE21	EIM_WAIT_B hold time from Clock rise	2	—	2	—	—	—	—	—

Table 48. Samsung Toggle Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF28	Data write setup	tDS[6]	0.25 × tCK - 0.32	—	ns
NF29	Data write hold	tDH[6]	0.25 × tCK - 0.79	—	ns
NF30	NAND_DQS/NAND_DQ read setup skew	tDQSQ[7]	—	3.18	—
NF31	NAND_DQS/NAND_DQ read hold skew	tQHS[7]	—	3.27	—

[1] The GPMI toggle mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

[2] AS minimum value can be 0, while DS/DH minimum value is 1.

[3] T = tCK (GPMI clock period) -0.075ns (half of maximum p-p jitter).

[4] CE_DELAY represents HW_GPMI_TIMING2[CE_DELAY]. NF18 is guaranteed by the design. Read/Write operation is started with enough time of ALE/CLE assertion to low level.

[5] PRE_DELAY+1) ≥ (AS+DS)

[6] Shown in Figure 31.

[7] Shown in Figure 32.

For DDR Toggle mode, Figure 30 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 1.4 ns (max) and 1.4 ns (max) for tQHS at 133 MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of an delayed NAND_DQS signal, which is provided by an internal DPLL. The delay value of this register can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the *i.MX 6SoloX Applications Processor Reference Manual* (IMX6SXRM)). Generally, the typical delay value is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.12 External Peripheral Interface Parameters

The following subsections provide information on external peripheral interfaces.

4.12.1 AUDMUX Timing Parameters

The AUDMUX provides a programmable interconnect logic for voice, audio, and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI module. For more information, see the respective SSI electrical specifications found within this document.

4.12.2 CMOS Sensor Interface (CSI) Timing Parameters

The CSI enables the chip to connect directly to external CMOS image sensors, which are classified as dumb or smart as follows:

- Dumb sensors only support traditional sensor timing (vertical sync (VSYNC) and horizontal sync (HSYNC)) and output-only Bayer and statistics data.

Table 53. Enhanced Serial Audio Interface (ESAI) Timing (continued)

No.	Characteristics[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
81	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) low[5]	— —	— —	— —	22.0 12.0	x ck i ck	ns
82	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	ESAI_TX_CLK rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
86	ESAI_TX_CLK rising edge to data out valid	— —	— —	— —	18.0 13.0	x ck i ck	ns
87	ESAI_TX_CLK rising edge to data out high impedance [67]	— —	— —	— —	21.0 16.0	x ck i ck	ns
89	ESAI_TX_FS input (bl, wr) setup time before ESAI_TX_CLK falling edge[5]	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	ESAI_TX_FS input (wl) setup time before ESAI_TX_CLK falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	ESAI_TX_FS input hold time after ESAI_TX_CLK falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns
95	ESAI_RX_HF_CLK/ESAI_TX_HF_CLK clock cycle	—	2 x T_C	15	—	—	ns
96	ESAI_TX_HF_CLK input rising edge to ESAI_TX_CLK output	—	—	—	18.0	—	ns
97	ESAI_RX_HF_CLK input rising edge to ESAI_RX_CLK output	—	—	—	18.0	—	ns

1 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are the same clock)

2 bl = bit length
wl = word length
wr = word length relative

3 ESAI_TX_CLK(SCKT pin) = transmit clock
ESAI_RX_CLK(SCKR pin) = receive clock
ESAI_TX_FS(FST pin) = transmit frame sync
ESAI_RX_FS(FSR pin) = receive frame sync
ESAI_TX_HF_CLK(HCKT pin) = transmit high frequency clock
ESAI_RX_HF_CLK(HCKR pin) = receive high frequency clock

4 For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

5 The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.

6 Periodically sampled and not 100% tested.

Figure 48 shows RMII mode timings. Table 62 describes the timing parameters (M16–M21) shown in the figure.

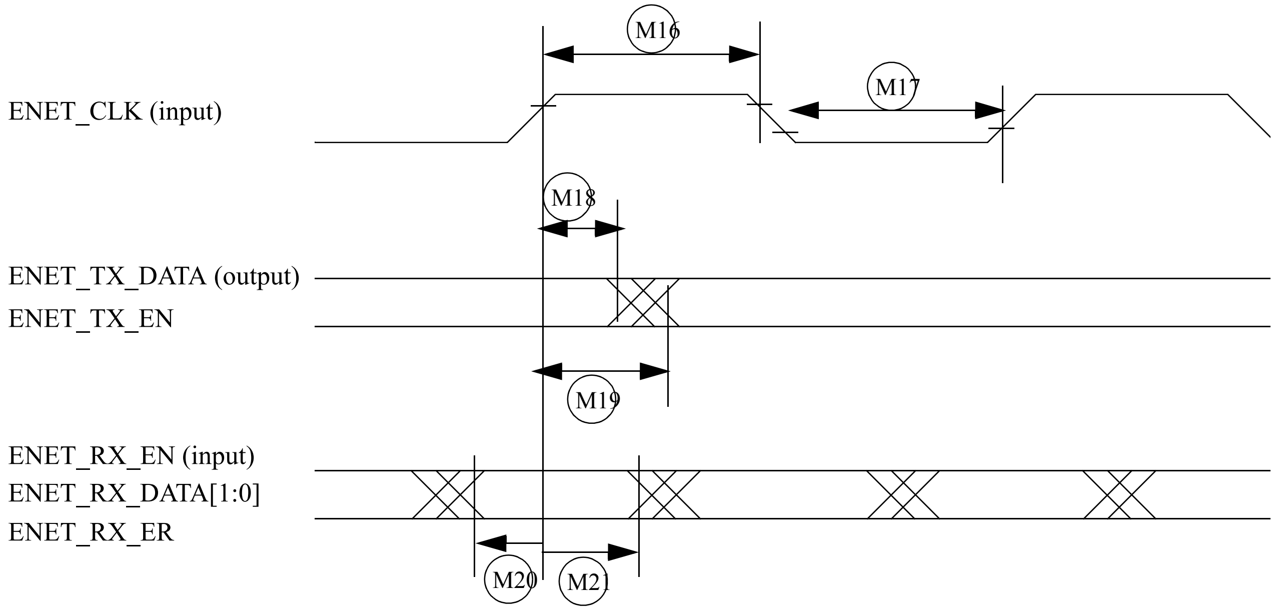

Figure 48. RMII Mode Signal Timing Diagram

Table 62. RMII Signal Timing

ID	Characteristic	Min	Max	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA invalid	4	—	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA valid	—	13	ns
M20	ENET_RX_DATAD[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	2	—	ns
M21	ENET_CLK to ENET_RX_DATAD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

4.12.6.3 Signal Switching Specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 63. RGMII Signal Switching Specifications [1]

Symbol	Description	Min	Max	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-500	500	ps

Table 80. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDxRXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDxRXC clock high period	36.0	—	ns
SS4	AUDx_TXC/AUDxRXC clock low period	36.0	—	ns
SS6	AUDx_TXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS8	AUDx_TXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS10	AUDx_TXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS12	AUDx_TXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS14	AUDx_TXC/AUDxRXC Internal AUDx_TXFS rise time	—	6.0	ns
SS15	AUDx_TXC/AUDxRXC Internal AUDx_TXFS fall time	—	6.0	ns
SS16	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS17	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS18	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns
Synchronous Internal Clock Operation				
SS42	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS43	AUDx_RXD hold after AUDx_TXC falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

Table 89. USB HSIC Receive Parameters[1] (continued)

Name	Parameter	Min	Max	Unit	Comment
Tsetup	data setup time	365	—	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

1 The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

4.12.20 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in revision 2.0 of the *USB On-The-Go and Embedded Host Supplement to the USB 2.0 Specification* with the amendments below (*On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification* is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ECN June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010
  - Portable device only

4.13 A/D Converter

4.13.1 12-bit ADC Electrical Characteristics

4.13.1.1 12-bit ADC Operating Conditions

Table 90. 12-bit ADC Operating Conditions

Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	VDDA_ADC_3P3	3.0	-	3.6	V	—
	Delta to VDD (VDD-VDDA_ADC_3P3)[2]	VDDA_ADC_3P3	-100	0	100	mV	—
Ground voltage	Delta to VSS (VSS-VSSAD)	ΔVSSAD	-100	0	100	mV	—
Ref Voltage High	—	V_{REFH}	1.13	VDDA_ADC_3P3	VDDA_ADC_3P3	V	—
Ref Voltage Low	—	V_{REFL}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V	—
Input Voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
Input Capacitance	8/10/12 bit modes	C_{ADIN}	—	1.5	2	pF	—
Input Resistance	ADLPC=0, ADHSC=1	R_{ADIN}	—	5	7	kohms	—
	ADLPC=0, ADHSC=0		—	12.5	15	kohms	—
	ADLPC=1, ADHSC=0		—	25	30	kohms	—
Analog Source Resistance	12 bit mode f_{ADCK} = 40MHz ADLSMP=0, ADSTS=10, ADHSC=1	R_{AS}	—	—	1	kohms	T_{samp}=150ns
R_{AS} depends on Sample Time Setting (ADLSMP, ADSTS) and ADC Power Mode (ADHSC, ADLPC). See charts for Minimum Sample Time versus R_{AS}							
ADC Conversion Clock Frequency	ADLPC=0, ADHSC=1 12 bit mode	f_{ADCK}	4	—	40	MHz	—
	ADLPC=0, ADHSC=0 12 bit mode		4	—	30	MHz	—
	ADLPC=1, ADHSC=0 12 bit mode		4	—	20	MHz	—

[1] Typical values assume VDDA_ADC_3P3= 3.0 V, Temp = 25°C, f_{ADCK}=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
[2] DC potential difference

Table 100. NAND Boot through GPMI

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG1[3:2]=01b	BOOT_CFG1[3:2]=10b
NAND_CLE	rawnand.CLE	Alt 0	Yes	—	—
NAND_ALE	rawnand.ALE	Alt 0	Yes	—	—
NAND_WP_B	rawnand.WP_B	Alt 0	Yes	—	—
NAND_READY_B	rawnand.READY_B	Alt 0	Yes	—	—
NAND_CE0_B	rawnand.CE0_B	Alt 0	Yes	—	—
NAND_CE1_B	rawnand.CE1_B	Alt 0	—	Yes	—
NAND_RE_B	rawnand.RE_B	Alt 0	Yes	—	—
NAND_WE_B	rawnand.WE_B	Alt 0	Yes	—	—
NAND_DATA00	rawnand.DATA00	Alt 0	Yes	—	—
NAND_DATA01	rawnand.DATA01	Alt 0	Yes	—	—
NAND_DATA02	rawnand.DATA02	Alt 0	Yes	—	—
NAND_DATA03	rawnand.DATA03	Alt 0	Yes	—	—
NAND_DATA04	rawnand.DATA04	Alt 0	Yes	—	—
NAND_DATA05	rawnand.DATA05	Alt 0	Yes	—	—
NAND_DATA06	rawnand.DATA06	Alt 0	Yes	—	—
NAND_DATA07	rawnand.DATA07	Alt 0	Yes	—	—
SD4_RESET_B	rawnand.DQS	Alt 1	Yes	—	—
SD4_DATA5	rawnand.CE2_B	Alt 1	—	—	Yes
SD4_DATA6	rawnand.CE3_B	Alt 1	—	—	Yes

Table 101. SD/MMC Boot through USDHC1

Ball Name	Signal Name	Mux Mode	Common	4-bit	8-bit	BOOT_CFG1[1]=1 (SD Power Cycle or SD boot with SDR50/SDR104)	SDMMC MFG Mode
GPIO1_IO02	usdhc1.CD_B	Alt 1	—	—	—	—	Yes
SD1_CLK	usdhc1.CLK	Alt 0	Yes	—	—	—	—
SD1_CMD	usdhc1.CMD	Alt 0	Yes	—	—	—	—
SD1_DATA0	usdhc1.DATA0	Alt 0	Yes	—	—	—	—
SD1_DATA1	usdhc1.DATA1	Alt 0	—	Yes	Yes	—	—
SD1_DATA2	usdhc1.DATA2	Alt 0	—	Yes	Yes	—	—
SD1_DATA3	usdhc1.DATA3	Alt 0	Yes	—	—	—	—
NAND_DATA00	usdhc1.DATA4	Alt 1	—	—	Yes	—	—
NAND_DATA01	usdhc1.DATA5	Alt 1	—	—	Yes	—	—

6.4.4 17x17 mm NP (No PCIe), 0.8 mm Pitch, 20x20 Ball Map

Table 114. 17x17 mm (No PCIe), 0.8 mm Pitch, 20x20 Ball Map

	A	B	C	D	E	F	G
1	VSS	DRAM_SDQS3_P	DRAM_DATA26	DRAM_DATA25	DRAM_DATA15	DRAM_DATA13	DRAM_SDQS1_P
2	DRAM_DATA24	DRAM_SDQS3_N	DRAM_DATA28	DRAM_DATA27	DRAM_DATA14	DRAM_DATA09	DRAM_DQM1
3	DRAM_DQM3	DRAM_DATA29	VSS	DRAM_CS1_B	VSS	VSS	DRAM_SDBA0
4	DRAM_DATA31	DRAM_DATA30	VSS	DRAM_RESET	DRAM_SDCKE1	DRAM_ADDR07	DRAM_ADDR05
5	ENET1_RX_CLK	ENET1_COL	DRAM_ZQPAD	ENET2_TX_CLK	ENET2_RX_CLK	VSS	DRAM_ADDR03
6	ENET1_MDIO	ENET1_MDC	ENET1_CRS	VSS	ENET2_CRS	NVCC_ENET	NVCC_DRAM
7	RGMII2_RD2	RGMII2_RD3	VDD_SOC_IN	RGMII1_RD2	ENET2_COL	ENET1_TX_CLK	VSS
8	RGMII2_RD0	RGMII2_RD1	VDD_SOC_IN	RGMII1_RD0	RGMII1_RD3	NVCC_RGMII1	VSS
9	RGMII2_RXC	RGMII2_RX_CTL	RGMII1_RD1	VSS	RGMII1_RXC	NVCC_RGMII2	VSS
10	RGMII2_TXC	RGMII2_TX_CTL	RGMII1_RX_CTL	RGMII1_TD3	RGMII1_TX_CTL	SD2_DATA2	VSS
11	RGMII2_TD0	RGMII2_TD1	RGMII1_TXC	RGMII1_TD0	RGMII1_TD2	SD2_DATA3	VSS
12	RGMII2_TD2	RGMII2_TD3	RGMII1_TD1	VSS	SD2_CLK	SD2_CMD	VSS
13	QSPI1A_DQS	QSPI1B_DQS	QSPI1B_DATA3	QSPI1B_DATA2	SD2_DATA0	NVCC_SD2	VSS
14	QSPI1B_DATA1	QSPI1B_DATA0	QSPI1B_SS0_B	QSPI1A_DATA2	SD2_DATA1	NVCC_QSPI	VSS
15	QSPI1B_SS1_B	QSPI1B_SCLK	QSPI1A_DATA1	VSS	QSPI1A_DATA0	NVCC_GPIO	NVCC_KEY
16	GPIO1_IO13	GPIO1_IO12	VDD_ARM_CAP	VDD_ARM_CAP	QSPI1A_DATA3	KEY_ROW0	LCD1_DATA23
17	GPIO1_IO07	GPIO1_IO08	QSPI1A_SS0_B	QSPI1A_SCLK	QSPI1A_SS1_B	VSS	LCD1_DATA21
18	GPIO1_IO04	GPIO1_IO05	VSS	GPIO1_IO06	KEY_ROW1	KEY_ROW2	KEY_COL2
19	GPIO1_IO09	GPIO1_IO10	GPIO1_IO00	GPIO1_IO01	KEY_COL4	KEY_ROW3	KEY_ROW4
20	VSS	GPIO1_IO11	GPIO1_IO02	GPIO1_IO03	KEY_COL3	KEY_COL1	KEY_COL0
	A	B	C	D	E	F	G

Table 116. 17x17 WP (with PCIe) Functional Contact Assignments (continued)

Ball Name	17x17 WP Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
LCD1_DATA21	G17	NVCC_LCD1	GPIO	ALT5	GPIO3_IO22	Input	Keeper
LCD1_DATA22	H19	NVCC_LCD1	GPIO	ALT5	GPIO3_IO23	Input	Keeper
LCD1_DATA23	G16	NVCC_LCD1	GPIO	ALT5	GPIO3_IO24	Input	Keeper
LCD1_ENABLE	J19	NVCC_LCD1	GPIO	ALT5	GPIO3_IO25	Input	Keeper
LCD1_HSYNC	J16	NVCC_LCD1	GPIO	ALT5	GPIO3_IO26	Input	Keeper
LCD1_RESET	J18	NVCC_LCD1	GPIO	ALT5	GPIO3_IO27	Input	Keeper
LCD1_VSYNC	J15	NVCC_LCD1	GPIO	ALT5	GPIO3_IO28	Input	Keeper
NAND_ALE	W6	NVCC_NAND	GPIO	ALT5	GPIO4_IO00	Input	Keeper
NAND_CE0_B	U7	NVCC_NAND	GPIO	ALT5	GPIO4_IO01	Input	Keeper
NAND_CE1_B	V9	NVCC_NAND	GPIO	ALT5	GPIO4_IO02	Input	Keeper
NAND_CLE	T8	NVCC_NAND	GPIO	ALT5	GPIO4_IO03	Input	Keeper
NAND_DATA00	V6	NVCC_NAND	GPIO	ALT5	GPIO4_IO04	Input	Keeper
NAND_DATA01	W8	NVCC_NAND	GPIO	ALT5	GPIO4_IO05	Input	Keeper
NAND_DATA02	Y7	NVCC_NAND	GPIO	ALT5	GPIO4_IO06	Input	Keeper
NAND_DATA03	U5	NVCC_NAND	GPIO	ALT5	GPIO4_IO07	Input	Keeper
NAND_DATA04	W7	NVCC_NAND	GPIO	ALT5	GPIO4_IO08	Input	Keeper
NAND_DATA05	T5	NVCC_NAND	GPIO	ALT5	GPIO4_IO09	Input	Keeper
NAND_DATA06	Y8	NVCC_NAND	GPIO	ALT5	GPIO4_IO10	Input	Keeper
NAND_DATA07	T6	NVCC_NAND	GPIO	ALT5	GPIO4_IO11	Input	Keeper
NAND_RE_B	U8	NVCC_NAND	GPIO	ALT5	GPIO4_IO12	Input	Keeper
NAND_READY_B	Y6	NVCC_NAND	GPIO	ALT5	GPIO4_IO13	Input	Keeper
NAND_WE_B	T7	NVCC_NAND	GPIO	ALT5	GPIO4_IO14	Input	Keeper
NAND_WP_B	V7	NVCC_NAND	GPIO	ALT5	GPIO4_IO15	Input	Keeper
ONOFF	N15	VDD_SNVS_IN	GPIO	—	ONOFF	Input	100 kΩ pull-up
PCIE_RX_N	P19	PCIE_VPH	—	—	PCIE_RX_N	—	—
PCIE_RX_P	P20	PCIE_VPH	—	—	PCIE_RX_P	—	—
PCIE_TX_N	R19	PCIE_VPH	—	—	PCIE_TX_N	—	—
PCIE_TX_P	R20	PCIE_VPH	—	—	PCIE_TX_P	—	—
POR_B	P14	VDD_SNVS_IN	GPIO	—	POR_B	Input	100 kΩ pull-up
QSPI1A_DATA0	E15	NVCC_QSPI	GPIO	ALT5	GPIO4_IO16	Input	Keeper

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M—1994.

3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.

4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: MAPBGA, THIN PROFILE, 14 X 14 X 1.165 PKG, 0.65 MM PITCH, 400 I/O	DOCUMENT NO: 98ASA00783D	REV: A
	STANDARD: NON—JEDEC	
	SOT1559—1	17 FEB 2016

Figure 88. 14x14 mm BGA Package Notes

Table 119. 14 x 14 Functional Contact Assignments (continued)

Ball Name	14x14 Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
DRAM_SDQS3_P	B2	NVCC_DRAM	DDRCLK	—	DRAM_SDQS3_P	Input	—
DRAM_SDWE_B	M1	NVCC_DRAM	DDR	—	DRAM_SDWE_B	Output	100 kΩ pull-up
ENET1_COL	B5	NVCC_ENET	GPIO	ALT5	GPIO2_IO00	Input	Keeper
ENET1_CRS	C6	NVCC_ENET	GPIO	ALT5	GPIO2_IO01	Input	Keeper
ENET1_MDC	B6	NVCC_ENET	GPIO	ALT5	GPIO2_IO02	Input	Keeper
ENET1_MDIO	A6	NVCC_ENET	GPIO	ALT5	GPIO2_IO03	Input	Keeper
ENET1_RX_CLK	A5	NVCC_ENET	GPIO	ALT5	GPIO2_IO04	Input	Keeper
ENET1_TX_CLK	F7	NVCC_ENET	GPIO	ALT5	GPIO2_IO05	Input	Keeper
ENET2_COL	E7	NVCC_ENET	GPIO	ALT5	GPIO2_IO06	Input	Keeper
ENET2_CRS	E6	NVCC_ENET	GPIO	ALT5	GPIO2_IO07	Input	Keeper
ENET2_RX_CLK	E5	NVCC_ENET	GPIO	ALT5	GPIO2_IO08	Input	Keeper
ENET2_TX_CLK	D5	NVCC_ENET	GPIO	ALT5	GPIO2_IO09	Input	Keeper
GPIO1_IO00	B20	NVCC_GPIO	GPIO	ALT5	GPIO1_IO00	Input	Keeper
GPIO1_IO01	D19	NVCC_GPIO	GPIO	ALT5	GPIO1_IO01	Input	Keeper
GPIO1_IO02	C19	NVCC_GPIO	GPIO	ALT5	GPIO1_IO02	Input	Keeper
GPIO1_IO03	D20	NVCC_GPIO	GPIO	ALT5	GPIO1_IO03	Input	Keeper
GPIO1_IO04	E16	NVCC_GPIO	GPIO	ALT5	GPIO1_IO04	Input	Keeper
GPIO1_IO05	B18	NVCC_GPIO	GPIO	ALT5	GPIO1_IO05	Input	Keeper
GPIO1_IO06	D18	NVCC_GPIO	GPIO	ALT5	GPIO1_IO06	Input	Keeper
GPIO1_IO07	A17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO07	Input	Keeper
GPIO1_IO08	E17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO08	Input	Keeper
GPIO1_IO09	A19	NVCC_GPIO	GPIO	ALT5	GPIO1_IO09	Input	Keeper
GPIO1_IO10	B19	NVCC_GPIO	GPIO	ALT5	GPIO1_IO10	Input	Keeper
GPIO1_IO11	C20	NVCC_GPIO	GPIO	ALT5	GPIO1_IO11	Input	Keeper
GPIO1_IO12	D17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO12	Input	Keeper
GPIO1_IO13	A16	NVCC_GPIO	GPIO	ALT5	GPIO1_IO13	Input	Keeper
JTAG_MOD	R8	NVCC_JTAG	GPIO	—	JTAG_MOD	Input	100 kΩ pull-up
JTAG_TCK	R9	NVCC_JTAG	GPIO	—	JTAG_TCK	Input	47 kΩ pull-up
JTAG_TDI	R10	NVCC_JTAG	GPIO	—	JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	Y9	NVCC_JTAG	GPIO	—	JTAG_TDO	Output	Keeper
JTAG_TMS	W9	NVCC_JTAG	GPIO	—	JTAG_TMS	Input	47 kΩ pull-up

Table 119. 14 x 14 Functional Contact Assignments (continued)

Ball Name	14x14 Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
RGMII2_TD1	C12	NVCC_RGMII2	GPIO	ALT5	GPIO5_IO19	Input	Keeper
RGMII2_TD2	B10	NVCC_RGMII2	GPIO	ALT5	GPIO5_IO20	Input	Keeper
RGMII2_TD3	B12	NVCC_RGMII2	GPIO	ALT5	GPIO5_IO21	Input	Keeper
RGMII2_TX_CTL	C9	NVCC_RGMII2	GPIO	ALT5	GPIO5_IO22	Input	Keeper
RGMII2_TXC	B11	NVCC_RGMII2	GPIO	ALT5	GPIO5_IO23	Input	Keeper
RTC_XTALI	Y17	VDD_SNVS_CAP	—	—	RTC_XTALI	—	—
RTC_XTALO	W17	VDD_SNVS_CAP	—	—	RTC_XTALO	—	—
SD2_CLK	E12	NVCC_SD1_SD2	GPIO	ALT5	GPIO6_IO06	Input	Keeper
SD2_CMD	F12	NVCC_SD1_SD2	GPIO	ALT5	GPIO6_IO07	Input	Keeper
SD2_DATA0	E13	NVCC_SD1_SD2	GPIO	ALT5	GPIO6_IO08	Input	Keeper
SD2_DATA1	E14	NVCC_SD1_SD2	GPIO	ALT5	GPIO6_IO09	Input	Keeper
SD2_DATA2	F10	NVCC_SD1_SD2	GPIO	ALT5	GPIO6_IO10	Input	Keeper
SD2_DATA3	F11	NVCC_SD1_SD2	GPIO	ALT5	GPIO6_IO11	Input	Keeper
SD3_CLK	V11	NVCC_LOW NVCC_HIGH	GPIO	ALT5	GPIO7_IO00	Input	100 kΩ pull-down
SD3_CMD	T13	NVCC_LOW NVCC_HIGH	GPIO	ALT5	GPIO7_IO01	Input	100 kΩ pull-down
SD3_DATA0	R11	NVCC_LOW NVCC_HIGH	GPIO	ALT5	GPIO7_IO02	Input	100 kΩ pull-down
SD3_DATA1	T11	NVCC_LOW NVCC_HIGH	GPIO	ALT5	GPIO7_IO03	Input	100 kΩ pull-down
SD3_DATA2	Y14	NVCC_LOW NVCC_HIGH	GPIO	ALT5	GPIO7_IO04	Input	100 kΩ pull-down
SD3_DATA3	T14	NVCC_LOW NVCC_HIGH	GPIO	ALT5	GPIO7_IO05	Input	100 kΩ pull-down
SD3_DATA4	U14	NVCC_LOW NVCC_HIGH	GPIO	ALT5	GPIO7_IO06	Input	100 kΩ pull-down
SD3_DATA5	U13	NVCC_LOW NVCC_HIGH	GPIO	ALT5	GPIO7_IO07	Input	100 kΩ pull-down
SD3_DATA6	V12	NVCC_LOW NVCC_HIGH	GPIO	ALT5	GPIO7_IO08	Input	100 kΩ pull-down
SD3_DATA7	U11	NVCC_LOW NVCC_HIGH	GPIO	ALT5	GPIO7_IO09	Input	100 kΩ pull-down
SD4_CLK	T10	NVCC_SD4	GPIO	ALT5	GPIO6_IO12	Input	Keeper
SD4_CMD	W12	NVCC_SD4	GPIO	ALT5	GPIO6_IO13	Input	Keeper