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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-A9, ARM® Cortex®-M4 |
| Number of Cores/Bus Width | 2 Core, 32-Bit |
| Speed | 200MHz, 800MHz |
| Co-Processors/DSP | Multimedia; NEON™ MPE |
| RAM Controllers | LPDDR2, LVDDR3, DDR3 |
| Graphics Acceleration | No |
| Display & Interface Controllers | Keypad, LCD |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | - |
| USB | USB 2.0 + PHY (1), USB 2.0 OTG + PHY (2) |
| Voltage - I/O | 1.8V, 2.5V, 2.8V, 3.15V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | A-HAB, ARM TZ, CAAM, CSU, SNVS, System JTAG, TVDECODE |
| Package / Case | 400-LFBGA |
| Supplier Device Package | 400-MAPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6x1cvo08ac |

## 1.2 Features

The i.MX 6SoloX processors are based on the ARM Cortex-A9 MPCore™ platform, which has the following features:

- Supports single ARM Cortex-A9 MPCore processor (with TrustZone)
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) coprocessor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 256 KB unified I/D L2 cache:
- Two Master AXI bus interfaces output of L2 cache
- Frequency of the core (including NEON coprocessor and L1 cache), as per Table 9, "Operating Ranges," on page 27.
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline
  - 32 double-precision VFPv3 floating point registers

The ARM Cortex-M4 platform:

- Cortex-M4 CPU core
- MPU (Memory Protection Unit)
- FPU (Floating Point Unit)
- 16 KByte Instruction Cache
- 16 KByte Data Cache
- 64 KByte TCM (Tightly-Coupled Memory)

The SoC-level memory system consists of the following additional components:

- Boot ROM, including HAB (96 KB)
- Internal multimedia / shared, fast access RAM (OCRAM, 128 KB)
- Internal RAM for state retention or general use (OCRAM_S, 16KB)
- Secure/non-secure RAM (32 KB)

**Table 2. i.MX 6SoloX Modules List (continued)**

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|---|---|---|---|
| ESAI | Enhanced Serial Audio Interface | Connectivity Peripherals | The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available. The ESAI has 12 pins for data and clocking connection to external devices. |
| FLEXCAN1 FLEXCAN2 | Flexible Controller Area Network | Connectivity Peripherals | The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames. |
| Fuse Box | Electrical Fuse Array | Security | Electrical Fuse Array. Enables setup of boot modes, security levels, security keys, and many other system parameters.The fuses are accessible through OCOTP_CTRL interface. |
| GC400T | Graphics Engine | Multimedia Peripherals | The GC400T is a graphics engine with separate 2D and 3D pipelines to provide both 2D and 3D acceleration. It supports DirectFB and GAL APIs. It supports OpenGL ES1.1/2.0 and OpenVG 1.1 APIs. |
| GIC | Global Interrupt Controller | ARM/Control | The Global Interrupt Controller (GIC) collects interrupt requests from all i.MX 6SoloX sources and routes them to the ARM MPCore(s). Each interrupt can be configured as a normal or a secure interrupt. Software Force Registers and software Priority Masking are also supported. This IP is part of the ARM Core complex. |
| GIS | General Interrupt Service module | Camera, Display, & Graphics | GIS can be used to automate the flow of data from the camera to the display. |

Table 38 shows DDR I/O output buffer impedance of i.MX 6SoloX processors.

**Table 38. DDR I/O Output Buffer Impedance**

| Parameter | Symbol | Test Conditions DSE (Drive Strength) | Typical | | Unit |
|---|---|---|---|---|---|
| | | | NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11 | NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10 | |
| Output Driver Impedance | Rdrv | 000<br>001<br>010<br>011<br>100<br>101<br>110<br>111 | Hi-Z<br>240<br>120<br>80<br>60<br>48<br>40<br>34 | Hi-Z<br>240<br>120<br>80<br>60<br>48<br>40<br>34 | Ω |

**Note:**
1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 Ω external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

### 4.8.4 USB HSIC I/O Output Buffer Impedance

Table 39 shows the USB HSIC I/O (USB_H_DATA and USB_H_STROBE) output buffer impedance.

**Table 39. USB HSIC I/O Output Buffer Impedance**

| Parameter | Symbol | Drive Strength (DSE) | Typical | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | NVCC_USB_H=1.2V DDR_SEL=10 | NVCC_USB_H=1.5V DDR_SEL=11 | NVCC_USB_H=1.8V DDR_SEL=11 | NVCC_USB_H=2.5V DDR_SEL=11 | |
| Output Driver Impedance | Rdrv | 000<br>001<br>010<br>011<br>100<br>101<br>110<br>111 | Hi-Z<br>240<br>120<br>80<br>60<br>48<br>40<br>34 | Hi-Z<br>240<br>120<br>80<br>60<br>48<br>40<br>34 | Hi-Z<br>247<br>113<br>73<br>55<br>43<br>36<br>30 | Hi-Z<br>287<br>121<br>76<br>57<br>45<br>37<br>31 | Ω |

### 4.8.5 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

## 4.9 System Modules Timing

This section contains the timing and electrical parameters for the modules in each i.MX 6SoloX processor.

### 4.9.1 Reset Timing Parameters

Figure 8 shows the reset timing and Table 40 lists the timing parameters.

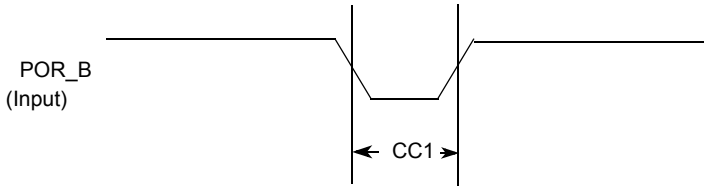



**Figure 8. Reset Timing Diagram**

**Table 40. Reset Timing Parameters**

| ID | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| CC1 | Duration of POR_B to be qualified as valid. | 1 | — | RTC_XTALI cycle |

### 4.9.2 WDOG Reset Timing Parameters

Figure 9 shows the WDOG reset timing and Table 41 lists the timing parameters.

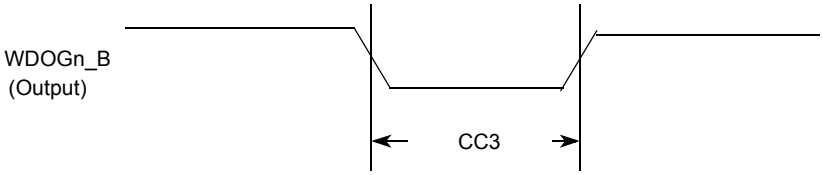



**Figure 9. WDOGn_B Timing Diagram**

**Table 41. WDOGn_B Timing Parameters**

| ID | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| CC3 | Duration of WDOGn_B Assertion | 1 | — | RTC_XTALI cycle |

**NOTE**

RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 µs.

**NOTE**

WDOG1_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

### 4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM. Maximum operating frequency for EIM data transfer is 104 MHz. Two system clocks are used with the EIM:

- ACLK_EIM_SLOW_CLK_ROOT is used to clock the EIM module.
  The maximum frequency for CLK_EIM_SLOW_CLK_ROOT is 132 MHz.

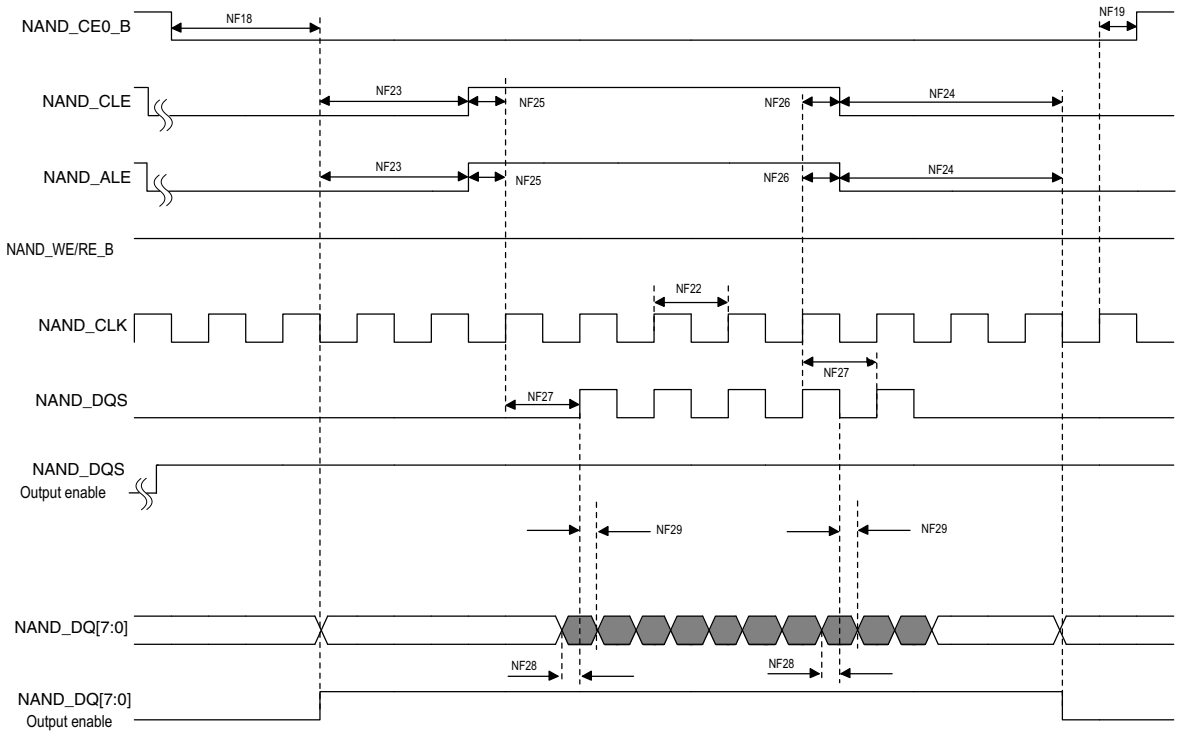



**Figure 28. Source Synchronous Mode Data Write Timing Diagram**

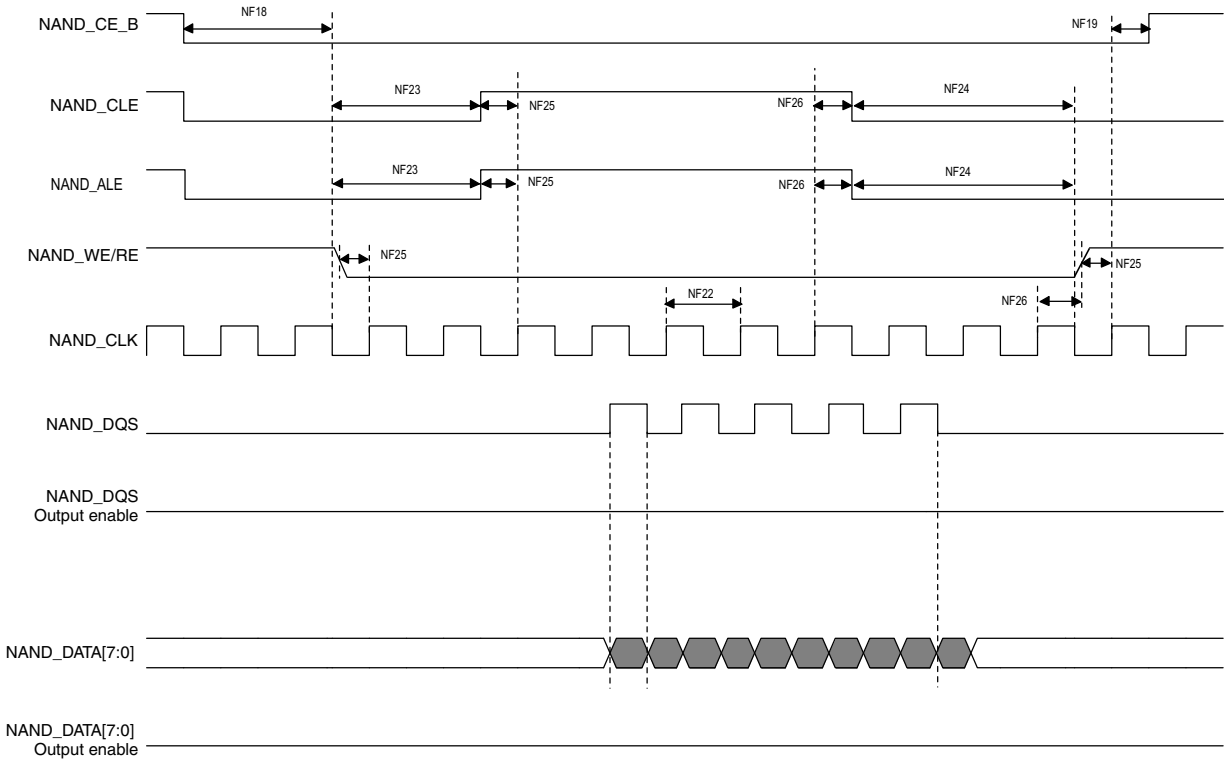



**Figure 29. Source Synchronous Mode Data Read Timing Diagram**

**Table 53. Enhanced Serial Audio Interface (ESAI) Timing (continued)**

| No. | Characteristics[1,2] | Symbol | Expression[2] | Min | Max | Condition[3] | Unit |
|---|---|---|---|---|---|---|---|
| 81 | ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) low[5] | —<br>— | —<br>— | —<br>— | 22.0<br>12.0 | x ck<br>i ck | ns |
| 82 | ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) high | —<br>— | —<br>— | —<br>— | 19.0<br>9.0 | x ck<br>i ck | ns |
| 83 | ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) low | —<br>— | —<br>— | —<br>— | 20.0<br>10.0 | x ck<br>i ck | ns |
| 84 | ESAI_TX_CLK rising edge to data out enable from high impedance | —<br>— | —<br>— | —<br>— | 22.0<br>17.0 | x ck<br>i ck | ns |
| 86 | ESAI_TX_CLK rising edge to data out valid | —<br>— | —<br>— | —<br>— | 18.0<br>13.0 | x ck<br>i ck | ns |
| 87 | ESAI_TX_CLK rising edge to data out high impedance [6][7] | —<br>— | —<br>— | —<br>— | 21.0<br>16.0 | x ck<br>i ck | ns |
| 89 | ESAI_TX_FS input (bl, wr) setup time before ESAI_TX_CLK falling edge[5] | —<br>— | —<br>— | 2.0<br>18.0 | —<br>— | x ck<br>i ck | ns |
| 90 | ESAI_TX_FS input (wl) setup time before ESAI_TX_CLK falling edge | —<br>— | —<br>— | 2.0<br>18.0 | —<br>— | x ck<br>i ck | ns |
| 91 | ESAI_TX_FS input hold time after ESAI_TX_CLK falling edge | —<br>— | —<br>— | 4.0<br>5.0 | —<br>— | x ck<br>i ck | ns |
| 95 | ESAI_RX_HF_CLK/ESAI_TX_HF_CLK clock cycle | — | $2 \times T_C$ | 15 | — | — | ns |
| 96 | ESAI_TX_HF_CLK input rising edge to ESAI_TX_CLK output | — | — | — | 18.0 | — | ns |
| 97 | ESAI_RX_HF_CLK input rising edge to ESAI_RX_CLK output | — | — | — | 18.0 | — | ns |

1 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are the same clock)

2 bl = bit length
wl = word length
wr = word length relative

3 ESAI_TX_CLK(SCKT pin) = transmit clock
ESAI_RX_CLK(SCKR pin) = receive clock
ESAI_TX_FS(FST pin) = transmit frame sync
ESAI_RX_FS(FSR pin) = receive frame sync
ESAI_TX_HF_CLK(HCKT pin) = transmit high frequency clock
ESAI_RX_HF_CLK(HCKR pin) = receive high frequency clock

4 For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

5 The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.

6 Periodically sampled and not 100% tested.

## 4.12.10 LVDS Display Bridge (LDB) Module Parameters

The LVDS interface complies with TIA/EIA 644-A standard. For more details, see TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits”.

**Table 67. LVDS Display Bridge (LDB) Electrical Specification**

| Parameter | Symbol | Test Condition | Min | Max | Units |
|---|---|---|---|---|---|
| Differential Voltage Output Voltage | $V_{OD}$ | 100 Ω Differential load | 250 | 450 | mV |
| Output Voltage High | Voh | 100 Ω differential load (0 V Diff—Output High Voltage static) | 1.25 | 1.6 | V |
| Output Voltage Low | Vol | 100 Ω differential load (0 V Diff—Output Low Voltage static) | 0.9 | 1.25 | V |
| Offset Static Voltage | $V_{OS}$ | Two 49.9 Ω resistors in series between N-P terminal, with output in either Zero or One state, the voltage measured between the 2 resistors. | 1.15 | 1.375 | V |
| VOS Differential | $V_{OSDIFF}$ | Difference in $V_{OS}$ between a One and a Zero state | -50 | 50 | mV |
| Output short circuited to GND | ISA ISB | With the output common shorted to GND | -24 | 24 | mA |
| VT Full Load Test | VTLoad | 100 Ω Differential load with a 3.74 kΩ load between GND and IO Supply Voltage | 247 | 454 | mV |

## 4.12.11 PCIe PHY Parameters

The PCIe interface complies with PCIe specification Gen2 x1 lane and supports the PCI Express 1.1/2.0 standard.

### 4.12.11.1 PCIE_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 200 Ω. 1% precision resistor on PCIE_REXT pads to ground. It is used for termination impedance calibration.

## 4.12.12 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMx_OUT) external pin.

Figure 54 depicts the timing of the PWM, and Table 68 lists the PWM timing parameters.

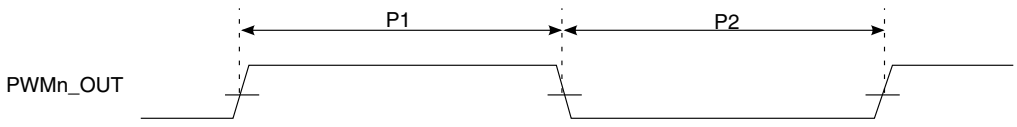



**Figure 54. PWM Timing**

**Table 70. QuadSPI Input/Read Timing (SDR mode with loopback DQS sampling)**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $T_{is}$ | Setup time for incoming data | 1 | — | ns |
| $T_{ih}$ | Hold time requirement for incoming data | 1 | — | ns |

## NOTE

- For internal sampling, the timing values assumes using sample point 0, that is QuadSPIx_SMPR[SDRSMP] = 0.
- For loopback DQS sampling, the data strobe is output to the DQS pad together with the serial clock. The data strobe is looped back from DQS pad and used to sample input data.

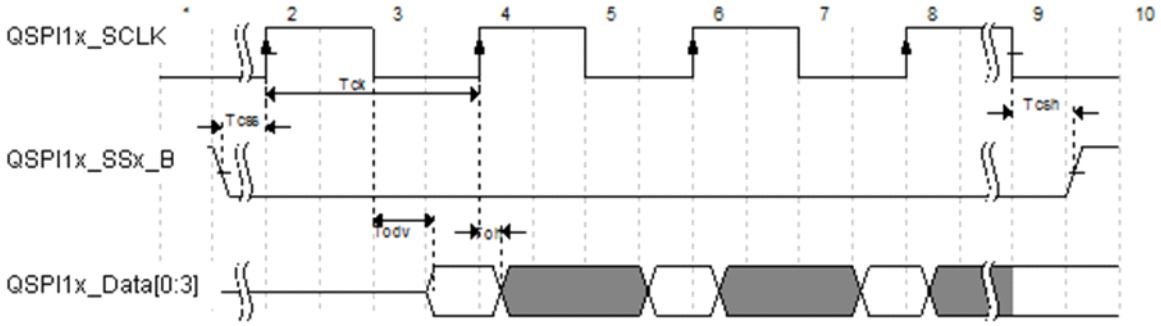



**Figure 57. QuadSPI Output/Write Timing (SDR mode)**

**Table 71. QuadSPI Output/Write Timing (SDR mode)**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $T_{ov}$ | Output Data Valid | — | 3.2 | ns |
| $T_{oh}$ | Output Data Hold | 0 | — | ns |
| $T_{ck}$ | SCK clock period | 12.5 | — | ns |
| $T_{css}$ | Chip select output setup time | 3 | — | SCK cycle(s) |
| $T_{csh}$ | Chip select output hold time | 3 | — | SCK cycle(s) |

## NOTE

Tcss and Tcsh are configured by the QuadSPIx_FLSHCR register, the default values of 3 are shown on the timing. Please refer to Reference Manual for further details.

### 4.12.13.2 DDR Mode

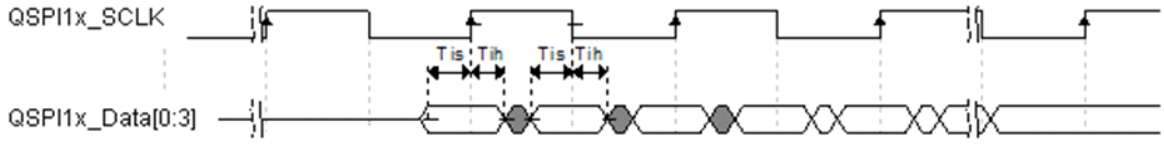



**Figure 58. QuadSPI Input/Read Timing (DDR mode with internal sampling)**

**Table 72. QuadSPI Input/Read Timing (DDR mode with internal sampling)**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $T_{is}$ | Setup time for incoming data | 8.67 | — | ns |
| $T_{ih}$ | Hold time requirement for incoming data | 0 | — | ns |

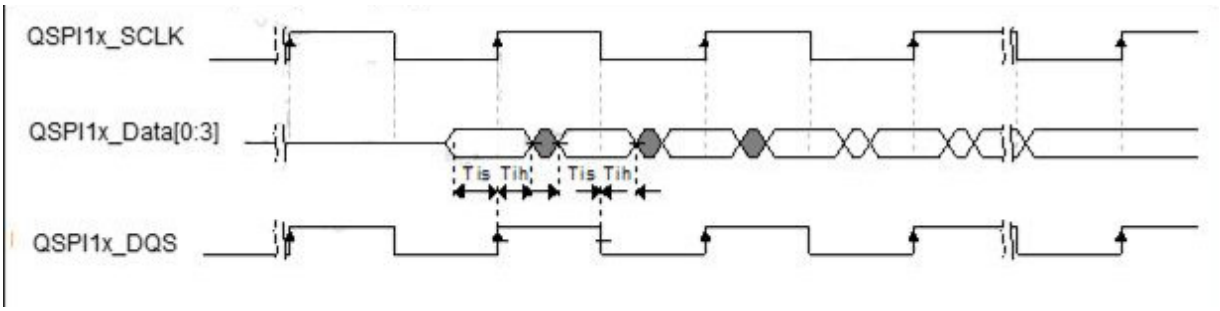



**Figure 59. QuadSPI Input/Read Timing (DDR mode with loopback DQS sampling)**

**Table 73. QuadSPI Input/Read Timing (DDR mode with loopback DQS sampling)**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $T_{is}$ | Setup time for incoming data | 1 | — | ns |
| $T_{ih}$ | Hold time requirement for incoming data | 1 | — | ns |

**NOTE**

- For internal sampling, the timing values assumes sample point 0, that is QuadSPIx_SMPR[DDRSMP] = 0.
- For loopback DQS sampling, the data strobe is output to the DQS pad together with the serial clock. The data strobe is looped back from the DQS pad and used to sample input data.

**Table 91. 12-bit ADC Characteristics ($V_{REFH}$ = VDDA_ADC_3P3, $V_{REFL}$ = $V_{SSAD}$) (continued)**

| Characteristic | Conditions[1] | Symbol | Min | Typ[2] | Max | Unit | Comment |
|---|---|---|---|---|---|---|---|
| [L:] Effective Number of Bits | 12 bit mode | ENOB | 10.1 | 10.7 | — | Bits | Fin = 100Hz |
| [L:] Signal to Noise plus Distortion | See ENOB | SINAD | SINAD = 6.02 x ENOB + 1.76 | | | dB | — |

1 All accuracy numbers assume the ADC is calibrated with $V_{REFH}$=VDDA_ADC_3P3

2 Typical values assume VDDA_ADC_3P3 = 3.0 V, Temp = 25°C, $F_{adck}$=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

**NOTE**

The ADC electrical spec is met with the calibration enabled configuration.

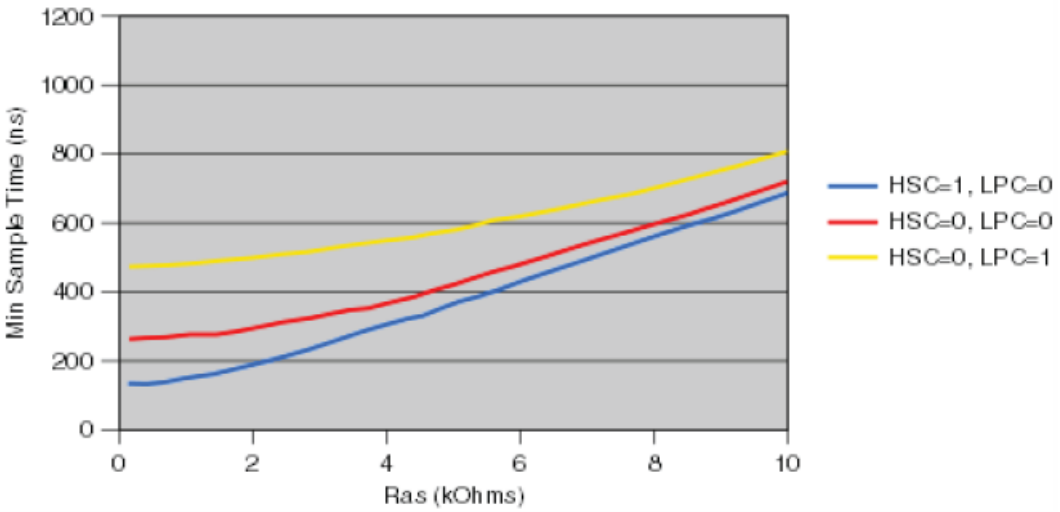



**Figure 80. Minimum Sample Time versus Ras (Cas = 2pF)**

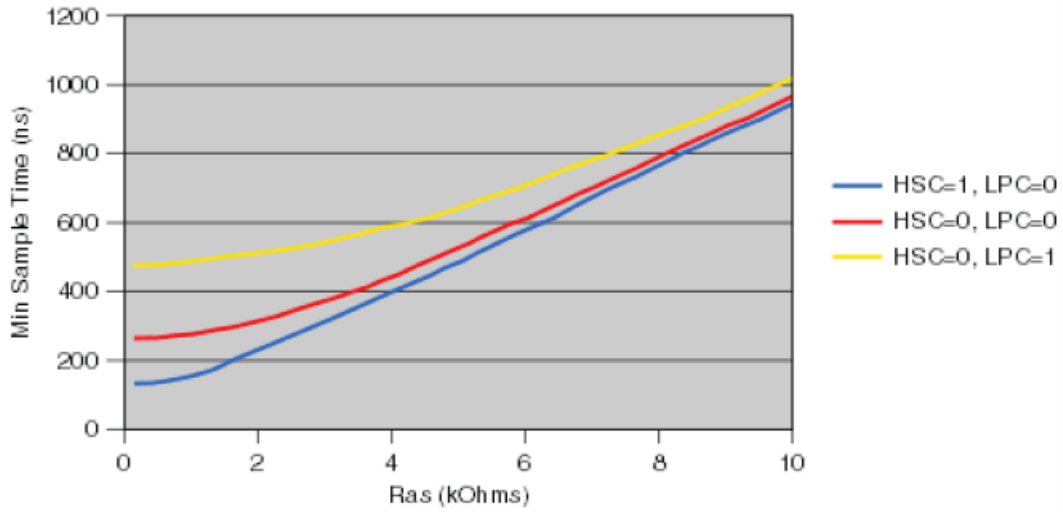
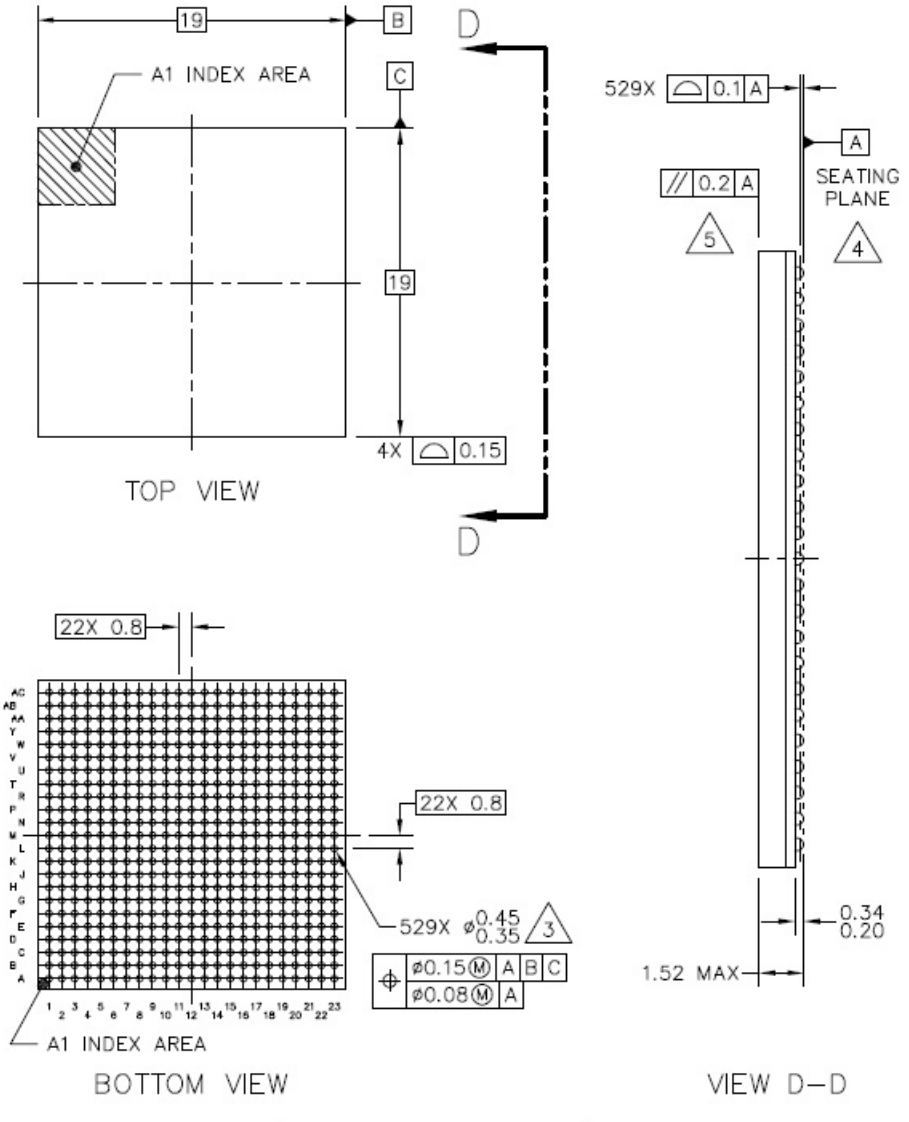



**Figure 81. Minimum Sample Time versus Ras (Cas = 5pF)**

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|---|---|---|
| TITLE: MAPBGA, 19 X 19 X 1.37 PKG, 0.8 MM PITCH, 529 I/O | DOCUMENT NO: 98ASA00646D | REV: B |
| | STANDARD: JEDEC MO–275 PPAC–1 | |
| | SOT1526–1 | 12 JAN 2016 |

**Figure 83. 19x19 mm BGA Package—Top, Bottom, and Side Views**

**Table 109. 19x19 mm Functional Contact Assignments (continued)**

| Ball Name | 19x19 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|---|---|---|---|---|---|---|---|
| | | | | Default Mode | Default Function | Input/ Output | Value |
| LCD1_DATA09 | H20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO10 | Input | Keeper |
| LCD1_DATA10 | H19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO11 | Input | Keeper |
| LCD1_DATA11 | H18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO12 | Input | Keeper |
| LCD1_DATA12 | G23 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO13 | Input | Keeper |
| LCD1_DATA13 | G22 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO14 | Input | Keeper |
| LCD1_DATA14 | G21 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO15 | Input | Keeper |
| LCD1_DATA15 | G19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO16 | Input | Keeper |
| LCD1_DATA16 | G18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO17 | Input | Keeper |
| LCD1_DATA17 | F23 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO18 | Input | Keeper |
| LCD1_DATA18 | F22 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO19 | Input | Keeper |
| LCD1_DATA19 | F21 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO20 | Input | Keeper |
| LCD1_DATA20 | G20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO21 | Input | Keeper |
| LCD1_DATA21 | F19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO22 | Input | Keeper |
| LCD1_DATA22 | F18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO23 | Input | Keeper |
| LCD1_DATA23 | E20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO24 | Input | Keeper |
| LCD1_ENABLE | E21 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO25 | Input | Keeper |
| LCD1_HSYNC | D23 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO26 | Input | Keeper |
| LCD1_RESET | E22 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO27 | Input | Keeper |
| LCD1_VSYNC | E23 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO28 | Input | Keeper |
| LVDS_CLK_N | T20 | NVCC_LVDS | LVDS | — | LVDS_CLK_N | — | — |
| LVDS_CLK_P | T21 | NVCC_LVDS | LVDS | ALT0 | LVDS_CLK_P | Input | — |
| LVDS_DATA0_N | V22 | NVCC_LVDS | LVDS | — | LVDS_DATA0_N | — | — |
| LVDS_DATA0_P | V23 | NVCC_LVDS | LVDS | ALT0 | LVDS_DATA0_P | Input | — |
| LVDS_DATA1_N | V20 | NVCC_LVDS | LVDS | — | LVDS_DATA1_N | — | — |
| LVDS_DATA1_P | V21 | NVCC_LVDS | LVDS | ALT0 | LVDS_DATA1_P | Input | — |
| LVDS_DATA2_N | U22 | NVCC_LVDS | LVDS | — | LVDS_DATA2_N | — | — |
| LVDS_DATA2_P | U23 | NVCC_LVDS | LVDS | ALT0 | LVDS_DATA2_P | Input | — |
| LVDS_DATA3_N | T22 | NVCC_LVDS | LVDS | — | LVDS_DATA3_N | — | — |
| LVDS_DATA3_P | T23 | NVCC_LVDS | LVDS | ALT0 | LVDS_DATA3_P | Input | — |
| NAND_ALE | AB7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO00 | Input | Keeper |
| NAND_CE0_B | AB8 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO01 | Input | Keeper |
| NAND_CE1_B | AC9 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO02 | Input | Keeper |
| NAND_CLE | AB9 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO03 | Input | Keeper |

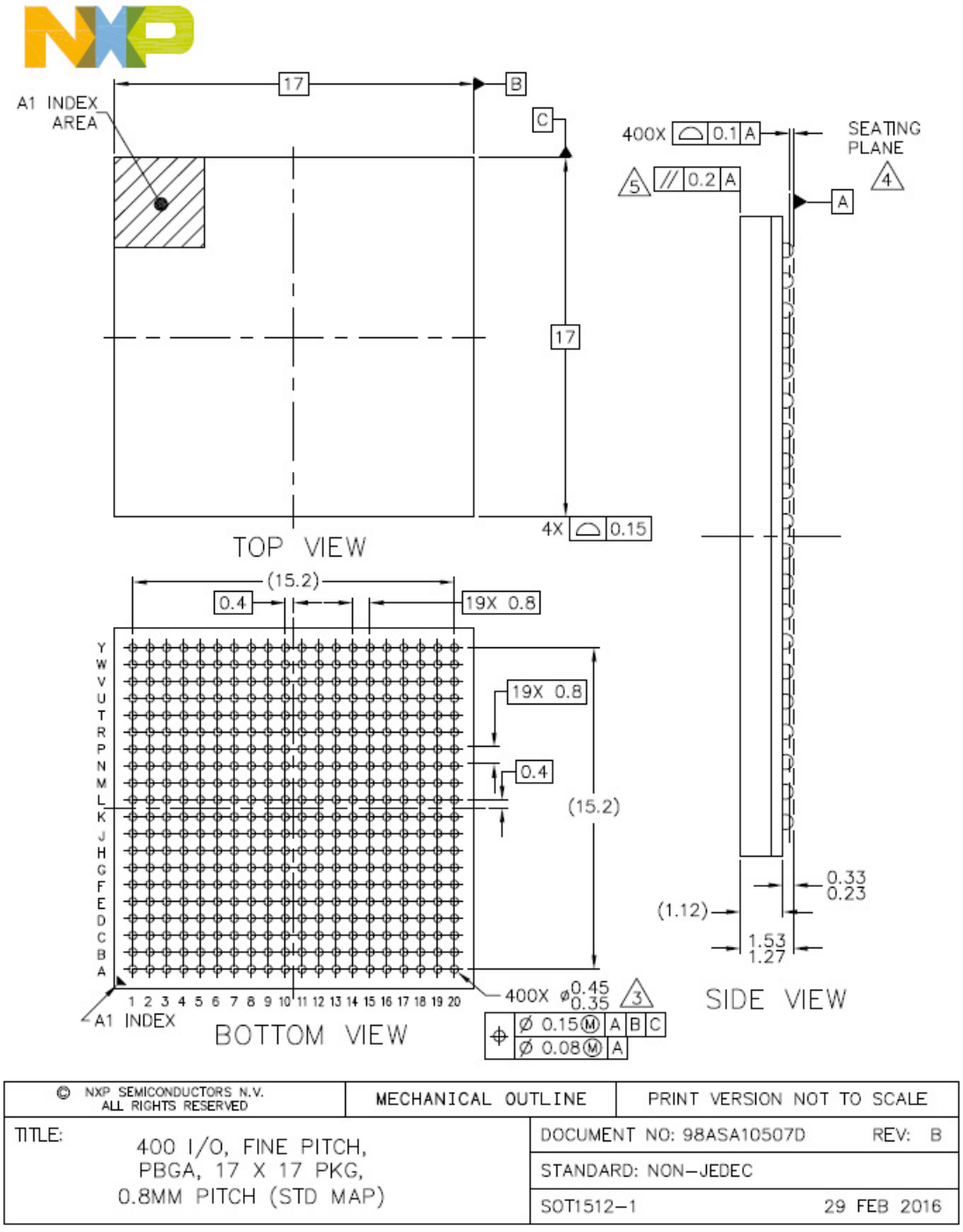


**Figure 85. 17x17 mm BGA Package—Top, Bottom, and Side Views**

**Table 113. 17x17 mm NP (No PCIe) Functional Contact Assignments (continued)**

| Ball Name | 17x17 NP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|---|---|---|---|---|---|---|---|
| | | | | Default Mode | Default Function | Input/ Output | Value |
| DRAM_ADDR11 | N4 | NVCC_DRAM | DDR | — | DRAM_ADDR11 | Output | 100 kΩ pull-up |
| DRAM_ADDR12 | P4 | NVCC_DRAM | DDR | — | DRAM_ADDR12 | Output | 100 kΩ pull-up |
| DRAM_ADDR13 | M4 | NVCC_DRAM | DDR | — | DRAM_ADDR13 | Output | 100 kΩ pull-up |
| DRAM_ADDR14 | R4 | NVCC_DRAM | DDR | — | DRAM_ADDR14 | Output | 100 kΩ pull-up |
| DRAM_CAS_B | J4 | NVCC_DRAM | DDR | — | DRAM_CAS_B | Output | 100 kΩ pull-up |
| DRAM_CS0_B | H4 | NVCC_DRAM | DDR | — | DRAM_CS0_B | Output | 100 kΩ pull-up |
| DRAM_CS1_B | D3 | NVCC_DRAM | DDR | — | DRAM_CS1_B | Output | 100 kΩ pull-up |
| DRAM_DATA00 | R1 | NVCC_DRAM | DDR | — | DRAM_DATA00 | Input | 100 kΩ pull-up |
| DRAM_DATA01 | T2 | NVCC_DRAM | DDR | — | DRAM_DATA01 | Input | 100 kΩ pull-up |
| DRAM_DATA02 | T1 | NVCC_DRAM | DDR | — | DRAM_DATA02 | Input | 100 kΩ pull-up |
| DRAM_DATA03 | R2 | NVCC_DRAM | DDR | — | DRAM_DATA03 | Input | 100 kΩ pull-up |
| DRAM_DATA04 | M1 | NVCC_DRAM | DDR | — | DRAM_DATA04 | Input | 100 kΩ pull-up |
| DRAM_DATA05 | M2 | NVCC_DRAM | DDR | — | DRAM_DATA05 | Input | 100 kΩ pull-up |
| DRAM_DATA06 | L2 | NVCC_DRAM | DDR | — | DRAM_DATA06 | Input | 100 kΩ pull-up |
| DRAM_DATA07 | N1 | NVCC_DRAM | DDR | — | DRAM_DATA07 | Input | 100 kΩ pull-up |
| DRAM_DATA08 | H1 | NVCC_DRAM | DDR | — | DRAM_DATA08 | Input | 100 kΩ pull-up |
| DRAM_DATA09 | F2 | NVCC_DRAM | DDR | — | DRAM_DATA09 | Input | 100 kΩ pull-up |
| DRAM_DATA10 | K2 | NVCC_DRAM | DDR | — | DRAM_DATA10 | Input | 100 kΩ pull-up |
| DRAM_DATA11 | J2 | NVCC_DRAM | DDR | — | DRAM_DATA11 | Input | 100 kΩ pull-up |

**Table 113. 17x17 mm NP (No PCIe) Functional Contact Assignments (continued)**

| Ball Name | 17x17 NP Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|---|---|---|---|---|---|---|---|
| | | | | Default Mode | Default Function | Input/ Output | Value |
| JTAG_TDO | R8 | NVCC_JTAG | GPIO | — | JTAG_TDO | Output | Keeper |
| JTAG_TMS | T10 | NVCC_JTAG | GPIO | — | JTAG_TMS | Input | 47 kΩ pull-up |
| JTAG_TRST_B | T9 | NVCC_JTAG | GPIO | — | JTAG_TRST_B | Input | 47 kΩ pull-up |
| KEY_COL0 | G20 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO10 | Input | Keeper |
| KEY_COL1 | F20 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO11 | Input | Keeper |
| KEY_COL2 | G18 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO12 | Input | Keeper |
| KEY_COL3 | E20 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO13 | Input | Keeper |
| KEY_COL4 | E19 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO14 | Input | Keeper |
| KEY_ROW0 | F16 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO15 | Input | Keeper |
| KEY_ROW1 | E18 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO16 | Input | Keeper |
| KEY_ROW2 | F18 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO17 | Input | Keeper |
| KEY_ROW3 | F19 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO18 | Input | Keeper |
| KEY_ROW4 | G19 | NVCC_KEY | GPIO | ALT5 | GPIO2_IO19 | Input | Keeper |
| LCD1_CLK | L17 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO00 | Input | Keeper |
| LCD1_DATA00 | M20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO01 | Input | Keeper |
| LCD1_DATA01 | M18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO02 | Input | Keeper |
| LCD1_DATA02 | M19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO03 | Input | Keeper |
| LCD1_DATA03 | N19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO04 | Input | Keeper |
| LCD1_DATA04 | N20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO05 | Input | Keeper |
| LCD1_DATA05 | M16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO06 | Input | Keeper |
| LCD1_DATA06 | M15 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO07 | Input | Keeper |
| LCD1_DATA07 | L20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO08 | Input | Keeper |
| LCD1_DATA08 | K18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO09 | Input | Keeper |
| LCD1_DATA09 | L16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO10 | Input | Keeper |
| LCD1_DATA10 | L19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO11 | Input | Keeper |
| LCD1_DATA11 | L15 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO12 | Input | Keeper |
| LCD1_DATA12 | K16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO13 | Input | Keeper |
| LCD1_DATA13 | K15 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO14 | Input | Keeper |
| LCD1_DATA14 | K17 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO15 | Input | Keeper |
| LCD1_DATA15 | H16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO16 | Input | Keeper |

**Table 119. 14 x 14 Functional Contact Assignments (continued)**

| Ball Name | 14x14 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|---|---|---|---|---|---|---|---|
| | | | | Default Mode | Default Function | Input/ Output | Value |
| DRAM_DATA28 | A2 | NVCC_DRAM | DDR | — | DRAM_DATA28 | Input | 100 kΩ pull-up |
| DRAM_DATA29 | C5 | NVCC_DRAM | DDR | — | DRAM_DATA29 | Input | 100 kΩ pull-up |
| DRAM_DATA30 | B4 | NVCC_DRAM | DDR | — | DRAM_DATA30 | Input | 100 kΩ pull-up |
| DRAM_DATA31 | A4 | NVCC_DRAM | DDR | — | DRAM_DATA31 | Input | 100 kΩ pull-up |
| DRAM_DQM0 | N1 | NVCC_DRAM | DDR | — | DRAM_DQM0 | Output | 100 kΩ pull-up |
| DRAM_DQM1 | G2 | NVCC_DRAM | DDR | — | DRAM_DQM1 | Output | 100 kΩ pull-up |
| DRAM_DQM2 | W1 | NVCC_DRAM | DDR | — | DRAM_DQM2 | Output | 100 kΩ pull-up |
| DRAM_DQM3 | C1 | NVCC_DRAM | DDR | — | DRAM_DQM3 | Output | 100 kΩ pull-up |
| DRAM_ODT0 | T1 | NVCC_DRAM | DDR | — | DRAM_ODT0 | Output | 100 kΩ pull-down |
| DRAM_RAS_B | J1 | NVCC_DRAM | DDR | — | DRAM_RAS_B | Output | 100 kΩ pull-up |
| DRAM_RESET | D4 | NVCC_DRAM | DDR | — | DRAM_RESET | Output | 100 kΩ pull-down |
| DRAM_SDBA0 | G4 | NVCC_DRAM | DDR | — | DRAM_SDBA0 | Output | 100 kΩ pull-up |
| DRAM_SDBA1 | M2 | NVCC_DRAM | DDR | — | DRAM_SDBA1 | Output | 100 kΩ pull-up |
| DRAM_SDBA2 | J2 | NVCC_DRAM | DDR | — | DRAM_SDBA2 | Output | 100 kΩ pull-up |
| DRAM_SDCKE0 | L5 | NVCC_DRAM | DDR | — | DRAM_SDCKE0 | Output | 100 kΩ pull-down |
| DRAM_SDCKE1 | J5 | NVCC_DRAM | DDR | — | DRAM_SDCKE1 | Output | 100 kΩ pull-down |
| DRAM_SDCLK0_N | L1 | NVCC_DRAM | DDRCLK | — | DRAM_SDCLK0_N | — | — |
| DRAM_SDCLK0_P | K1 | NVCC_DRAM | DDRCLK | — | DRAM_SDCLK0_P | Output | Low |
| DRAM_SDQS0_N | P2 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS0_N | — | — |
| DRAM_SDQS0_P | P1 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS0_P | Input | — |
| DRAM_SDQS1_N | H1 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS1_N | — | — |
| DRAM_SDQS1_P | G1 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS1_P | Input | — |
| DRAM_SDQS2_N | V2 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS2_N | — | — |
| DRAM_SDQS2_P | V1 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS2_P | Input | — |
| DRAM_SDQS3_N | B1 | NVCC_DRAM | DDRCLK | — | DRAM_SDQS3_N | — | — |

**Table 119. 14 x 14 Functional Contact Assignments (continued)**

| Ball Name | 14x14 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|---|---|---|---|---|---|---|---|
| | | | | Default Mode | Default Function | Input/ Output | Value |
| LCD1_DATA19 | J20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO20 | Input | Keeper |
| LCD1_DATA20 | H17 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO21 | Input | Keeper |
| LCD1_DATA21 | G18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO22 | Input | Keeper |
| LCD1_DATA22 | G19 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO23 | Input | Keeper |
| LCD1_DATA23 | G16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO24 | Input | Keeper |
| LCD1_ENABLE | K20 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO25 | Input | Keeper |
| LCD1_HSYNC | J15 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO26 | Input | Keeper |
| LCD1_RESET | J18 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO27 | Input | Keeper |
| LCD1_VSYNC | J16 | NVCC_LCD1 | GPIO | ALT5 | GPIO3_IO28 | Input | Keeper |
| NAND_ALE | W6 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO00 | Input | Keeper |
| NAND_CE0_B | U7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO01 | Input | Keeper |
| NAND_CE1_B | T8 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO02 | Input | Keeper |
| NAND_CLE | R7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO03 | Input | Keeper |
| NAND_DATA00 | V6 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO04 | Input | Keeper |
| NAND_DATA01 | W8 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO05 | Input | Keeper |
| NAND_DATA02 | Y7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO06 | Input | Keeper |
| NAND_DATA03 | U5 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO07 | Input | Keeper |
| NAND_DATA04 | W7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO08 | Input | Keeper |
| NAND_DATA05 | T5 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO09 | Input | Keeper |
| NAND_DATA06 | Y8 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO10 | Input | Keeper |
| NAND_DATA07 | T6 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO11 | Input | Keeper |
| NAND_RE_B | U8 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO12 | Input | Keeper |
| NAND_READY_B | Y6 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO13 | Input | Keeper |
| NAND_WE_B | T7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO14 | Input | Keeper |
| NAND_WP_B | V7 | NVCC_NAND | GPIO | ALT5 | GPIO4_IO15 | Input | Keeper |
| ONOFF | U16 | VDD_SNVS_IN | GPIO | — | ONOFF | Input | 100 kΩ pull-up |
| POR_B | R16 | VDD_SNVS_IN | GPIO | — | POR_B | Input | 100 kΩ pull-up |
| QSPI1A_DATA0 | E15 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO16 | Input | Keeper |
| QSPI1A_DATA1 | C15 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO17 | Input | Keeper |
| QSPI1A_DATA2 | D14 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO18 | Input | Keeper |
| QSPI1A_DATA3 | A18 | NVCC_QSPI | GPIO | ALT5 | GPIO4_IO19 | Input | Keeper |

**Table 119. 14 x 14 Functional Contact Assignments (continued)**

| Ball Name | 14x14 Ball | Power Group | Ball Type | Out of Reset Condition | | | |
|---|---|---|---|---|---|---|---|
| | | | | Default Mode | Default Function | Input/ Output | Value |
| SD4_DATA0 | Y10 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO14 | Input | Keeper |
| SD4_DATA1 | Y11 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO15 | Input | Keeper |
| SD4_DATA2 | Y13 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO16 | Input | Keeper |
| SD4_DATA3 | W13 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO17 | Input | Keeper |
| SD4_DATA4 | Y12 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO18 | Input | Keeper |
| SD4_DATA5 | W10 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO19 | Input | Keeper |
| SD4_DATA6 | U10 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO20 | Input | Keeper |
| SD4_DATA7 | W11 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO21 | Input | Keeper |
| SD4_RESET_B | V10 | NVCC_SD4 | GPIO | ALT5 | GPIO6_IO22 | Input | Keeper |
| SNVS_PMIC_ON_REQ | P15 | VDD_SNVS_IN | GPIO | — | SNVS_PMIC_ON_REQ | Output | 100 kΩ pull-up |
| SNVS_TAMPER | P14 | VDD_SNVS_IN | GPIO | — | SNVS_TAMPER | Input | 100 kΩ pull-down |
| TEST_MODE | V15 | VDD_SNVS_IN | — | — | TEST_MODE | Input | 100 kΩ pull-down |
| USB_H_DATA | Y5 | NVCC_USB_H | GPIO | ALT5 | GPIO7_IO10 | Input | 100 kΩ pull-down |
| USB_H_STROBE | W5 | NVCC_USB_H | GPIO | ALT5 | GPIO7_IO11 | Input | 100 kΩ pull-down |
| USB_OTG1_CHD_B | T17 | VDD_USB_CAP | — | — | USB_OTG1_CHD_B | — | — |
| USB_OTG1_DN | V19 | VDD_USB_CAP | — | — | USB_OTG1_DN | — | — |
| USB_OTG1_DP | V20 | VDD_USB_CAP | — | — | USB_OTG1_DP | — | — |
| USB_OTG2_DN | Y19 | VDD_USB_CAP | — | — | USB_OTG2_DN | — | — |
| USB_OTG2_DP | W19 | VDD_USB_CAP | — | — | USB_OTG2_DP | — | — |
| XTALI | T19 | NVCC_PLL | — | — | XTALI | — | — |
| XTALO | T20 | NVCC_PLL | — | — | XTALO | — | — |

### 6.5.3 14 x 14 mm, 0.65 mm pitch, 20 x 20 Ball Map

Table 120 shows the 14 x14 mm, 0.65 mm pitch, 20 x 20 ball map for the i.MX 6SoloX.

**Table 121. i.MX 6SoloX Data Sheet Document Revision History (continued)**

| Rev. Number | Date | Substantive Change(s) |
|---|---|---|
| 2 | 06/2016 | • Changed throughout:<br>- VDD_AFE_3P3 to VDDA_AFE_3P3<br>- VDDAD to VDDA_ADC_3P3<br>• Table 1, changed all instances of “2N19K” to “2N19K or 3N19K”.<br>• Figure 1, added new row under Silicon Rev, “Rev 1.3 Production...”<br>• Table 2, i.MX 6SoloX Modules List:<br>- BCH, deleted “encryption/decryption” in Brief Description column<br>- eCSPI1-eCSPI5: deleted “with data rate...” in Brief Description column<br>- uSDHC1-uSDHC4: added “Conforms to the SD...”<br>- uSDHC1-uSDHC4: deleted 7th and 8th paragraphs<br>- uSDHC1-uSDHC4: added “Each port is placed...”<br>• Table 3, Special Signal Considerations<br>- Signal Name, GPANAIO: updated text to “Analog output for NXP...”<br>- Signal Name, POR_B: deleted second sentence<br>• Section 3.2, “Recommended Connections for Unused Analog Interfaces”, removed text and original table, Recommended Connections for Unused Analog Interfaces, and referred reader to the Hardware Development Guide.<br>• Section 4.1.1, “Absolute Maximum Ratings<br>- added new CAUTION<br>- updated Table 6, Absolute Maximum Ratings<br>• Section 4.1.2, “Thermal Resistance, added NOTE<br>• Table 7, 19x19 mm (VM)..., corrected Junction to Package Top value 0.2 to 2<br>• Table 8, 17x17 mm NP (VO)..., corrected Junction to Package Top value 0.2 to 2<br>• Table 9, 14x14 mm (VK)..., updated Junction to Package Top value 0.2 to 2<br>• Table 9, Operating ranges, USB supply voltages: changed 5.25 to 5.5<br>• Table 12, Maximum Supply Currents<br>- added text: Use Maximum IO equation<br>- added footnotes<br>• Section 4.2.1, “Power-Up Sequence, - Removed references to the internal POR function. Internal POR is not supported on the i.MX 6SoloX.”<br>- Deleted bullets 4 and 5<br>• Section 4.3.2.3, “LDO_USB, changed 5.25 to 5.5<br>• Section 4.6.1, “XTALI and RTC_XTALI (Clock Inputs) DC Parameters, added new NOTE.<br>• Table 23, XTALI and RTC_XTALI DC Parameters, added new footnote, “This voltage specification...”<br>• Section 4.10, “Multi-mode DDR Controller (MMDC) this new section added, replacing the original section 4.9.4 DDR SRAM Specific Parameters (DDR3/DDR3L and LPDDR2).<br>• Table 56, SDR50/SDR104 Interface..., changed SD2 Min and max values to 0.46 and 0.54. Changed SD5 Max to 0.74.<br>• Table 63, RGMII Signal Switching Specifications, deleted footnote 1.<br>• Table 75, Master Mode SAI Timing:<br>- changed S1 Min value to 20<br>- changed S3 Min value to 2 x S1<br>*(continued on next page)* |

**Table 121. i.MX 6SoloX Data Sheet Document Revision History (continued)**

| Rev. Number | Date | Substantive Change(s) |
|---|---|---|
| 1 | 7/2015 | *(continued from previous page)*<br>• Updated Table 44, "EIM Asynchronous Timing Parameters Relative to Chip Select," on page 60. Elaborated to show results of calculations. No specification change.<br>• In Table 64, “DDR3/DDR3L Read Cycle,” on page 93, updated minimum value for DDR26<br>• Added note regarding ECSPIx_MOSI to Figure 36, "ECSPI Master Mode Timing Diagram," on page 74<br>• Added note regarding ECSPIx_MISO to Figure 37, "ECSPI Slave Mode Timing Diagram," on page 75<br>• Updated Figure 42, "SDR50/SDR104 Timing," on page 82<br>• In Table 67, "LVDS Display Bridge (LDB) Electrical Specification," on page 93:<br>– Corrected units for $V_{OH}$ values from ‘mV’ to ‘V’<br>– Corrected units for $V_{OL}$ values from ‘mV’ to ‘V’<br>• In Section 4.12.20, “USB PHY Parameters,” in list of amendments to Rev. 2 of the The USB PHY meets the electrical compliance requirements defined in revision 2.0 of the *USB On-The-Go and Embedded Host Supplement to the USB 2.0 Specification,* added “Portable device only” under “Battery Charging Specification”<br>• Added Table 107, "Signals with Different States During Reset and After Reset," on page 130<br>• In Table 109, "19x19 mm Functional Contact Assignments," on page 136, corrected GPIO signal names<br>• In Table 112, "17x17 mm NP (no PCIe) Supplies Contact Assignments," on page 155, added ball L9 to the VDD_SOC_CAP row<br>• In Table 119, "14 x 14 Functional Contact Assignments," on page 189, corrected power group for SD2 ball names to ‘NVCC_SD1_SD2’ |
| 0 | 2/2015 | • Initial public release |