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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9, ARM® Cortex®-M4
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	200MHz, 800MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1), USB 2.0 OTG + PHY (2)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.15V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	A-HAB, ARM TZ, CAAM, CSU, SNVS, System JTAG, TVDECODE
Package / Case	400-LFBGA
Supplier Device Package	400-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6x1cvo08acr

Figure 1 describes the part number nomenclature so that the users can identify the characteristics of the specific part number they have (for example, cores, frequency, temperature grade, fuse options, and silicon revision). The primary characteristic which describes which data sheet applies to a specific part is the temperature grade (junction) field.

- The i.MX 6SoloX Automotive and Infotainment Applications Processors data sheet (IMX6SXAEC) covers parts listed with an “A (Automotive temp)”
- The i.MX 6SoloX Applications Processors for Consumer Products data sheet (IMX6SXCEC) covers parts listed with a “D (Commercial temp)” or “E (Extended Commercial temp)”
- The i.MX 6SoloX Applications Processors for Industrial Products data sheet (IMX6SXIEC) covers parts listed with “C (Industrial temp)”

Ensure to have the proper data sheet for specific part by verifying the temperature grade (junction) field and matching it to the proper data sheet. If there will be any questions, visit see the web page nxp.com/imx6series or contact a NXP representative for details.

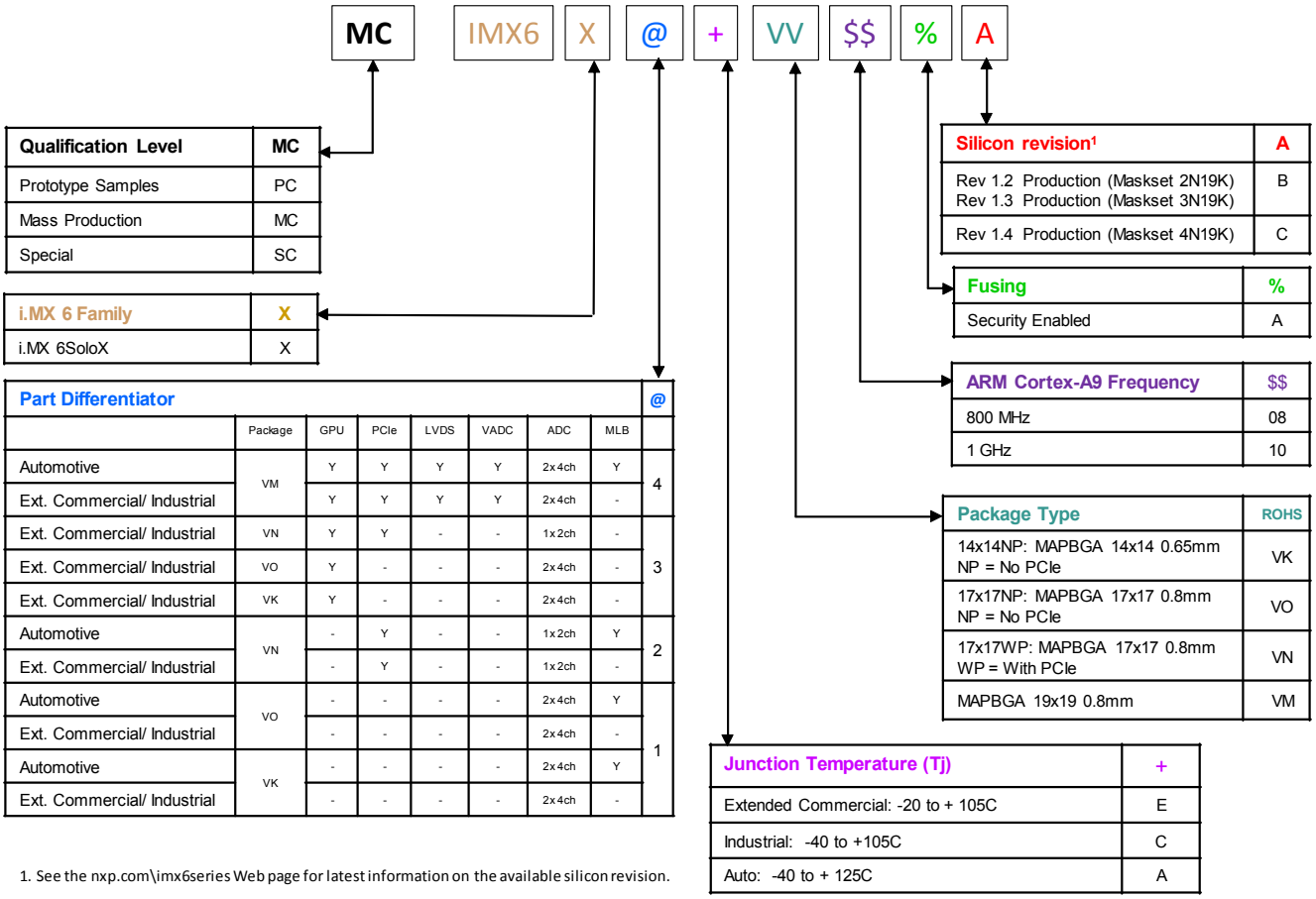


Figure 1. Part Number Nomenclature—i.MX 6SoloX

1.2 Features

The i.MX 6SoloX processors are based on the ARM Cortex-A9 MPCore™ platform, which has the following features:

- Supports single ARM Cortex-A9 MPCore processor (with TrustZone)
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) coprocessor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 256 KB unified I/D L2 cache:
- Two Master AXI bus interfaces output of L2 cache
- Frequency of the core (including NEON coprocessor and L1 cache), as per Table 9, "Operating Ranges," on page 27.
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline
  - 32 double-precision VFPv3 floating point registers

The ARM Cortex-M4 platform:

- Cortex-M4 CPU core
- MPU (Memory Protection Unit)
- FPU (Floating Point Unit)
- 16 KByte Instruction Cache
- 16 KByte Data Cache
- 64 KByte TCM (Tightly-Coupled Memory)

The SoC-level memory system consists of the following additional components:

- Boot ROM, including HAB (96 KB)
- Internal multimedia / shared, fast access RAM (OCRAM, 128 KB)
- Internal RAM for state retention or general use (OCRAM_S, 16KB)
- Secure/non-secure RAM (32 KB)

- Four I^2C
- Two Gigabit Ethernet Controllers (designed to be compatible with IEEE AVB standards and IEEE Std 1588®), 10/100/1000 Mbps
- Eight Pulse Width Modulators (PWM)
- System JTAG Controller (SJC)
- GPIO with interrupt capabilities
- 8x8 Key Pad Port (KPP)
- Two Quad SPIs
- Two Flexible Controller Area Network (FlexCAN), 1 Mbps each
- Three Watchdog timers (WDOG)
- Up to two 4-channel, 12-bit Analog to Digital Converters (ADC), VM, VO, VK packages
- One 2-channel, 12-bit Analog to Digital Converter (ADC), VN package

The i.MX 6SoloX processors integrate advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use software state retention and power gating for ARM Cortex-A9 CPU core, the ARM Cortex-M4 CPU core, and the ARM NEON MPE coprocessor.
- Support various levels of system power modes
- Use flexible clock gating control scheme

The i.MX 6SoloX processors use dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption, while having the CPU core relatively free for performing other tasks.

The i.MX 6SoloX processors incorporate the following hardware accelerators:

- GPU—2D (BitBlt) and 3D (OpenGL ES) Graphics Processing Unit
- PXP—PiXel Processing Pipeline for imagine resize, rotation, overlay and CSC. Off loading key pixel processing operations are required to support the LCD display applications.
- ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM—Cryptographic Acceleration and Assurance Module, containing cryptographic and hash engines, 32 KB secure RAM, and True and Pseudo Random Number Generator (NIST certified).
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock
- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSEs and will determine the security level operation mode as well as the TZ policy.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6SoloX processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6SoloX processor system.

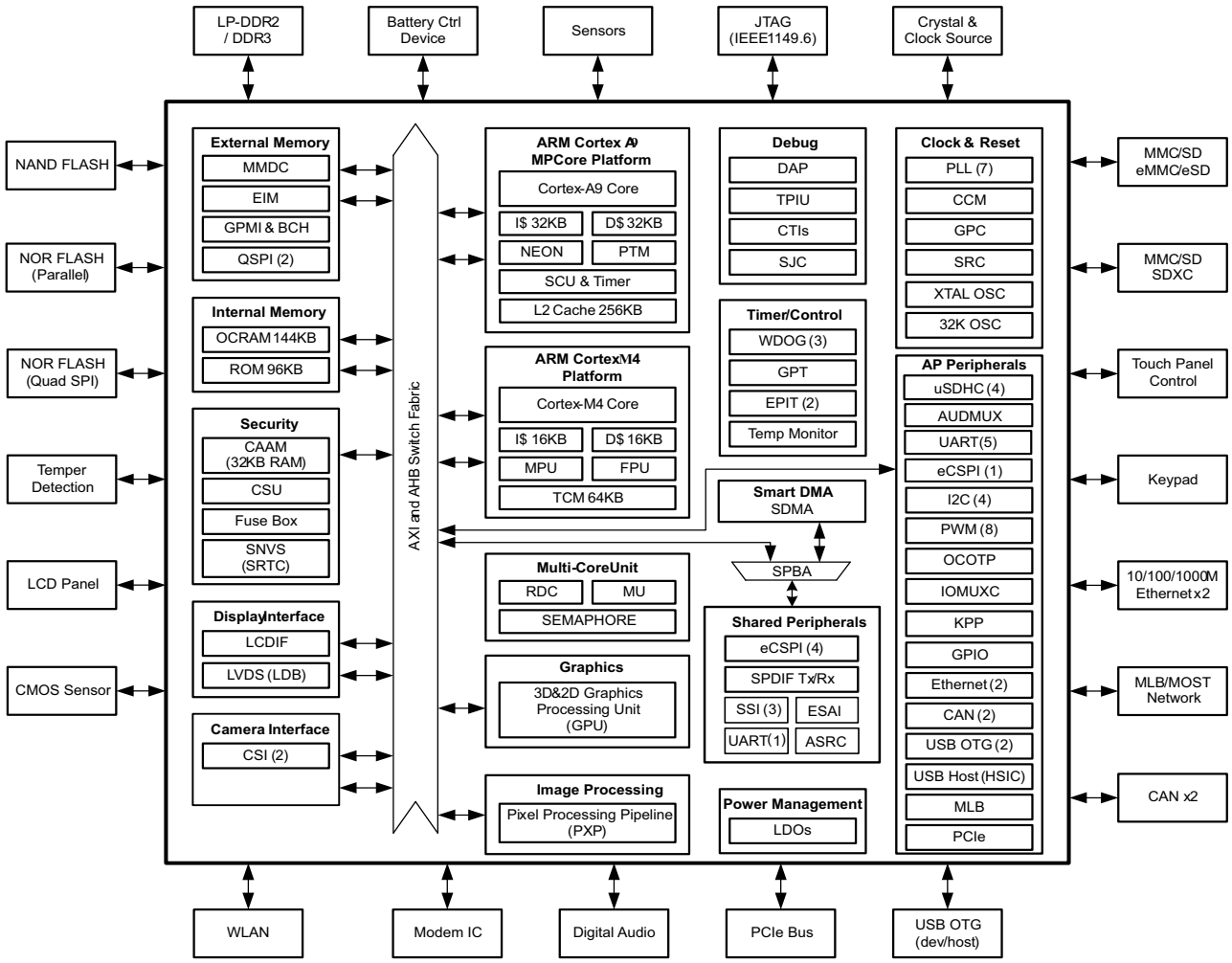


Figure 2. i.MX 6SoloX System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (8) indicates eight separate PWM peripherals.

Table 2. i.MX 6SoloX Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
CSI	Parallel CSI	Multimedia Peripherals	The CSI IP provides parallel CSI standard camera interface port. The CSI parallel data ports are up to 24 bits. It is designed to support 24-bit RGB888/YUV444, CCIR656 video interface, 8-bit YCbCr, YUV or RGB, and 8-bit/10-bit/26-bit Bayer data input.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6SoloX platform.
CTI	Cross Trigger Interfaces	Debug/Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: System memory and peripheral registers All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.
DBGMON	Debug Monitor	Debug	DBGMON is a real-time debug monitor to record last AXI transaction before system reset.
eCSPI1 eCSPI2 eCSPI3 eCSPI4 eCSPI5	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency Multiple chip selects
ENET1 ENET2	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the *i.MX 6SoloX Applications Processor Reference Manual* (IMX6SXRM) for details.
EPIT1 EPIT2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.

Table 2. i.MX 6SoloX Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: Powered by a 16-bit Instruction-Set micro-RISC engine Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels 48 events with total flexibility to trigger any combination of channels Memory accesses including linear, FIFO, and 2D addressing Shared peripherals between ARM and SDMA Very fast Context-Switching with 2-level priority based preemptive multi-tasking DMA units with auto-flush and prefetch capability Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) DMA ports can handle unit-directional and bi-directional flows (copy mode) Up to 8-word buffer for configurable burst transfers for EMIv2.5 Support of byte-swapping and CRC calculations Library of Scripts and API is available
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6SoloX processors use JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6SoloX SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.
SPDIF	Sony Philips Digital Interconnect Format	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.

Table 13. Low Power Mode Current and Power Consumption (LDO Bypass Mode) (continued)

Mode	Test Conditions	Supply	Typical[1]	Units
Suspend/ Deep Sleep mode (DSM)	See the Power Modes table in the Clock and Power Management chapter of the *i.MX 6SoloX Applications Processor Reference Manual* (IMX6SXRM) for the definition of this mode.	VDD_ARM_IN (0.9 V)	0.001	mA
		VDD_SOC_IN (1.05 V)	1.005	
		VDDHIGH_IN (3.3 V)	0.034	
		Total	2.067	mW
SNVS	SNVS power domain powered. All other power domains are off.	VDD_SNVS_IN (2.8 V)	41	µA
		Total	0.115	mW

1 Typical process material in fab.

Table 14. Low Power Mode Current and Power Consumption (LDO Enabled Mode)

Mode	Test Conditions	Supply	Typical[1]	Units
Low Power Idle	See the Power Modes table in the Clock and Power Management chapter of the *i.MX 6SoloX Applications Processor Reference Manual* (IMX6SXRM) for the definition of this mode. SOC LDO is enabled. Bandgap is enabled.	VDDARM_IN (1.3V)	0.008	mA
		VDDSOC_IN (1.3V)	2.343	
		VDDHIGH_IN (3.3V)	3.376	
		Total	14.196	mW
Suspend/ Deep Sleep mode (DSM	See the Power Modes table in the Clock and Power Management chapter of the *i.MX 6SoloX Applications Processor Reference Manual* (IMX6SXRM) for the definition of this mode.	VDDARM_IN (1.3V)	0.033	mA
		VDDSOC_IN (1.3V)	1.3	
		VDDHIGH_IN (3.3V)	0.034	
		Total	2.231	mW

1 Typical process material in fab.

4.1.7 USB PHY Current Consumption

4.1.7.1 Power Down Mode

In power down mode, everything is powered down, including the USB_VBUS valid detectors in typical condition. Table 15 shows the USB interface current consumption in power down mode.

Table 15. USB PHY Current Consumption in Power Down Mode

	VDD_USB_CAP (3.0 V)	VDD_HIGH_CAP (2.5 V)	NVCC_PLL (1.1 V)
Current	5.1 µA	1.7 µA	<0.5 µA

NOTE

The currents on the VDD_HIGH_CAP and VDD_USB_CAP were identified to be the voltage divider circuits in the USB-specific level shifters.

2 In this table:
t means clock period from axi_clk frequency.
CSA means register setting for WCSA when in write operations or RCSA when in read operations.
CSN means register setting for WCSN when in write operations or RCSN when in read operations.
ADVN means register setting for WADVN when in write operations or RADVN when in read operations.
ADVA means register setting for WADVA when in write operations or RADVA when in read operations.

4.10 Multi-mode DDR Controller (MMDC)

The Multi-mode DDR Controller is a dedicated interface to DDR3/DDR3L/LPDDR2 SDRAM.

4.10.1 MMDC Compatibility with JEDEC-Compliant SDRAMs

The i.MX 6SoloX MMDC supports the following memory types:

- LPDDR2 SDRAM compliant to JESD209-2B LPDDR2 JEDEC standard release June, 2009
- DDR3 SDRAM compliant to JESD79-3D DDR3 JEDEC standard release April, 2008

MMDC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the Hardware Development Guide for i.MX 6SoloX Application Processors (IMX6SXHDG).

4.10.2 MMDC Supported DDR3/LPDDR2 Configurations

The table below shows the supported DDR3/LPDDR2 configurations:

Table 45. i.MX 6SoloX Supported DDR3/LPDDR2 Configurations

Parameter	Min	Max	Unit
LPDDR2			
JEDEC LPDDR2 Device Speed Grade[1]	LPDDR2-800	—	—
JEDEC LPDDR2 Device Bus Width	x16	x32	Bits
JEDEC LPDDR2 Device Count[2]	1	2	Devices
DDR3/DDR3L			
JEDEC DDR3/DDR3L Device Speed Grade[3]	DDR3-800	—	—
JEDEC DDR3/DDR3L Device Bus Width	x16	x32	Bits
JEDEC DDR3/DDR3L Device Count[4]	1	2	Devices

1 Higher speed grade memories are supported as long as they are backward compatible with the speed grade shown.
2 Supported configurations are one 32-bit DDR memory or two 16-bit DDR memories.
3 Higher speed grade memories are supported as long as they are backward compatible with the speed grade shown.
4 Supported configurations are one 32-bit DDR memory or two 16-bit DDR memories.

4.12.4 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 53 shows the interface timing values. The number field in the table refers to timing signals found in Figure 38 and Figure 39.

Table 53. Enhanced Serial Audio Interface (ESAI) Timing

No.	Characteristics[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
62	Clock cycle[4]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period: • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
64	Clock low period: • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
65	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) high	— —	— —	— —	17.0 7.0	x ck i ck a	ns
66	ESAI_RX_CLK rising edge to ESAI_RX_FS out (bl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
67	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) high[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wr) low[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wl) high	— —	— —	— —	16.0 6.0	x ck i ck a	ns
70	ESAI_RX_CLK rising edge to ESAI_RX_FS out (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before ESAI_RX_CLK (SCK in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after ESAI_RX_CLK falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	ESAI_RX_FS input (bl, wr) high before ESAI_RX_CLK falling edge[5]	— —	— —	2.0 12.0	— —	x ck i ck a	ns
74	ESAI_RX_FS input (wl) high before ESAI_RX_CLK falling edge	— —	— —	2.0 12.0	— —	x ck i ck a	ns
75	ESAI_RX_FS input hold time after ESAI_RX_CLK falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
78	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) high	— —	— —	— —	18.0 8.0	x ck i ck	ns
79	ESAI_TX_CLK rising edge to ESAI_TX_FS out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
80	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) high[5]	— —	— —	— —	20.0 10.0	x ck i ck	ns

Table 53. Enhanced Serial Audio Interface (ESAI) Timing (continued)

No.	Characteristics[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
81	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) low[5]	— —	— —	— —	22.0 12.0	x ck i ck	ns
82	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	ESAI_TX_CLK rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
86	ESAI_TX_CLK rising edge to data out valid	— —	— —	— —	18.0 13.0	x ck i ck	ns
87	ESAI_TX_CLK rising edge to data out high impedance [6][7]	— —	— —	— —	21.0 16.0	x ck i ck	ns
89	ESAI_TX_FS input (bl, wr) setup time before ESAI_TX_CLK falling edge[5]	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	ESAI_TX_FS input (wl) setup time before ESAI_TX_CLK falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	ESAI_TX_FS input hold time after ESAI_TX_CLK falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns
95	ESAI_RX_HF_CLK/ESAI_TX_HF_CLK clock cycle	—	$2 \times T_C$	15	—	—	ns
96	ESAI_TX_HF_CLK input rising edge to ESAI_TX_CLK output	—	—	—	18.0	—	ns
97	ESAI_RX_HF_CLK input rising edge to ESAI_RX_CLK output	—	—	—	18.0	—	ns

1 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are the same clock)

2 bl = bit length
wl = word length
wr = word length relative

3 ESAI_TX_CLK(SCKT pin) = transmit clock
ESAI_RX_CLK(SCKR pin) = receive clock
ESAI_TX_FS(FST pin) = transmit frame sync
ESAI_RX_FS(FSR pin) = receive frame sync
ESAI_TX_HF_CLK(HCKT pin) = transmit high frequency clock
ESAI_RX_HF_CLK(HCKR pin) = receive high frequency clock

4 For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

5 The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.

6 Periodically sampled and not 100% tested.

4.12.17.2 SSI Receiver Timing with Internal Clock

Figure 70 depicts the SSI receiver internal clock timing and Table 81 lists the timing parameters for the receiver timing with the internal clock.

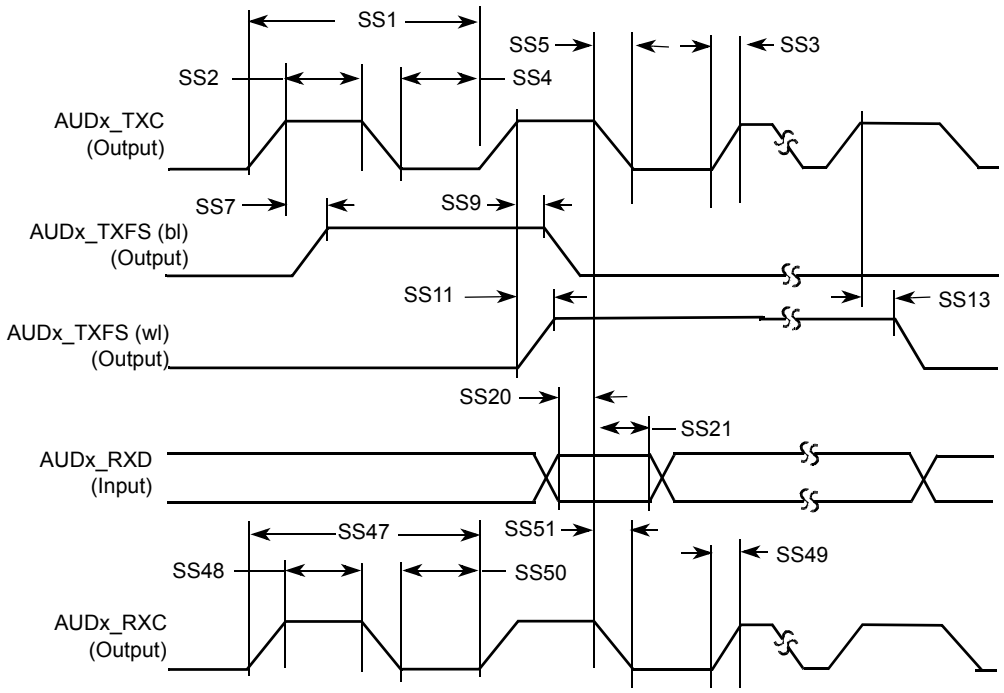


Figure 70. SSI Receiver Internal Clock Timing Diagram

Table 81. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS3	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS4	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS5	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS7	AUDx_RXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS9	AUDx_RXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS11	AUDx_RXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS13	AUDx_RXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS20	AUDx_RXD setup time before AUDx_RXC low	10.0	—	ns
SS21	AUDx_RXD hold time after AUDx_RXC low	0.0	—	ns

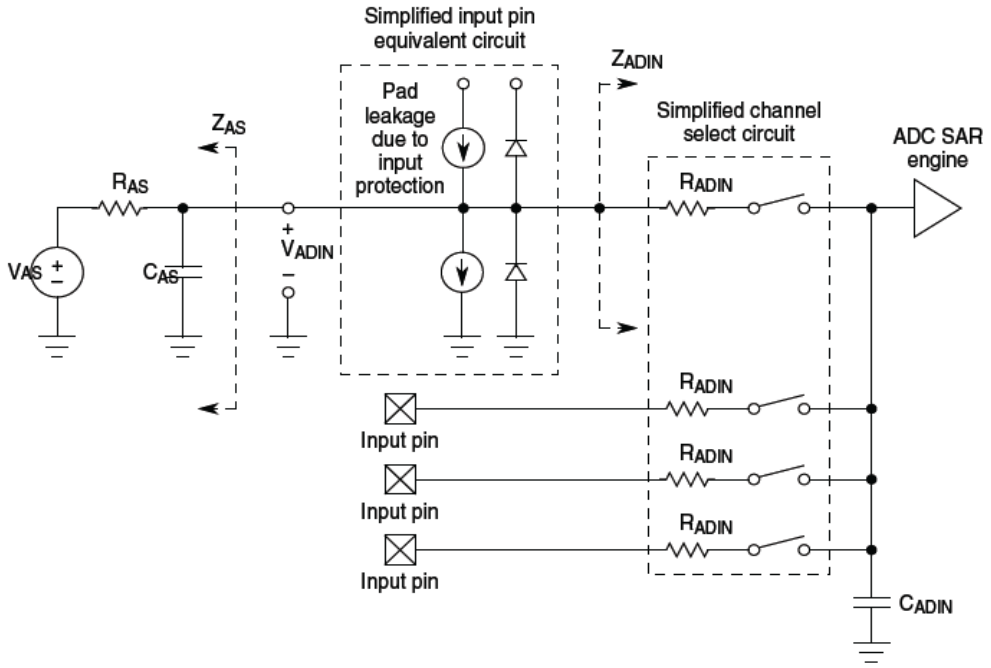


Figure 79. 12-bit ADC Input Impedance Equivalency Diagram

4.13.1.1.1 12-bit ADC Characteristics

Table 91. 12-bit ADC Characteristics (V_{REFH} = VDDA_ADC_3P3, V_{REFL} = V_{SSAD})

Characteristic	Conditions[1]	Symbol	Min	Typ[2]	Max	Unit	Comment
[L:] Supply Current	ADLPC=1, ADHSC=0	I_{DDAD}	—	250	—	μA	ADLSMP=0 ADSTS=10 ADCO=1
	ADLPC=0, ADHSC=0			350			
	ADLPC=0, ADHSC=1			400			
[L:] Supply Current	Stop, Reset, Module Off	I_{DDAD}	—	0.01	0.8	μA	—
ADC Asynchronous Clock Source	ADHSC=0	f_{ADACK}	—	10	—	MHz	$t_{ADACK} = 1/f_{ADACK}$
	ADHSC=1		—	20	—		
Sample Cycles	ADLSMP=0, ADSTS=00	Csamp	—	2	—	cycles	—
	ADLSMP=0, ADSTS=01			4			
	ADLSMP=0, ADSTS=10			6			
	ADLSMP=0, ADSTS=11			8			
	ADLSMP=1, ADSTS=00			12			
	ADLSMP=1, ADSTS=01			16			
	ADLSMP=1, ADSTS=10			20			
	ADLSMP=1, ADSTS=11			24			

Table 100. NAND Boot through GPMI

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG1[3:2]=01b	BOOT_CFG1[3:2]=10b
NAND_CLE	rawnand.CLE	Alt 0	Yes	—	—
NAND_ALE	rawnand.ALE	Alt 0	Yes	—	—
NAND_WP_B	rawnand.WP_B	Alt 0	Yes	—	—
NAND_READY_B	rawnand.READY_B	Alt 0	Yes	—	—
NAND_CE0_B	rawnand.CE0_B	Alt 0	Yes	—	—
NAND_CE1_B	rawnand.CE1_B	Alt 0	—	Yes	—
NAND_RE_B	rawnand.RE_B	Alt 0	Yes	—	—
NAND_WE_B	rawnand.WE_B	Alt 0	Yes	—	—
NAND_DATA00	rawnand.DATA00	Alt 0	Yes	—	—
NAND_DATA01	rawnand.DATA01	Alt 0	Yes	—	—
NAND_DATA02	rawnand.DATA02	Alt 0	Yes	—	—
NAND_DATA03	rawnand.DATA03	Alt 0	Yes	—	—
NAND_DATA04	rawnand.DATA04	Alt 0	Yes	—	—
NAND_DATA05	rawnand.DATA05	Alt 0	Yes	—	—
NAND_DATA06	rawnand.DATA06	Alt 0	Yes	—	—
NAND_DATA07	rawnand.DATA07	Alt 0	Yes	—	—
SD4_RESET_B	rawnand.DQS	Alt 1	Yes	—	—
SD4_DATA5	rawnand.CE2_B	Alt 1	—	—	Yes
SD4_DATA6	rawnand.CE3_B	Alt 1	—	—	Yes

Table 101. SD/MMC Boot through USDHC1

Ball Name	Signal Name	Mux Mode	Common	4-bit	8-bit	BOOT_CFG1[1]=1 (SD Power Cycle or SD boot with SDR50/SDR104)	SDMMC MFG Mode
GPIO1_IO02	usdhc1.CD_B	Alt 1	—	—	—	—	Yes
SD1_CLK	usdhc1.CLK	Alt 0	Yes	—	—	—	—
SD1_CMD	usdhc1.CMD	Alt 0	Yes	—	—	—	—
SD1_DATA0	usdhc1.DATA0	Alt 0	Yes	—	—	—	—
SD1_DATA1	usdhc1.DATA1	Alt 0	—	Yes	Yes	—	—
SD1_DATA2	usdhc1.DATA2	Alt 0	—	Yes	Yes	—	—
SD1_DATA3	usdhc1.DATA3	Alt 0	Yes	—	—	—	—
NAND_DATA00	usdhc1.DATA4	Alt 1	—	—	Yes	—	—
NAND_DATA01	usdhc1.DATA5	Alt 1	—	—	Yes	—	—

Table 101. SD/MMC Boot through USDHC1 (continued)

Ball Name	Signal Name	Mux Mode	Common	4-bit	8-bit	BOOT_CFG1[1]=1 (SD Power Cycle or SD boot with SDR50/SDR104)	SDMMC MFG Mode
NAND_DATA02	usdhc1.DATA6	Alt 1	—	—	Yes	—	—
NAND_DATA03	usdhc1.DATA7	Alt 1	—	—	Yes	—	—
NAND_WP_B	GPIO4_15	Alt 5	—	—	—	Yes	—
NAND_READY_B	usdhc1.VSELECT	Alt 1	—	—	—	Yes	—

Table 102. SD/MMC Boot through USDHC2

Ball Name	Signal Name	Mux Mode	Common	4-bit	8-bit	BOOT_CFG1[1]=1 (SD Power Cycle or SD boot with SDR50/SDR104)
SD2_CLK	usdhc2.CLK	Alt 0	Yes	—	—	—
SD2_CMD	usdhc2.CMD	Alt 0	Yes	—	—	—
SD2_DATA0	usdhc2.DATA0	Alt 0	Yes	—	—	—
SD2_DATA1	usdhc2.DATA1	Alt 0	—	Yes	Yes	—
SD2_DATA2	usdhc2.DATA2	Alt 0	—	Yes	Yes	—
SD2_DATA3	usdhc2.DATA3	Alt 0	Yes	—	—	—
NAND_DATA04	usdhc2.DATA4	Alt 1	—	—	Yes	—
NAND_DATA05	usdhc2.DATA5	Alt 1	—	—	Yes	—
NAND_DATA06	usdhc2.DATA6	Alt 1	—	—	Yes	—
NAND_DATA07	usdhc2.DATA7	Alt 1	—	—	Yes	—
NAND_RE_B	GPIO4_IO12	Alt 5	—	—	—	Yes
NAND_CE0_B	usdhc2.VSELECT	Alt 1	—	—	—	Yes

Table 103. SD/MMC Boot through USDHC3

Ball Name	Signal Name	Mux Mode	Common	4-bit	8-bit	BOOT_CFG1[1]=1 (SD Power Cycle or SD boot with SDR50/SDR104)
SD3_CLK	usdhc3.CLK	Alt 0	Yes	—	—	—
SD3_CMD	usdhc3.CMD	Alt 0	Yes	—	—	—
SD3_DATA0	usdhc3.DATA0	Alt 0	Yes	—	—	—
SD3_DATA1	usdhc3.DATA1	Alt 0	—	Yes	Yes	—
SD3_DATA2	usdhc3.DATA2	Alt 0	—	Yes	Yes	—

6.3.2 19x19 mm Supplies Contact Assignments and Functional Contact Assignments

Table 108 shows supplies contact assignments for the 19x19 mm package.

Table 108. 19x19 mm Supplies Contact Assignments

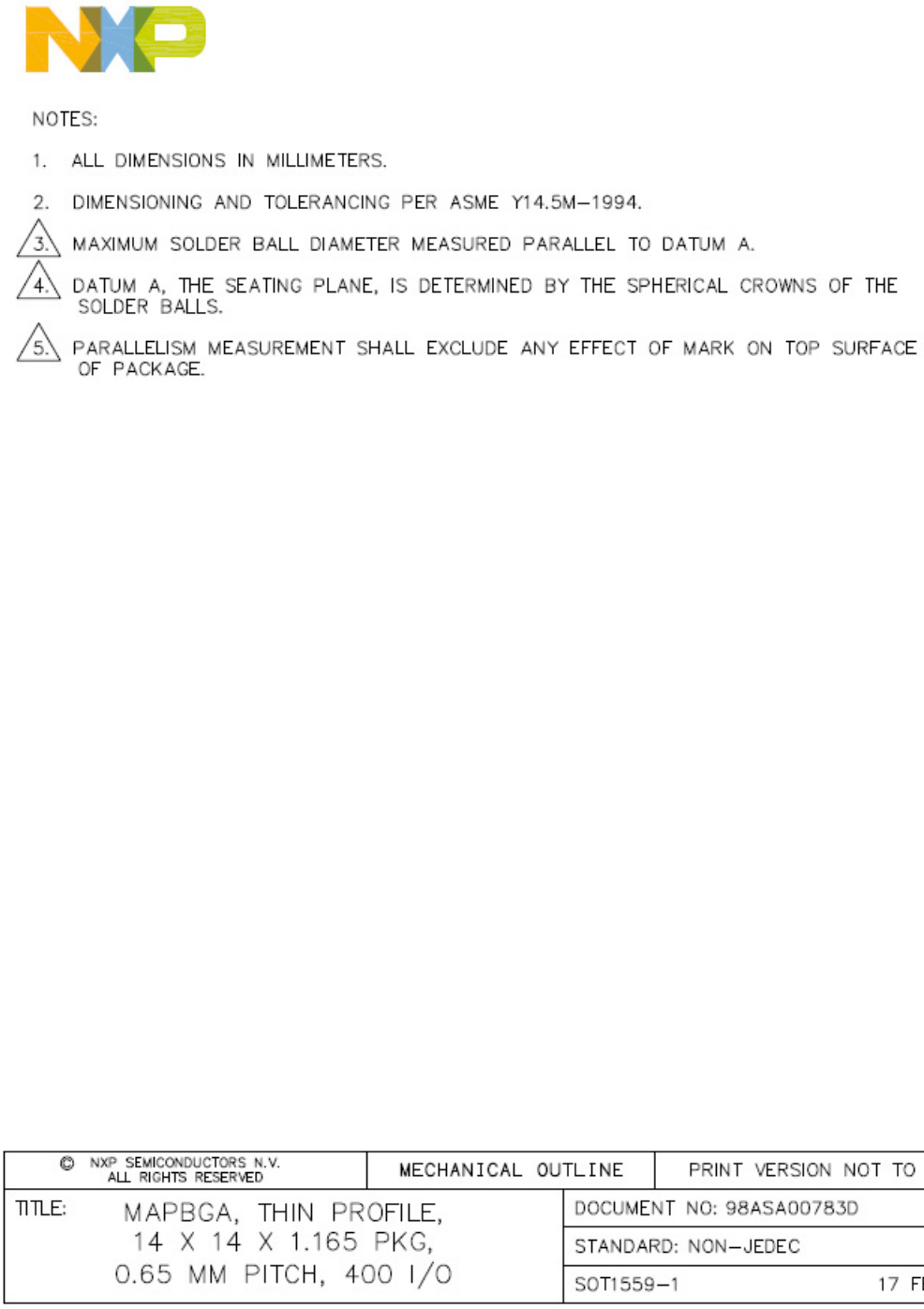
Supply Rail Name	19x19 Ball(s) Position(s)	Remark
ADC_VREFH	AA16	ADC high reference voltage
ADC_VREFL	U16	ADC low reference voltage
DRAM_VREF	M3	DDR voltage reference input. Connect to a voltage source that is 50% of NVCC_DRAM.
DRAM_ZQPAD	C4	DDR output buffer driver calibration reference voltage input. Connect DRAM_ZQPAD to an external 240 ohm 1% resistor to Vss.
GPANAIO	V18	Analog output for NXP use only. This output must always be left unconnected.
NGND_KEL0	R16	Connect to Vss
NVCC_CSI	P18	Supply input for the CSI interface
NVCC_DRAM	F5, G5, H5, J5, K5, L5, M5, N5, P5, R5, T5, U5, V5	Supply input for the DDR I/O interface
NVCC_DRAM_2P5	M6	Supply input for the DDR interface
NVCC_ENET	F6	Supply input for the ENET interfaces
NVCC_GPIO	G15	Supply input for the GPIO interface
NVCC_HIGH	U12	3.3 V Supply input for the dual-voltage I/Os on the SD3 interface
NVCC_JTAG	U11	Supply input for the JTAG interface
NVCC_KEY	G16	Supply input for the Key Pad Port (KPP) interface
NVCC_LCD1	G17	Supply input for the LCD interface
NVCC_LOW	V11	1.8 V Supply input for the dual-voltage IOs on the SD3 interface
NVCC_LVDS	T18	Supply input for the LVDS interface
NVCC_NAND	U8	Supply input for the Raw NAND flash memories interface
NVCC_PLL	Y23	Supply input for the PLLs
NVCC_QSPI	G14	Supply input for the QSPI interface
NVCC_RGMII1	F8	Supply input for the RGMII1 interface
NVCC_RGMII2	G9	Supply input for the RGMII2 interface
NVCC_SD1	G12	Supply input for the SD1 interface
NVCC_SD2	G11	Supply input for the SD2 interface
NVCC_SD4	U10	Supply input for the SD4 interface
NVCC_USB_H	AA6	Supply input for the USB HSIC interface
PCIE_REXT	M21	PCIe impedance calibration resistor. Connect PCIE_REXT to an external 200 ohm 1% resistor to Vss.
PCIE_VP	L18	Supply input for the PCIe PHY
PCIE_VPH	R18	Supply input for the PCIe PHY

Table 110. 19x19 mm, 0.8 mm Pitch, 23x23 Ball Map (continued)

	H	J	K	L	M	N	P
1	DRAM_SDQS1_P	DRAM_DATA08	DRAM_DATA12	DRAM_DATA09	DRAM_SDCLK0_N	DRAM_DATA05	DRAM_DATA04
2	DRAM_SDQS1_N	VSS	DRAM_DATA10	VSS	DRAM_SDCLK0_P	VSS	DRAM_DATA07
3	DRAM_ADDR03	VSS	DRAM_SDWE_B	VSS	DRAM_VREF	VSS	DRAM_ADDR09
4	DRAM_SDBA0	DRAM_CS0_B	DRAM_CAS_B	DRAM_RAS_B	DRAM_SDBA2	DRAM_ADDR00	DRAM_ADDR13
5	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM
6	VSS	VSS	VSS	VSS	NVCC_DRAM_2P5	VSS	VSS
7	VSS	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP
8	VSS	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN
9	VSS	VDD_SOC_CAP	VDD_SOC_IN	VSS	VSS	VSS	VDD_SOC_IN
10	VSS	VDD_SOC_CAP	VDD_SOC_IN	VSS	VSS	VSS	VDD_SOC_IN
11	VSS	VDD_SOC_CAP	VDD_SOC_IN	VSS	VSS	VSS	VDD_SOC_IN
12	VSS	VDD_ARM_CAP	VDD_ARM_IN	VSS	VSS	VSS	VDD_SOC_IN
13	VSS	VDD_ARM_CAP	VDD_ARM_IN	VSS	VSS	VSS	VDD_SOC_IN
14	VSS	VDD_ARM_CAP	VDD_ARM_IN	VSS	VSS	VSS	VDD_SOC_IN
15	VSS	VDD_ARM_CAP	VDD_ARM_IN	VDD_ARM_IN	VDD_ARM_IN	VDD_SOC_IN	VDD_SOC_IN
16	VSS	VDD_ARM_CAP	VDD_ARM_CAP	VDD_ARM_CAP	VDD_ARM_CAP	VDD_SOC_CAP	VDD_SOC_CAP
17	VSS	VSS	VSS	VSS	VSS	VSS	VSS
18	LCD1_DATA11	LCD1_DATA06	LCD1_DATA04	PCIE_VP	PCIE_VPTX	RSVD	NVCC_CSI
19	LCD1_DATA10	LCD1_DATA05	LCD1_DATA03	CSI_DATA07	CSI_DATA06	CSI_DATA04	CSI_DATA02
20	LCD1_DATA09	VSS	LCD1_DATA02	CSI_HSYNC	VSS	CSI_DATA05	CSI_DATA01
21	LCD1_CLK	VDD_ARM_IN	RSVD	RSVD	PCIE_REXT	CSI_DATA03	CSI_DATA00
22	LCD1_DATA08	LCD1_DATA01	RSVD	RSVD	VSS	PCIE_RX_N	PCIE_TX_N
23	LCD1_DATA07	LCD1_DATA00	RSVD	RSVD	VSS	PCIE_RX_P	PCIE_TX_P
	H	J	K	L	M	N	P

Table 116. 17x17 WP (with PCIe) Functional Contact Assignments (continued)

Ball Name	17x17 WP Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
ENET1_MDIO	A6	NVCC_ENET	GPIO	ALT5	GPIO2_IO03	Input	Keeper
ENET1_RX_CLK	A5	NVCC_ENET	GPIO	ALT5	GPIO2_IO04	Input	Keeper
ENET1_TX_CLK	F7	NVCC_ENET	GPIO	ALT5	GPIO2_IO05	Input	Keeper
ENET2_COL	E7	NVCC_ENET	GPIO	ALT5	GPIO2_IO06	Input	Keeper
ENET2_CRS	E6	NVCC_ENET	GPIO	ALT5	GPIO2_IO07	Input	Keeper
ENET2_RX_CLK	E5	NVCC_ENET	GPIO	ALT5	GPIO2_IO08	Input	Keeper
ENET2_TX_CLK	D5	NVCC_ENET	GPIO	ALT5	GPIO2_IO09	Input	Keeper
GPIO1_IO00	C19	NVCC_GPIO	GPIO	ALT5	GPIO1_IO00	Input	Keeper
GPIO1_IO01	D19	NVCC_GPIO	GPIO	ALT5	GPIO1_IO01	Input	Keeper
GPIO1_IO02	C20	NVCC_GPIO	GPIO	ALT5	GPIO1_IO02	Input	Keeper
GPIO1_IO03	D20	NVCC_GPIO	GPIO	ALT5	GPIO1_IO03	Input	Keeper
GPIO1_IO04	A18	NVCC_GPIO	GPIO	ALT5	GPIO1_IO04	Input	Keeper
GPIO1_IO05	B18	NVCC_GPIO	GPIO	ALT5	GPIO1_IO05	Input	Keeper
GPIO1_IO06	D18	NVCC_GPIO	GPIO	ALT5	GPIO1_IO06	Input	Keeper
GPIO1_IO07	A17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO07	Input	Keeper
GPIO1_IO08	B17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO08	Input	Keeper
GPIO1_IO09	A19	NVCC_GPIO	GPIO	ALT5	GPIO1_IO09	Input	Keeper
GPIO1_IO10	B19	NVCC_GPIO	GPIO	ALT5	GPIO1_IO10	Input	Keeper
GPIO1_IO11	B20	NVCC_GPIO	GPIO	ALT5	GPIO1_IO11	Input	Keeper
GPIO1_IO12	B16	NVCC_GPIO	GPIO	ALT5	GPIO1_IO12	Input	Keeper
GPIO1_IO13	A16	NVCC_GPIO	GPIO	ALT5	GPIO1_IO13	Input	Keeper
JTAG_MOD	R7	NVCC_JTAG	GPIO	—	JTAG_MOD	Input	100 kΩ pull-up
JTAG_TCK	R9	NVCC_JTAG	GPIO	—	JTAG_TCK	Input	47 kΩ pull-up
JTAG_TDI	R10	NVCC_JTAG	GPIO	—	JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	R8	NVCC_JTAG	GPIO	—	JTAG_TDO	Output	Keeper
JTAG_TMS	T10	NVCC_JTAG	GPIO	—	JTAG_TMS	Input	47 kΩ pull-up
JTAG_TRST_B	T9	NVCC_JTAG	GPIO	—	JTAG_TRST_B	Input	47 kΩ pull-up
KEY_COL0	G20	NVCC_KEY	GPIO	ALT5	GPIO2_IO10	Input	Keeper



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: MAPBGA, THIN PROFILE, 14 X 14 X 1.165 PKG, 0.65 MM PITCH, 400 I/O	DOCUMENT NO: 98ASA00783D REV: A
	STANDARD: NON–JEDEC
	SOT1559–1 17 FEB 2016

Figure 88. 14x14 mm BGA Package Notes

6.5.2 14x14 mm Supplies Contact Assignments and Functional Contact Assignments

Table 118 shows supplies contact assignments for the 14x14 mm package and Table 119 shows the functional contact assignments.

Table 118. 14x14 mm Supplies Contact Assignments

Supply Rail Name	14x14 mm Ball Position(s)	Comments
ADC_VREFH	Y15	ADC high reference voltage
ADC_VREFL	V14	ADC low reference voltage
DRAM_VREF	K4	DDR voltage reference input. Connect to a voltage source that is 50% of NVCC_DRAM.
DRAM_ZQPAD	H2	DDR output buffer driver calibration reference voltage input. Connect DRAM_ZQPAD to an external 240 ohm 1% resistor to Vss.
GPANAIO	P16	Analog output for NXP use only. This output must always be left unconnected.
NVCC_DRAM	G6, H6, J6, K6, L6, M6, N6, P6	Supply input for the DDR I/O interface
NVCC_DRAM_2P5	K7	Supply input for the DDR interface
NVCC_ENET	F6	Supply input for the ENET interfaces
NVCC_GPIO	F15	Supply input for the GPIO interface
NVCC_HIGH	R12	3.3 V Supply input for the dual-voltage I/Os on the SD3 interface
NVCC_JTAG	T9	Supply input for the JTAG interface
NVCC_KEY	G15	Supply input for the Key Pad Port (KPP) interface
NVCC_CSI_LCD1	H15	Supply input for the LCD interface
NVCC_LOW	V13	1.8 V Supply input for the dual-voltage I/Os on the SD3 interface
NVCC_NAND	R6	Supply input for the Raw NAND flash memories interface
NVCC_PLL	U18	Supply input for the PLLs
NVCC_QSPI	F14	Supply input for the QSPI interface
NVCC_RGMII1	F8	Supply input for the RGMII1 interface
NVCC_RGMII2	E11	Supply input for the RGMII2 interface
NVCC_SD1_SD2	F13	Supply input for the SD2 interface
NVCC_SD4	T12	Supply input for the SD4 interface
NVCC_USB_H	V5	Supply input for the USB HSIC interface
NGND_KEL0	T16	Ground
PCIE_VP_CAP	L18	PCIe LDO output. Although this package does not support PCIe, this output requires a 4.7uF capacitor to ground unless the PCIE LDO is disabled.
USB_OTG1_VBUS	W20	VBUS input for USB_OTG1
USB_OTG2_VBUS	U17	VBUS input for USB_OTG2

Table 119. 14 x 14 Functional Contact Assignments (continued)

Ball Name	14x14 Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
JTAG_TRST_B	V8	NVCC_JTAG	GPIO	—	JTAG_TRST_B	Input	47 kΩ pull-up
KEY_COL0	F18	NVCC_KEY	GPIO	ALT5	GPIO2_IO10	Input	Keeper
KEY_COL1	F19	NVCC_KEY	GPIO	ALT5	GPIO2_IO11	Input	Keeper
KEY_COL2	G17	NVCC_KEY	GPIO	ALT5	GPIO2_IO12	Input	Keeper
KEY_COL3	E20	NVCC_KEY	GPIO	ALT5	GPIO2_IO13	Input	Keeper
KEY_COL4	E19	NVCC_KEY	GPIO	ALT5	GPIO2_IO14	Input	Keeper
KEY_ROW0	F16	NVCC_KEY	GPIO	ALT5	GPIO2_IO15	Input	Keeper
KEY_ROW1	E18	NVCC_KEY	GPIO	ALT5	GPIO2_IO16	Input	Keeper
KEY_ROW2	F20	NVCC_KEY	GPIO	ALT5	GPIO2_IO17	Input	Keeper
KEY_ROW3	G20	NVCC_KEY	GPIO	ALT5	GPIO2_IO18	Input	Keeper
KEY_ROW4	H19	NVCC_KEY	GPIO	ALT5	GPIO2_IO19	Input	Keeper
LCD1_CLK	L19	NVCC_LCD1	GPIO	ALT5	GPIO3_IO00	Input	Keeper
LCD1_DATA00	M19	NVCC_LCD1	GPIO	ALT5	GPIO3_IO01	Input	Keeper
LCD1_DATA01	L17	NVCC_LCD1	GPIO	ALT5	GPIO3_IO02	Input	Keeper
LCD1_DATA02	M18	NVCC_LCD1	GPIO	ALT5	GPIO3_IO03	Input	Keeper
LCD1_DATA03	N20	NVCC_LCD1	GPIO	ALT5	GPIO3_IO04	Input	Keeper
LCD1_DATA04	N19	NVCC_LCD1	GPIO	ALT5	GPIO3_IO05	Input	Keeper
LCD1_DATA05	M15	NVCC_LCD1	GPIO	ALT5	GPIO3_IO06	Input	Keeper
LCD1_DATA06	M16	NVCC_LCD1	GPIO	ALT5	GPIO3_IO07	Input	Keeper
LCD1_DATA07	J19	NVCC_LCD1	GPIO	ALT5	GPIO3_IO08	Input	Keeper
LCD1_DATA08	K18	NVCC_LCD1	GPIO	ALT5	GPIO3_IO09	Input	Keeper
LCD1_DATA09	L15	NVCC_LCD1	GPIO	ALT5	GPIO3_IO10	Input	Keeper
LCD1_DATA10	K19	NVCC_LCD1	GPIO	ALT5	GPIO3_IO11	Input	Keeper
LCD1_DATA11	L16	NVCC_LCD1	GPIO	ALT5	GPIO3_IO12	Input	Keeper
LCD1_DATA12	K15	NVCC_LCD1	GPIO	ALT5	GPIO3_IO13	Input	Keeper
LCD1_DATA13	K16	NVCC_LCD1	GPIO	ALT5	GPIO3_IO14	Input	Keeper
LCD1_DATA14	K17	NVCC_LCD1	GPIO	ALT5	GPIO3_IO15	Input	Keeper
LCD1_DATA15	H16	NVCC_LCD1	GPIO	ALT5	GPIO3_IO16	Input	Keeper
LCD1_DATA16	H20	NVCC_LCD1	GPIO	ALT5	GPIO3_IO17	Input	Keeper
LCD1_DATA17	M20	NVCC_LCD1	GPIO	ALT5	GPIO3_IO18	Input	Keeper
LCD1_DATA18	L20	NVCC_LCD1	GPIO	ALT5	GPIO3_IO19	Input	Keeper