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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 22x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f303ret7

3 Functional overview

3.1 ARM® Cortex®-M4 core with FPU with embedded Flash and SRAM

The ARM® Cortex®-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 32-bit RISC processor with FPU features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allows efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32F303xD/E family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32F303xD/E family devices.

3.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU manage up to 8 protection areas that are further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS detects it and takes action. In an RTOS environment, the kernel dynamically updates the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.3 Embedded Flash memory

All STM32F303xD/E devices feature 384/512 Kbyte of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

Table 9. STM32F303xD/E SPI/I^2S implementation

SPI features(1)	SPI1	SPI2	SPI3	SPI4
Hardware CRC calculation	X	X	X	X
Rx/Tx FIFO	X	X	X	X
NSS pulse mode	X	X	X	X
I^2S mode	-	X	X	-
TI mode	X	X	X	X

1. X = supported.

3.24 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

3.25 Universal serial bus (USB)

The STM32F303xD/E embeds a full-speed USB device peripheral compliant with the USB specification version 2.0. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 Kbyte (256 bytes are used for CAN peripheral if enabled) and suspend/resume support.

The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

3.26 Infrared transmitter

The STM32F303xD/E devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

Table 13. STM32F303xD/E pin definitions (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	UFBGA100	WLCSP100	LQFP144						
11	18	K2	H10	29	PC3	I/O	TTa	-	EVENTOUT, TIM1_CH4, TIM1_BKIN2	ADC12_IN9
12	20	K1	H8	30	VSSA	S	-	(1)	-	-
-	-	-	-	31	VREF-	S	-	(1)	-	-
-	21	M1	J8	32	VREF+(4)	S	-	-	-	-
13	22	L1	J10	33	VDDA	S	-	-	-	-
14	23	L2	H9	34	PA0	I/O	TTa	-	TIM2_CH1/TIM2_ETR, TSC_G1_IO1, USART2_CTS, COMP1_OUT, TIM8_BKIN, TIM8_ETR, EVENTOUT	ADC1_IN1(3), COMP1_INM, RTC_TAMP2, WKUP1
15	24	M2	J9	35	PA1	I/O	TTa	-	RTC_REFIN, TIM2_CH2, TSC_G1_IO2, USART2_RTS, TIM15_CH1N, EVENTOUT	ADC1_IN2(3), COMP1_INP, OPAMP1_VINP, OPAMP3_VINP
16	25	K3	F7	36	PA2	I/O	TTa	(5)	TIM2_CH3, TSC_G1_IO3, USART2_TX, COMP2_OUT, TIM15_CH1, EVENTOUT	ADC1_IN3(3), COMP2_INM, OPAMP1_VOUT
17	26	L3	G7	37	PA3	I/O	TTa	-	TIM2_CH4, TSC_G1_IO4, USART2_RX, TIM15_CH2, EVENTOUT	ADC1_IN4(3), OPAMP1_VINM OPAMP,1_VINP
18	27	D3	K9, K10	38	VSS	S	-	-	-	-
19	28	H3	K8	39	VDD	S	-	(1)	-	-
20	29	M3	J7	40	PA4	I/O	TTa	(5)	TIM3_CH2, TSC_G2_IO1, SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_CK, EVENTOUT	ADC2_IN1(3), DAC1_OUT1, COMP1_INM, COMP2_INM, COMP3_INM, COMP4_INM, COMP5_INM, COMP6_INM, COMP7_INM, OPAMP4_VINP

Table 13. STM32F303xD/E pin definitions (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	UFBGA100	WLCSP100	LQFP144						
45	71	A12	D1	104	PA12	I/O	FT	-	TIM16_CH1, I2SCKIN, TIM1_CH2N, USART1_RTS, COMP2_OUT, CAN_TX, TIM4_CH2, TIM1_ETR, EVENTOUT	USB_DP
46	72	A11	E3	105	PA13	I/O	FT	-	SWDIO-JTMS, TIM16_CH1N, TSC_G4_IO3, IR-OUT, USART3_CTS, TIM4_CH3, EVENTOUT	-
-	-	-	-	106	PH2	I/O	FT	(1)	EVENTOUT	-
47	74	F11	A1, A2, B1	107	VSS	S	-	-	-	-
48	75	G11	D2	108	VDD	S	-	-	-	-
49	76	A10	C2	109	PA14	I/O	FTf	-	SWCLK-JTCK, TSC_G4_IO4, I2C1_SDA, TIM8_CH2, TIM1_BKIN, USART2_TX, EVENTOUT	-
50	77	A9	B2	110	PA15	I/O	FTf	-	JTDI, TIM2_CH1/TIM2_ETR, TIM8_CH1, TSC_SYNC, I2C1_SCL, SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_RX, TIM1_BKIN, EVENTOUT	-
51	78	B11	E4	111	PC10	I/O	FT	-	EVENTOUT, TIM8_CH1N, UART4_TX, SPI3_SCK/I2S3_CK, USART3_TX	-
52	79	C10	D3	112	PC11	I/O	FT	-	EVENTOUT, TIM8_CH2N, UART4_RX, SPI3_MISO/I2S3ext_SD, USART3_RX	-

Table 14. STM32F303xD/E alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3/TIM8/20/15/GPCOMP7/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/TIM8/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP3/5/6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port A	PA0	-	TIM2_CH1/TIM2_ETR	-	TSC_G1_IO1	-	-	-	USART2_CTS	COMP1_OUT	TIM8_BKIN	TIM8_ETR	-	-	-	-	EVENT OUT
	PA1	RTC_REFIN	TIM2_CH2	-	TSC_G1_IO2	-	-	-	USART2_RTS	-	TIM15_CH1N	-	-	-	-	-	EVENT OUT
	PA2	-	TIM2_CH3	-	TSC_G1_IO3	-	-	-	USART2_TX	COMP2_OUT	TIM15_CH1	-	-	-	-	-	EVENT OUT
	PA3	-	TIM2_CH4	-	TSC_G1_IO4	-	-	-	USART2_RX	-	TIM15_CH2	-	-	-	-	-	EVENT OUT
	PA4	-		TIM3_CH2	TSC_G2_IO1	-	SPI1_NSS	SPI3_NSS/I2S3_WS	USART2_CK	-	-	-	-	-	-	-	EVENT OUT
	PA5	-	TIM2_CH1/TIM2_ETR	-	TSC_G2_IO2	-	SPI1_SCK	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA6	-	TIM16_CH1	TIM3_CH1	TSC_G2_IO3	TIM8_BKIN	SPI1_MISO	TIM1_BKIN	-	COMP1_OUT	-	-	-	-	-	-	EVENT OUT
	PA7	-	TIM17_CH1	TIM3_CH2	TSC_G2_IO4	TIM8_CH1N	SPI1_MOSI	TIM1_CH1N	-	-	-	-	-	-	-	-	EVENT OUT
	PA8	MCO	-	-	I2C3_SCL	I2C2_SMBAL	I2S2_MCK	TIM1_CH1	USART1_CK	COMP3_OUT	-	TIM4_ETR	-	-	-	-	EVENT OUT
	PA9	-	-	I2C3_SMBAL	TSC_G4_IO1	I2C2_SCL	I2S3_MCK	TIM1_CH2	USART1_TX	COMP5_OUT	TIM15_BKIN	TIM2_CH3	-	-	-	-	EVENT OUT

Table 14. STM32F303xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM12/3/4/8/20/15/GPCOMP1	I2C3/TIM8/20/15/GPCOMP7/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/TIM8/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP3/5/6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port G	PG5	-	EVENT OUT	TIM20_ETR	-	-	-	-	-	-	-	-	-	FMC_A15	-	-	-
	PG6	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_INT2	-	-	-
	PG7	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_INT3	-	-	-
	PG8	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PG9	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_NE2/FMC_NCE3	-	-	-
	PG10	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_NCE4_1/FMC_NE3	-	-	-
	PG11	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_NCE4_2	-	-	-
	PG12	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_NE4	-	-	-
	PG13	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A24	-	-	-
	PG14	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A25	-	-	-
	PG15	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Note: The total current consumption is the sum of I_{DD} and I_{DDA}.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz,1 wait state from 24 to 48 MHz and 2 wait states from 48 to 72 MHz)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK2} = f_{HCLK}$ and $f_{PCLK1} = f_{HCLK/2}$
- When f_{HCLK} > 8 MHz, the PLL is ON and the PLL input is equal to HSI/2 (4 MHz) or HSE (8 MHz) in bypass mode.

The parameters given in *Table 25* to *Table 29* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 19*.

Table 25. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6V

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, executing from Flash	External clock (HSE bypass)	72 MHz	66.4	76.5	76.9	77.4	33.0	37.2	38.1	38.9	mA
			64 MHz	59.8	66.4	67.7	68.6	29.7	33.5	34.3	35.0	
			48 MHz	47.3	53.7	53.8	55.1	23.2	26.2	27.1	28.0	
			32 MHz	33.3	36.8	37.4	38.5	16.8	19.8	20.6	21.4	
			24 MHz	26.0	29.4	30.0	31.2	13.5	16.6	17.4	18.6	
			8 MHz	10.7	13.8	14.4	15.3	6.63	10.2	10.5	11.2	
			1 MHz	4.27	7.47	8.13	8.90	3.78	7.40	7.70	8.50	
		Internal clock (HSI)	64 MHz	55.6	59.6	62.8	63.2	29.4	33.1	34.5	35.0	
			48 MHz	43.6	47.0	49.2	50.1	23.1	26.2	27.1	28.0	
			32 MHz	30.8	33.6	35.3	35.8	16.7	19.8	20.6	21.5	
			24 MHz	24.0	28.0	28.2	29.7	13.5	16.5	17.5	18.4	
			8 MHz	10.5	13.6	14.7	15.2	6.63	9.74	10.6	11.2	
I_{DD}	Supply current in Run mode, executing from RAM	External clock (HSE bypass)	72 MHz	66.2	76.2(2)	76.7	77.2(2)	32.8	36.9(2)	37.7	38.5(2)	
			64 MHz	59.6	66.2	67.6	68.4	29.3	33.1	33.9	34.4	
			48 MHz	47.0	53.4	53.6	54.9	22.4	25.6	26.2	27.2	
			32 MHz	33.0	36.6	37.2	38.1	16.0	19.0	19.5	20.4	
			24 MHz	25.6	29.0	29.5	30.6	12.8	15.7	16.3	17.6	
			8 MHz	10.3	13.4	13.8	14.7	6.40	9.48	9.93	10.90	

Table 25. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6V (continued)

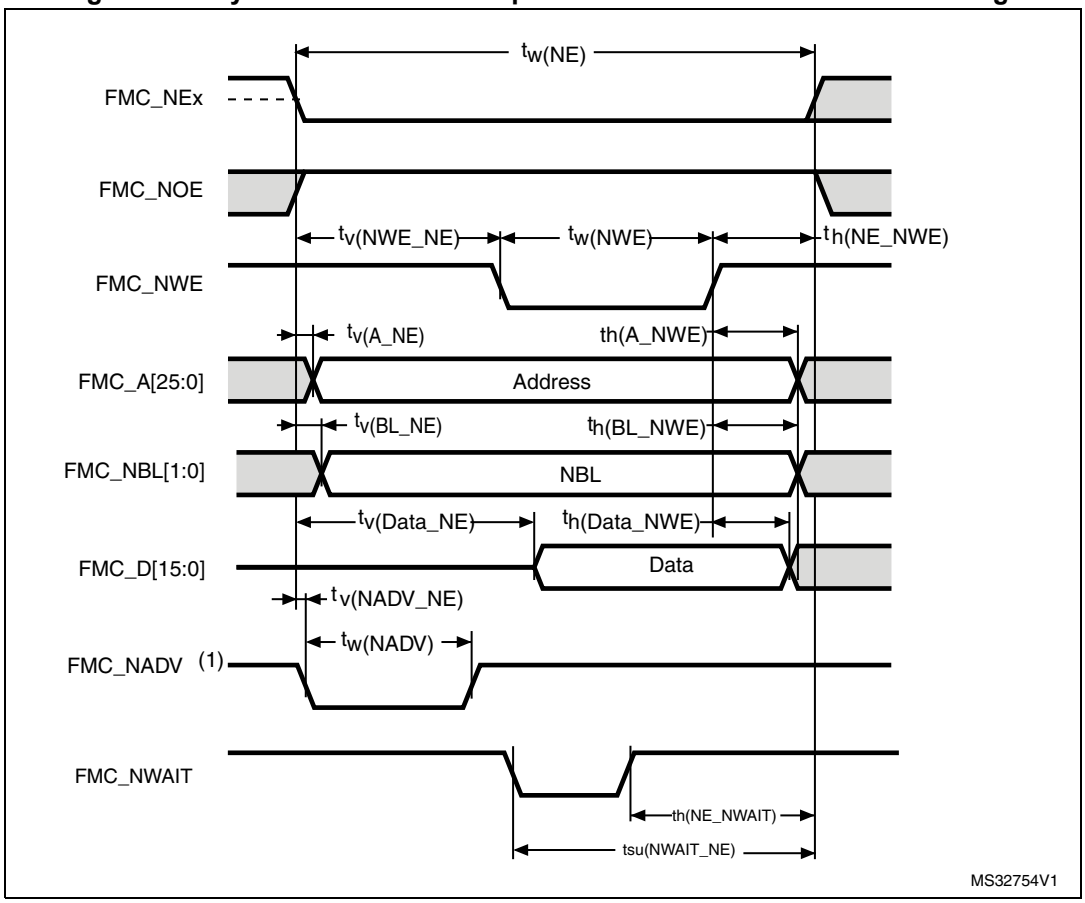
Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, executing from RAM	External clock (HSE bypass)	1 MHz	3.92	7.06	7.54	8.60	3.42	6.53	7.05	8.10	mA
		Internal clock (HSI)	64 MHz	55.4	59.2	62.5	62.9	29.1	32.7	34.0	34.6	
			48 MHz	43.1	46.7	49.0	49.9	22.8	26.1	26.8	27.8	
			32 MHz	30.5	33.2	35.0	35.5	15.8	18.8	19.5	20.9	
			24 MHz	23.8	27.8	27.9	29.2	12.6	15.6	16.3	17.5	
			8 MHz	9.85	13.1	14.1	14.6	6.20	9.37	10.3	10.7	
I_{DD}	Supply current in Sleep mode, executing from Flash or RAM	External clock (HSE bypass)	72 MHz	48.8	53.5(2)	53.6	54.0(2)	7.60	8.20(2)	8.50	9.00(2)	
			64 MHz	43.5	48.6	49.1	49.3	6.90	7.50	7.80	8.00	
			48 MHz	33.6	38.1	40.0	41.3	5.30	5.80	6.00	6.40	
			32 MHz	24.3	27.5	28.1	29.3	3.80	4.10	4.40	4.70	
			24 MHz	18.6	21.9	22.4	22.6	2.90	3.30	3.40	3.90	
			8 MHz	8.24	11.27	11.79	12.70	1.36	1.74	1.85	2.00	
			1 MHz	3.64	6.72	7.36	8.30	0.79	1.17	1.26	1.35	
		Internal clock (HSI)	64 MHz	39.7	43.9	45.5	45.8	6.70	7.30	7.40	7.70	
			48 MHz	30.4	33.9	35.3	36.5	5.10	5.60	5.70	6.10	
			32 MHz	21.9	25.8	26.2	26.7	3.60	4.10	4.20	4.50	
			24 MHz	17.0	20.2	21.5	21.7	2.98	3.41	3.46	3.57	
			8 MHz	7.81	11.0	11.7	12.4	1.41	1.74	1.81	1.87	

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production with code executing from RAM.

Table 26. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run mode, code executing from Flash or RAM	HSE bypass	72 MHz	220	243	255	260	241	264	281	287	µA
			64 MHz	194	215	226	231	212	233	248	254	
			48 MHz	145	164	172	176	158	176	187	192	
			32 MHz	100	116	121	124	108	123	130	134	
			24 MHz	78	92	96	98	85	97	102	105	
			8 MHz	1.9	3.1	3.6	4.4	2.5	3.7	4.4	5.5	

Figure 21. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 47. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	3THCLK-1	3THCLK+2	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	THCLK+0.5	THCLK+1	
$t_{w(NWE)}$	FMC_NWE low time	THCLK-2	THCLK+1	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	THCLK-0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	THCLK-1.5	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	1	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	THCLK-0.5	-	
$t_{v(Data\_NE)}$	Data to FMC_NEx low to Data valid	-	THCLK+ 3	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	THCLK+0.5	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	2.5	
$t_{w(NADV)}$	FMC_NADV low time	-	THCLK+2	

1. Based on characterization, not tested in production.

Table 53. Synchronous multiplexed NOR/PSRAM read timings(1) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	ns
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	4	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	6	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. Based on characterization, not tested in production.

Figure 25. Synchronous multiplexed PSRAM write timings

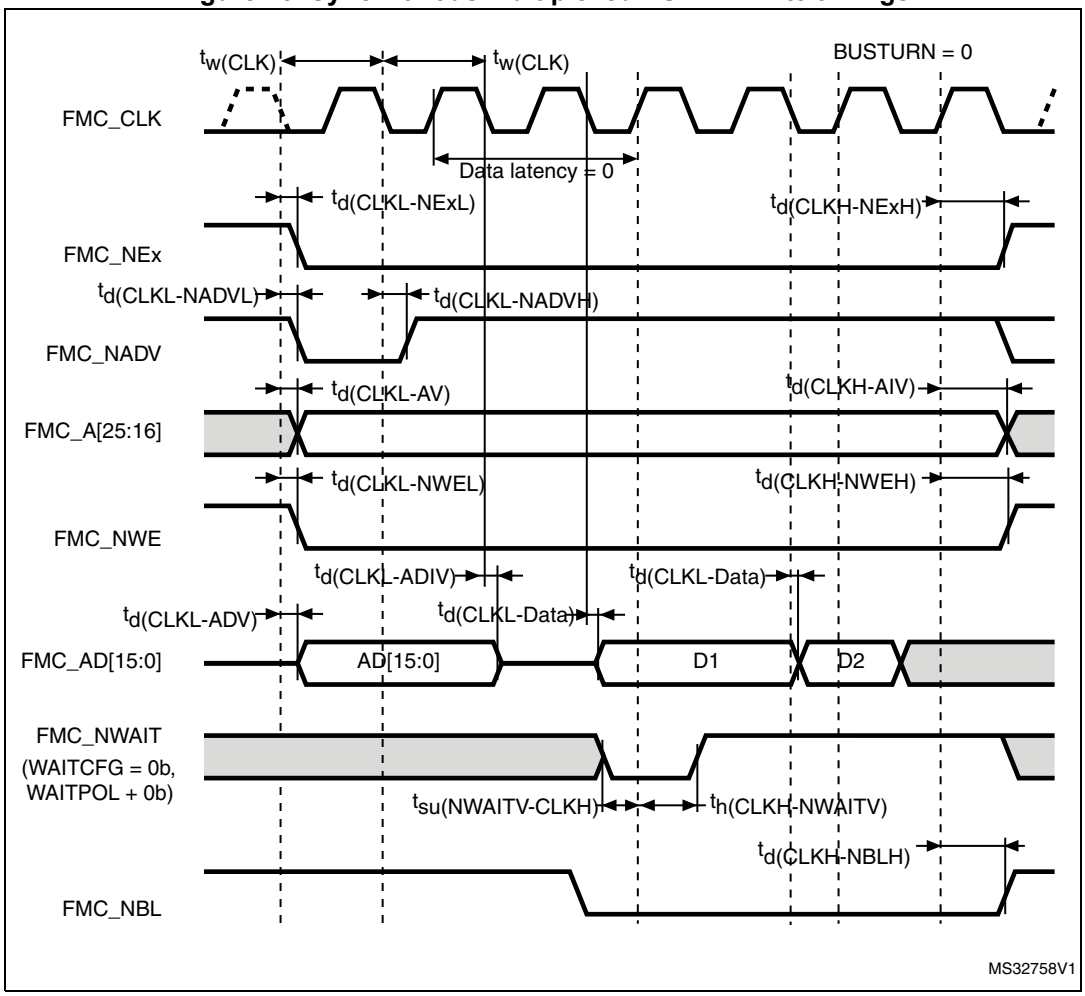


Figure 26. Synchronous non-multiplexed NOR/PSRAM read timings

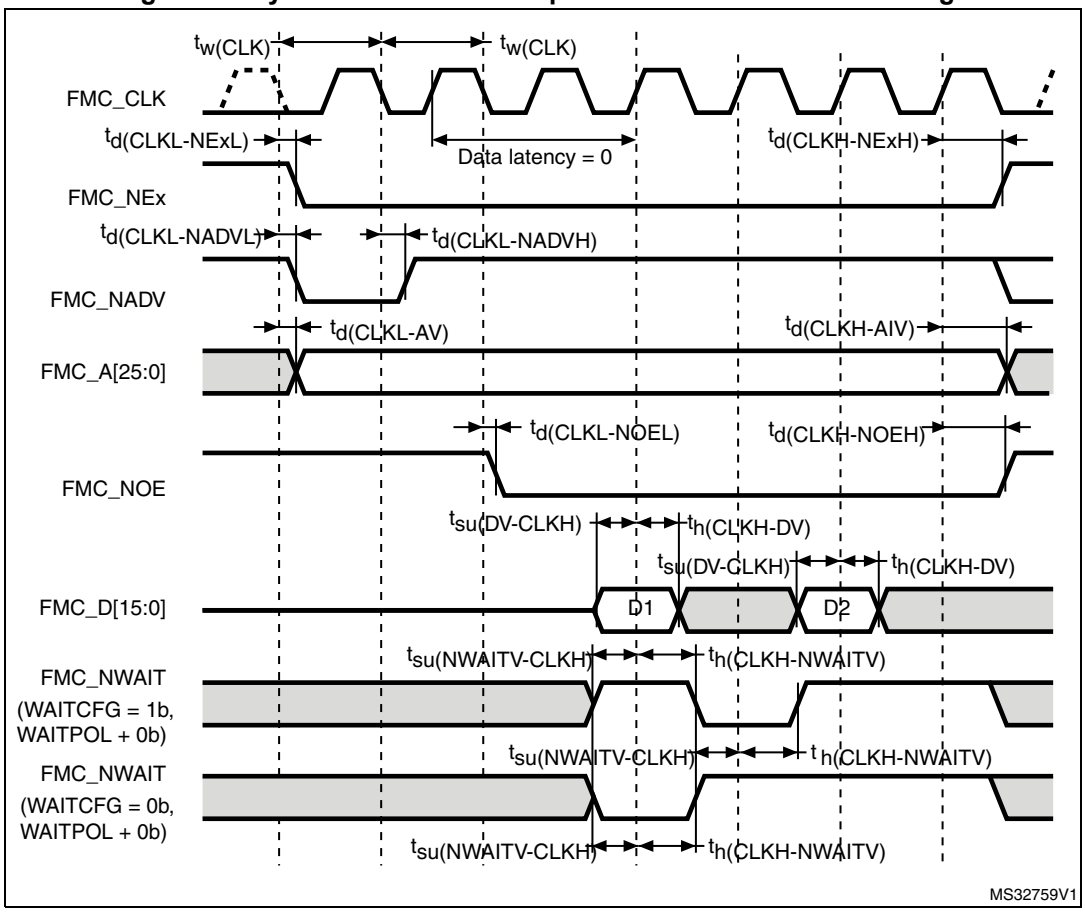


Table 55. Synchronous non-multiplexed NOR/PSRAM read timings(1)

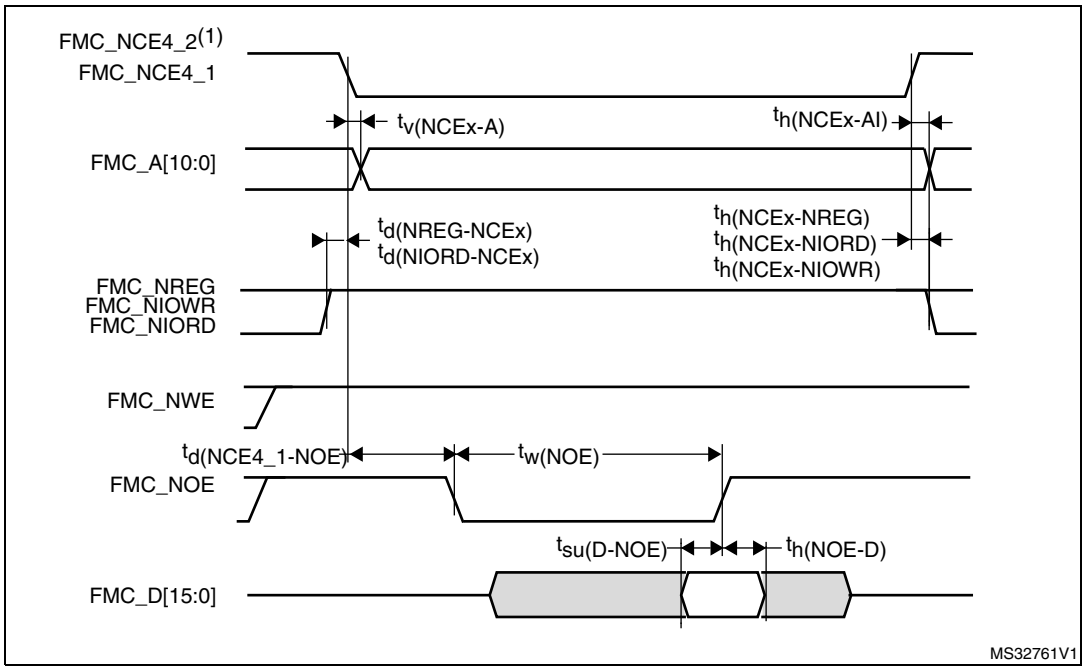
Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	2THCLK-1	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	THCLK+1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	7	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	2.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	7	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	THCLK	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	6	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	THCLK+1	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	3.5	-	

Table 57. Switching characteristics for PC Card/CF read and write cycles in attribute/common space(1)

Symbol	Parameter	Min	Max	Unit
$t_{v(NCEx-A)}$	FMC_Ncex low to FMC_Ay valid	-	0	ns
$t_{h(NCEx\_AI)}$	FMC_NCEx high to FMC_Ax invalid	2.5	-	
$t_{d(NREG-NCEx)}$	FMC_NCEx low to FMC_NREG valid	-	2	
$t_{h(NCEx-NREG)}$	FMC_NCEx high to FMC_NREG invalid	0	-	
$t_{d(NCEx-NWE)}$	FMC_NCEx low to FMC_NWE low	-	5THCLK+2	
$t_{w(NWE)}$	FMC_NWE low width	8THCLK	8THCLK+0.5	
$t_{d(NWE\_NCEx)}$	FMC_NWE high to FMC_NCEx high	5THCLK-1	-	
$t_{v\ (NWE-D)}$	FMC_NWE low to FMC_D[15:0] valid	-	5	
$t_{h\ (NWE-D)}$	FMC_NWE high to FMC_D[15:0] invalid	4THCLK-1	-	
$t_{d\ (D-NWE)}$	FMC_D[15:0] valid before FMC_NWE high	13THCLK-3	-	
$t_{d(NCEx-NOE)}$	FMC_NCEx low to FMC_NOE low	-	5THCLK+2	
$t_{w(NOE)}$	FMC_NOE low width	8THCLK-1	8THCLK+2	
$t_{d(NOE\_NCEx)}$	FMC_NOE high to FMC_NCEx high	5THCLK-1	-	
$t_{su\ (D-NOE)}$	FMC_D[15:0] valid data before FMC_NOE high	THCLK+2	-	
$t_{h(NOE-D)}$	FMC_N0E high to FMC_D[15:0] invalid	0	-	

1. Based on characterization, not tested in production.

Figure 28. PC Card/CompactFlash controller waveforms for common memory read access



1. FMC_NCE4_2 remains high (inactive during 8-bit access.

Figure 29. PC Card/CompactFlash controller waveforms for common memory write access

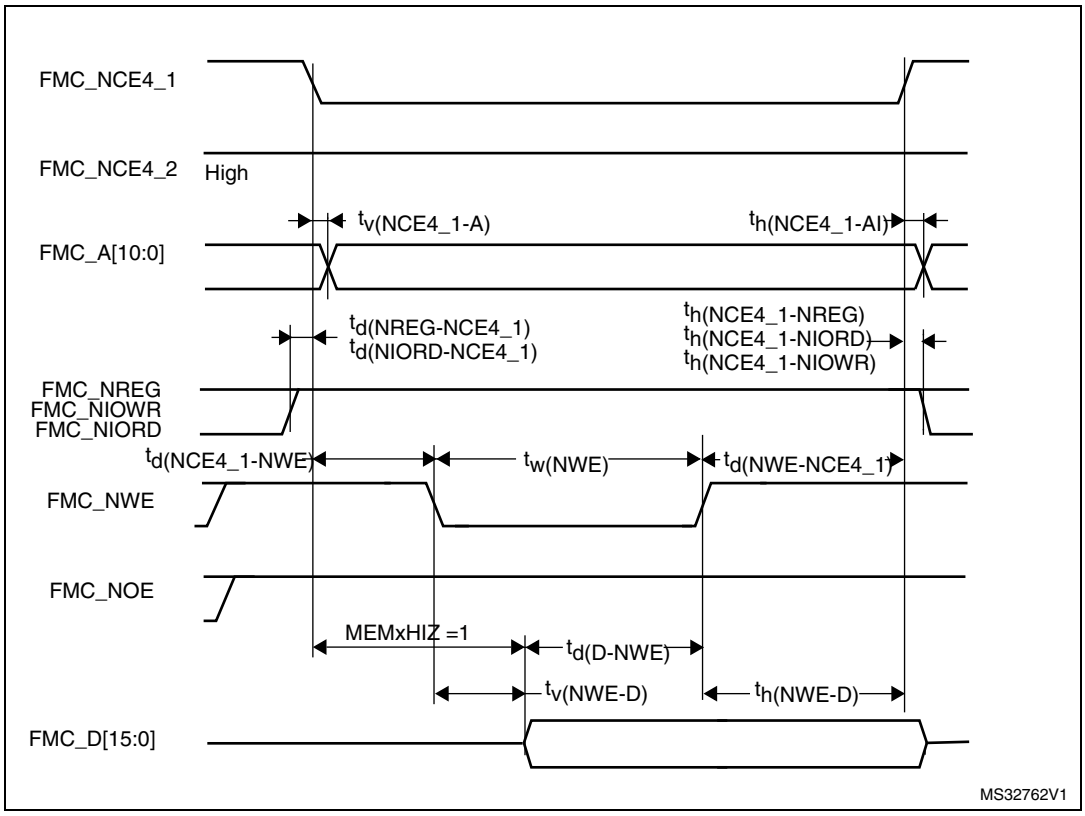


Table 79. ADC characteristics (continued)

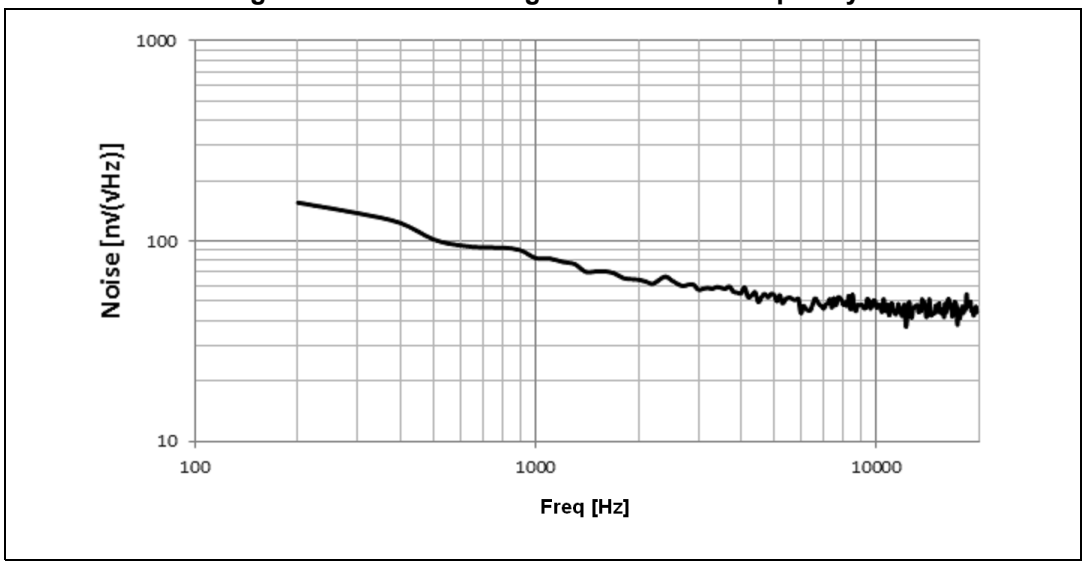
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{REF}	Current on VREF+ pin (see *Figure 49*)	Single-ended mode, 5 MSPS	-	104	139	µA
		Single-ended mode, 1 MSPS	-	20.4	37	
		Single-ended mode, 200 KSPS	-	3.3	11.3	
		Differential mode, 5 MSPS	-	174	235	
		Differential mode, 1 MSPS	-	34.6	52.6	
		Differential mode, 200 KSPS	-	6	13.6	
V_{REF+}	Positive reference voltage	-	2	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	-	0.14	-	72	MHz
f_S(1)	Sampling rate	Resolution = 12 bits, Fast Channel	0.01	-	5.14	MSPS
		Resolution = 10 bits, Fast Channel	0.012	-	6	
		Resolution = 8 bits, Fast Channel	0.014	-	7.2	
		Resolution = 6 bits, Fast Channel	0.0175	-	9	
f_{TRIG}(1)	External trigger frequency	f_{ADC} = 72 MHz Resolution = 12 bits	-	-	5.14	MHz
		Resolution = 12 bits	-	-	14	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(2)	-	0	-	V_{REF+}	V
R_{AIN}(1)	External input impedance	-	-	-	100	kΩ
C_{ADC}(1)	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}(1)	Power-up time	-	0	0	1	µs
t_{CAL}(1)	Calibration time	f_{ADC} = 72 MHz	1.56			µs
		-	112			$1/f_{ADC}$
t_{latr}(1)	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2	$1/f_{ADC}$
		CKMODE = 10	-	-	2.25	$1/f_{ADC}$
		CKMODE = 11	-	-	2.125	$1/f_{ADC}$
$t_{latrinj}$(1)	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3	$1/f_{ADC}$
		CKMODE = 10	-	-	3.25	$1/f_{ADC}$
		CKMODE = 11	-	-	3.125	$1/f_{ADC}$

Table 80. Maximum ADC R_{AIN} (1) (continued)

Resolution	Sampling cycle @ 72 MHz	Sampling time [ns] @ 72 MHz	R_{AIN} max (kΩ)		
			Fast channels(2)	Slow channels	Other channels(3)
8 bits	1.5	20.83	0.150	NA	0.039
	2.5	34.72	0.390	0.180	0.180
	4.5	62.50	0.820	0.560	0.470
	7.5	104.17	1.50	1.20	1.00
	19.5	270.83	3.90	3.30	2.70
	61.5	854.17	12.00	12.00	8.20
	181.5	2520.83	39.00	33.00	27.00
	601.5	8354.17	100.00	100.00	82.00
6 bits	1.5	20.83	0.270	0.100	0.150
	2.5	34.72	0.560	0.390	0.330
	4.5	62.50	1.200	0.820	0.820
	7.5	104.17	2.20	1.80	1.50
	19.5	270.83	5.60	4.70	3.90
	61.5	854.17	18.0	15.0	12.0
	181.5	2520.83	56.0	47.0	39.0
	601.5	8354.17	100.00	100.0	100.0

1. Data based on characterization results, not tested in production.
2. All fast channels, expect channels on PA2, PA6, PB1, PB12.
3. Fast channels available on PA2, PA6, PB1, PB12.

Figure 53. OPAMP voltage noise versus frequency



6.3.23 Temperature sensor characteristics

Table 89. TS characteristics

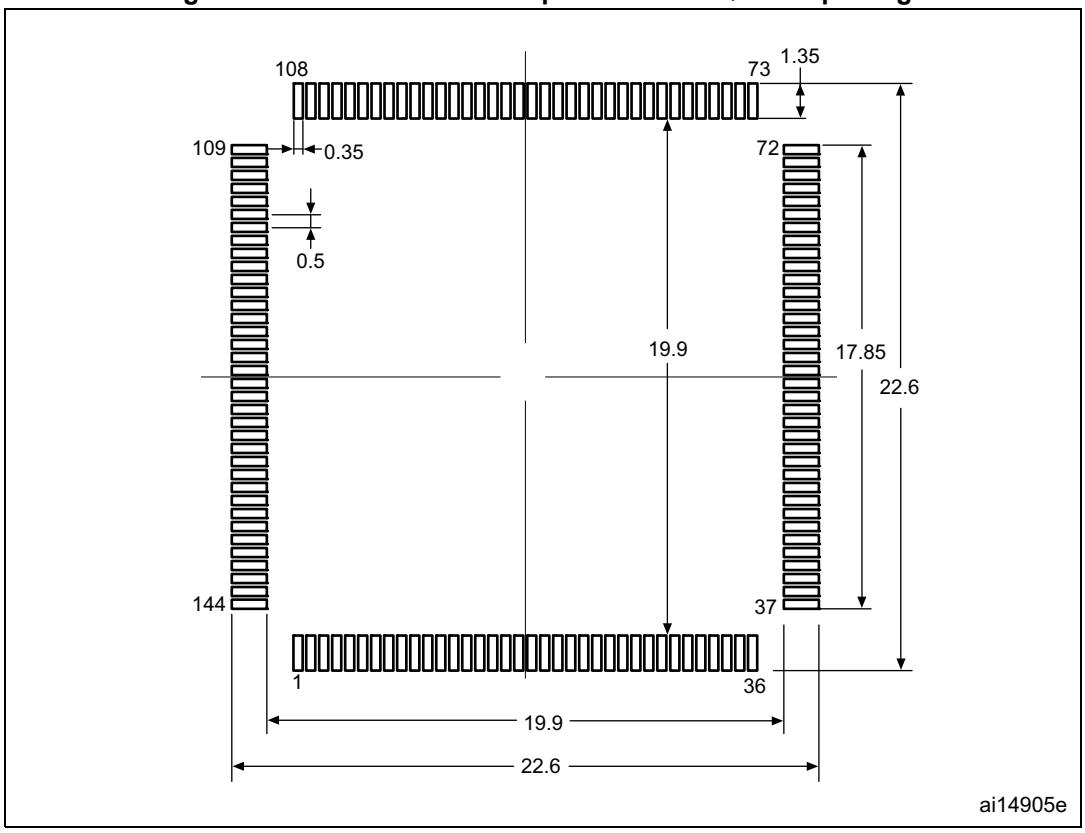
Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(1)	Startup time	4	-	10	µs
T_{S_temp}(1)(2)	ADC sampling time when reading the temperature	2.2	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

Table 90. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

Figure 55. Recommended footprint for the LQFP144 package

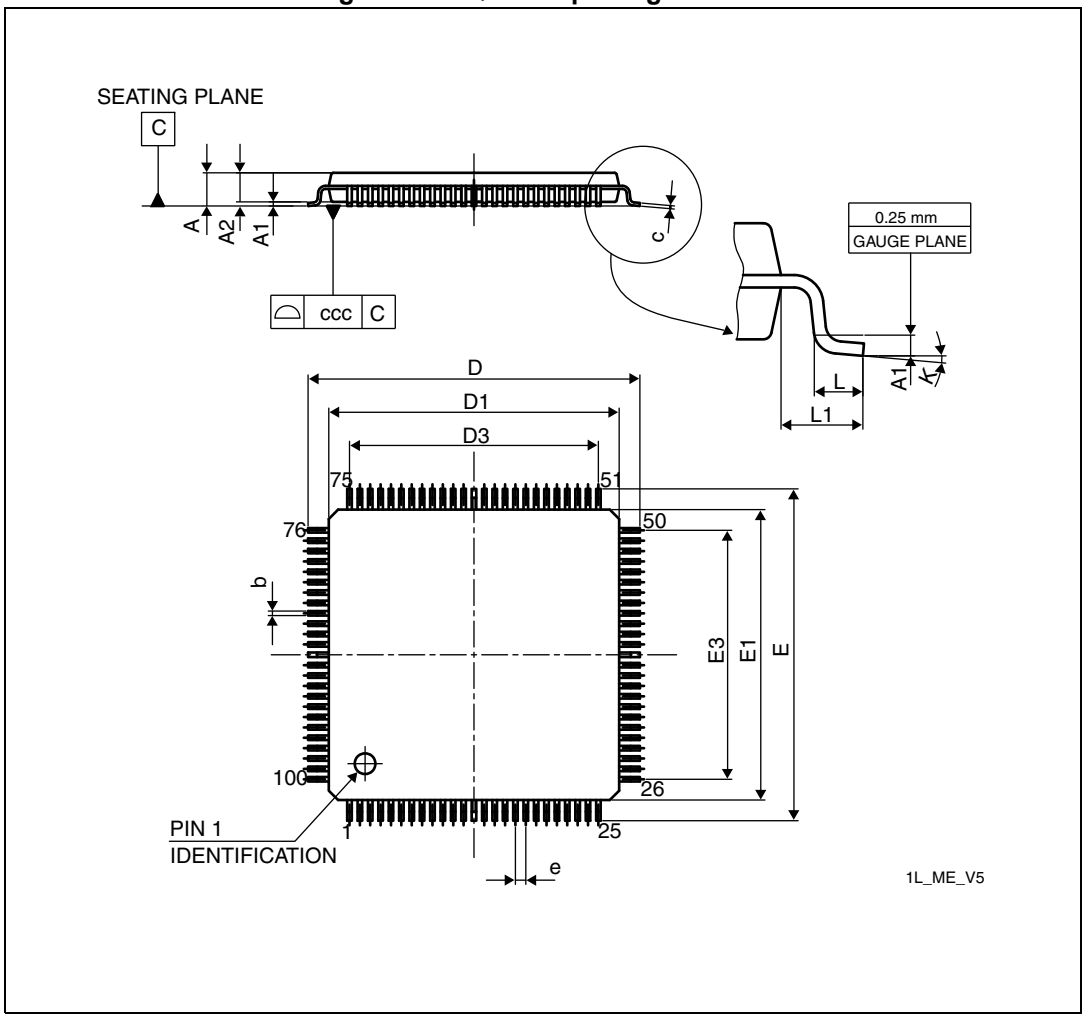


1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

7.4 LQFP100 package information

LQFP100 is a 100-pin, 14 x 14 mm low-profile quad flat package.

Figure 60. LQFP100 package outline



1. Drawing is not to scale.

Table 95. LQPF100 package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378

Table 96. WLCSP100 package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Typ	Min	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.38	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
Ø b[3]	0.22	0.25	0.28	-	0.0098	0.0110
D	4.74	4.775	4.81	-	0.1880	0.1894
E	5.006	5.041	5.076	-	0.1985	0.1998
e	-	0.4	-	-	0.0157	-
e1	-	3.6	-	-	0.1417	-
e2	-	3.6	-	-	0.1417	-
F	-	0.5875	-	-	0.0231	-
G	-	0.7205	-	-	0.0284	-
N	-	100	-	-	3.9370	-
aaa	-	0.1	-	-	0.0039	-
bbb	-	0.1	-	-	0.0039	-
ccc	-	0.1	-	-	0.0039	-
ddd	-	0.05	-	-	0.0020	-
eee	-	0.05	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 64. Recommended footprint for the WLCSP100 package

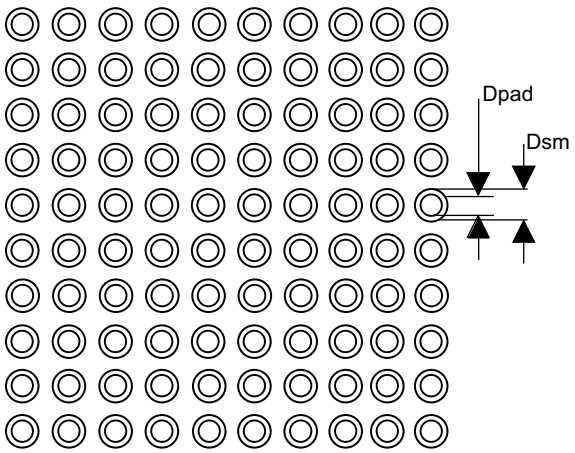


Table 97. WLCSP100 recommended PCB design rules (0.4 mm pitch)

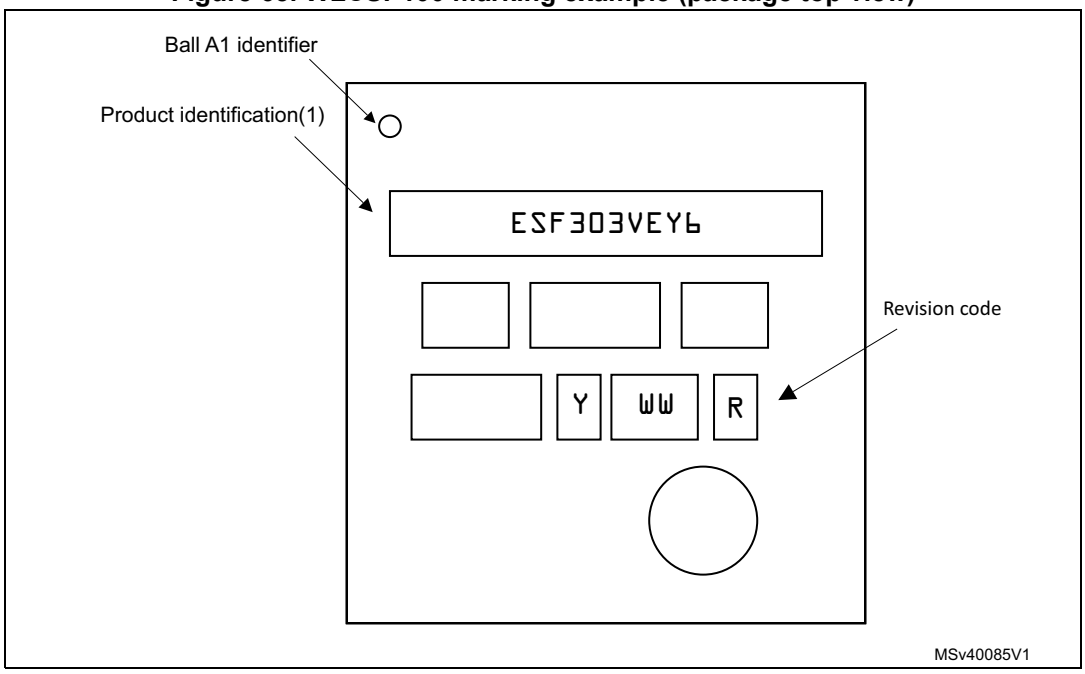
Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm
Stencil thickness	0.1 mm

Device marking for WLCSP100

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 65. WLCSP100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.