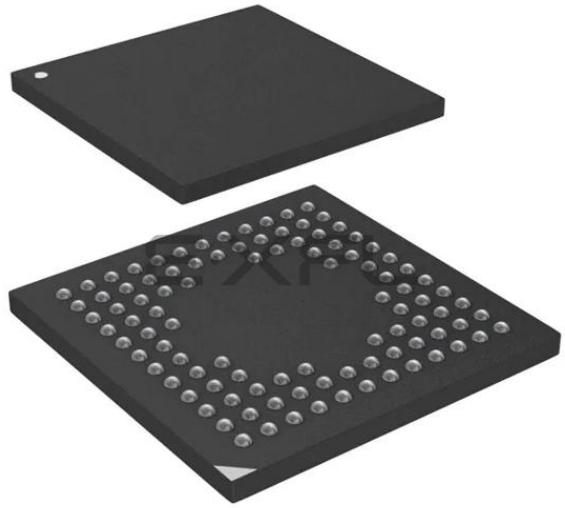

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	84
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 39x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f303vdh6

- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability (for each channel)
- External triggers for conversion
- Input voltage reference VREF+

3.16 Operational amplifier (OPAMP)

The STM32F303xD/E embed four operational amplifiers with external or internal follower routing and PGA capability (or even amplifier and filter capability with external components). When an operational amplifier is selected, an external ADC channel is used to enable output measurement.

The operational amplifier features:

- 8.2 MHz bandwidth
- 0.5 mA output capability
- Rail-to-rail input/output
- In PGA mode, the gain is programmed to be 2, 4, 8 or 16.

3.17 Ultra-fast comparators (COMP)

The STM32F303xD/E devices embed seven ultra-fast rail-to-rail comparators with programmable reference voltage (internal or external) and selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pin
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to *Table 23: Embedded internal reference voltage* for the value and precision of the internal reference voltage.

All comparators can wake up from STOP mode, generate interrupts and breaks for the timers.

3.18 Timers and watchdogs

The STM32F303xD/E include three advanced control timers, up to six general-purpose timers, two basic timers, two watchdog timers and one SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

communication mode and have LIN Master/Slave capability. The USART interfaces can be served by the DMA controller.

3.22 Universal asynchronous receiver transmitter (UART)

The STM32F303xD/E devices have 2 embedded universal asynchronous receiver transmitters (UART4, and UART5). The UART interfaces support IrDA SIR ENDEC, multiprocessor communication mode and single-wire half-duplex communication mode. The UART4 interface can be served by the DMA controller.

Refer to *Table 8* for the features available in all U(S)ART interfaces.

Table 8. USART features

USART modes/features(1)	USART1	USART2	USART3	UART4	UART5
Hardware flow control for modem	X	X	X	-	-
Continuous communication using DMA	X	X	X	X	-
Multiprocessor communication	X	X	X	X	X
Synchronous mode	X	X	X	-	-
Smartcard mode	X	X	X	-	-
Single-wire half-duplex communication	X	X	X	X	X
IrDA SIR ENDEC block	X	X	X	X	X
LIN mode	X	X	X	X	X
Dual clock domain and wakeup from Stop mode	X	X	X	X	X
Receiver timeout interrupt	X	X	X	X	X
Modbus communication	X	X	X	X	X
Auto baud rate detection	X	X	X	-	-
Driver Enable	X	X	X	-	-

1. X = supported.

3.23 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I^2S)

Up to four SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) supporting four different audio standards can operate as master or slave at half-duplex and full duplex communication modes. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by 8-bit programmable linear prescaler. When operating in master mode it can output a clock for an external audio component at 256 times the sampling frequency.

Refer to *Table 9* for the features available in SPI1, SPI2, SPI3 and SPI4.

4 Pinout and pin description

Figure 4. STM32F303xD/E LQFP64 pinout

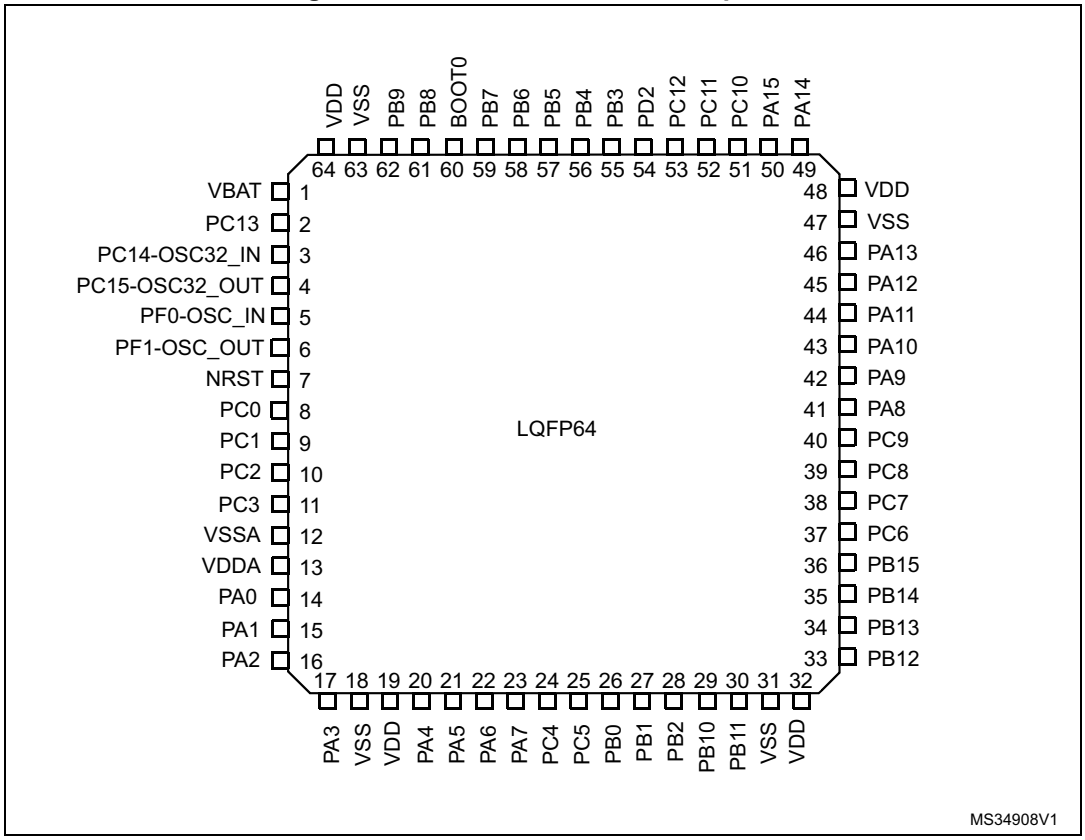
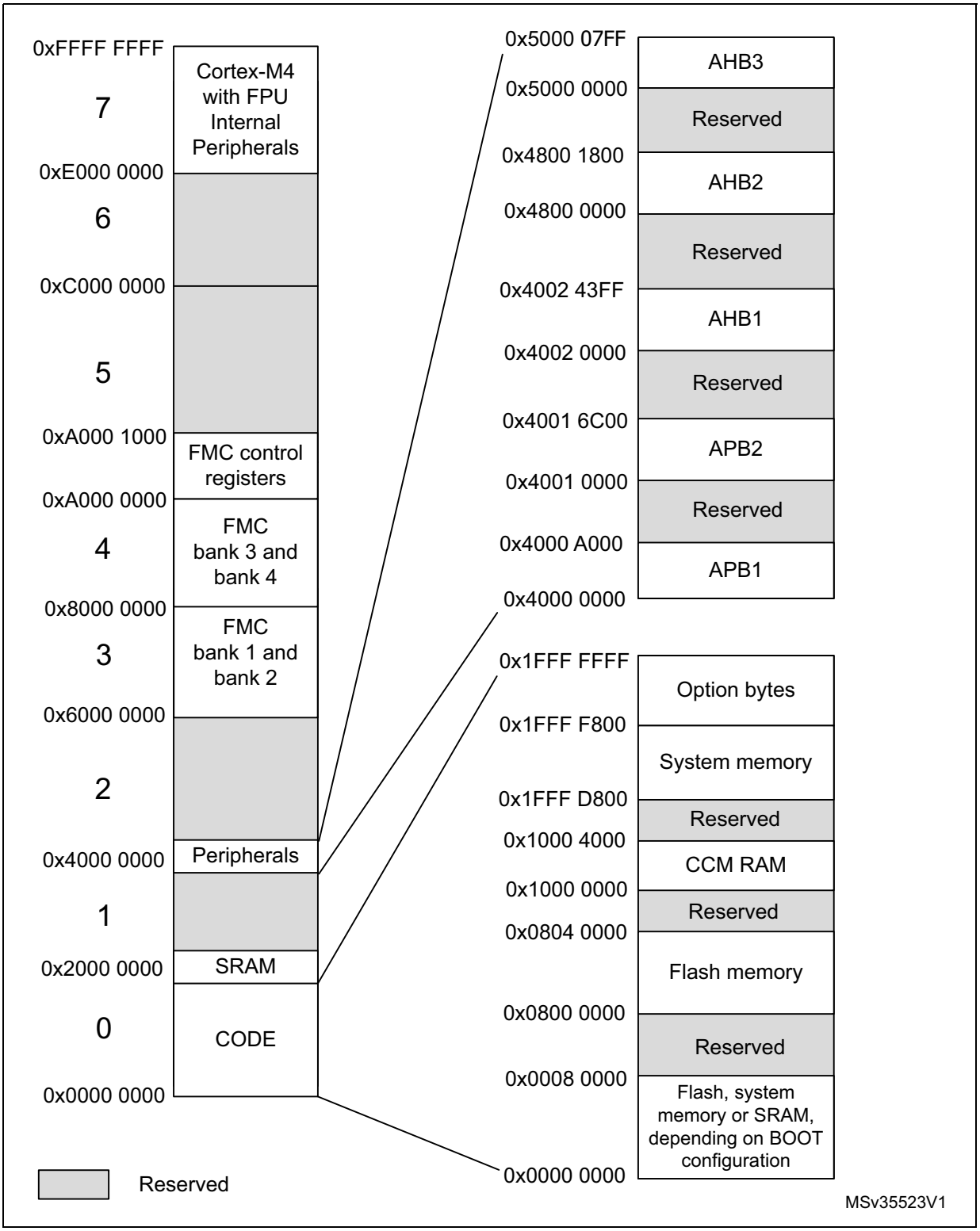


Table 14. STM32F303xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3/TIM8/20/15/GPCOMP7/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/TIM8/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP3/5/6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port E	PE12	-	EVENT OUT	TIM1_CH3N	-	-	SPI4_SCK	-	-	-	-	-	-	FMC_D9	-	-	-
	PE13	-	EVENT OUT	TIM1_CH3	-	-	SPI4_MISO	-	-	-	-	-	-	FMC_D10	-	-	-
	PE14	-	EVENT OUT	TIM1_CH4	-	-	SPI4_MOSI	TIM1_BKIN2	-	-	-	-	-	FMC_D11	-	-	-
	PE15	-	EVENT OUT	TIM1_BKIN	-	-	-	-	USART3_RX	-	-	-	-	FMC_D12	-	-	-
Port F	PF0	-	EVENT OUT	-	-	I2C2_SDA	SPI2_NSS/I2S2_WS	TIM1_CH3N	-	-	-	-	-	-	-	-	-
	PF1	-	EVENT OUT	-	-	I2C2_SCL	SPI2_SCK/I2S2_CK	-	-	-	-	-	-	-	-	-	-
	PF2	-	EVENT OUT	TIM20_CH3	-	-	-	-	-	-	-	-	-	FMC_A2	-	-	-
	PF3	-	EVENT OUT	TIM20_CH4	-	-	-	-	-	-	-	-	-	FMC_A3	-	-	-
	PF4	-	EVENT OUT	COMP1_OUT	TIM20_CH1N	-	-	-	-	-	-	-	-	FMC_A4	-	-	-
	PF5	-	EVENT OUT	TIM20_CH2N	-	-	-	-	-	-	-	-	-	FMC_A5	-	-	-
	PF6	-	EVENT OUT	TIM4_CH4	-	I2C2_SCL	-	-	USART3_RTS	-	-	-	-	FMC_NIORD	-	-	-
	PF7	-	EVENT OUT	TIM20_BKIN	-	-	-	-	-	-	-	-	-	FMC_NREG	-	-	-

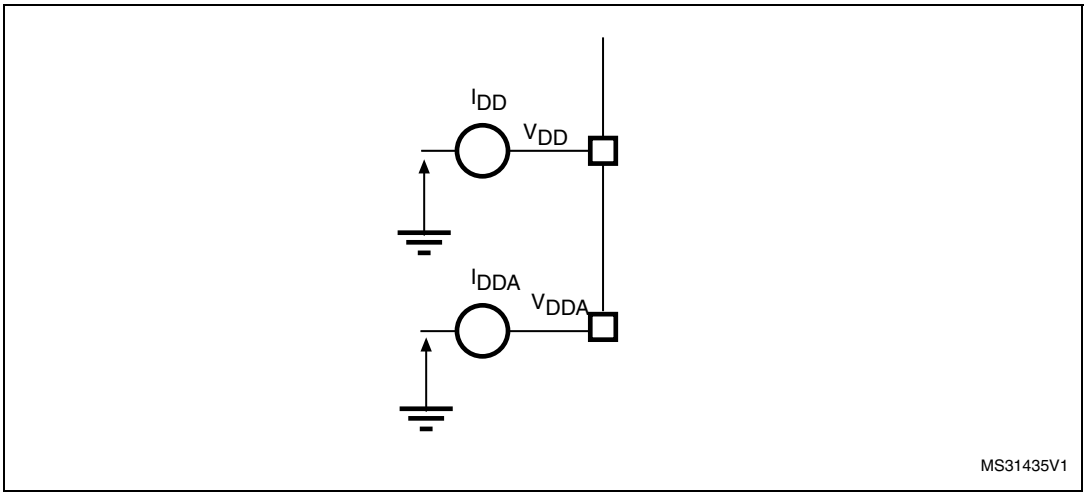
5 Memory mapping

Figure 9. STM32F303xD/E memory map



6.1.7 Current consumption measurement

Figure 13. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 16: Voltage characteristics*, *Table 17: Current characteristics*, and *Table 18: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 16. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{BAT} and V_{DD})	-0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	
V_{REF+}–V_{DDA}(2)	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	
V_{IN}(3)	Input voltage on FT and FTf pins	V_{SS} –0.3	V_{DD} + 4.0	V
	Input voltage on TTa pins	V_{SS} –0.3	4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
	Input voltage on Boot0 pin	0	9	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.13: Electrical sensitivity characteristics*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range. The following relationship must be respected between V_{DDA} and V_{DD}:
V_{DDA} must power on before or at the same time as V_{DD} in the power up sequence.
V_{DDA} must be greater than or equal to V_{DD}.
2. V_{REF+} must be always lower or equal than V_{DDA} ($V_{REF+} \leq V_{DDA}$). If unused then it must be connected to V_{DDA}.
3. V_{IN} maximum must always be respected. Refer to *Table 17: Current characteristics* for the maximum allowed injected current values.

6.3 Operating conditions

6.3.1 General operating conditions

Table 19. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	36	
f_{PCLK2}	Internal APB2 clock frequency	-	0	72	
V_{DD}	Standard operating voltage	-	2	3.6	V
V_{DDA}	Analog operating voltage (OPAMP and DAC not used)	Must have a potential equal to or higher than V_{DD}	2	3.6	V
	Analog operating voltage (OPAMP and DAC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.65	3.6	V
V_{IN}	I/O input voltage	TC I/O	-0.3	V_{DD}+0.3	V
		TTa I/O	-0.3	V_{DDA}+0.3	
		FT and FTf I/O(1)	-0.3	5.5	
		BOOT0	0	5.5	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(2)	LQFP144	-	606	mW
		WLCSP100	-	454	
		LQFP100	-	476	
		UFBGA100	-	339	
		LQFP64	-	435	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	-40	85	°C
		Low power dissipation(3)	-40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	-40	105	°C
		Low power dissipation(3)	-40	125	
T_J	Junction temperature range	6 suffix version	-40	105	°C
		7 suffix version	-40	125	

1. To sustain a voltage higher than V_{DD}+0.3 V, the internal pull-up/pull-down resistors must be disabled.
2. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 7.7: Thermal characteristics*).
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.7: Thermal characteristics*).

Table 22. Programmable voltage detector characteristics (continued)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	V
		Falling edge	2.56	2.68	2.8	
V_{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3	
		Falling edge	2.66	2.78	2.9	
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
IDD(PVD)	PVD current consumption	-	-	0.15	0.26	µA

1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.

6.3.4 Embedded reference voltage

The parameters given in *Table 23* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 19*.

Table 23. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.16	1.2	1.25	V
		–40 °C < T_A < +85 °C	1.16	1.2	1.24(1)	V
$T_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage	-	2.2	-	-	µs
V_{RERINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V ±10 mV	-	-	10(2)	mV
T_{Coeff}	Temperature coefficient	-	-	-	100(2)	ppm/°C

1. Data based on characterization results, not tested in production.
2. Guaranteed by design, not tested in production.

Table 24. Internal reference voltage calibration values

Calibration value name	Description	Memory address
V_{REFINT_CAL}	Raw data acquired at temperature of 30 °C V_{DDA}= 3.3 V	0x1FFF F7BA - 0x1FFF F7BB

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 13: Current consumption measurement scheme*.

Table 45. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	2THCLK– 1	2THCLK+1	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	1	
$t_{w(NOE)}$	FMC_NOE low time	2THCLK	2THCLK+ 1.5	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	3	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	2 (NA)	
$t_{h(BL\_NOE)}$	FMC_BL hold time after FMC_NOE high	0	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	THCLK + 6	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOEx high setup time	THCLK +7	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	2	
$t_{w(NADV)}$	FMC_NADV low time	-	THCLK +1.5	

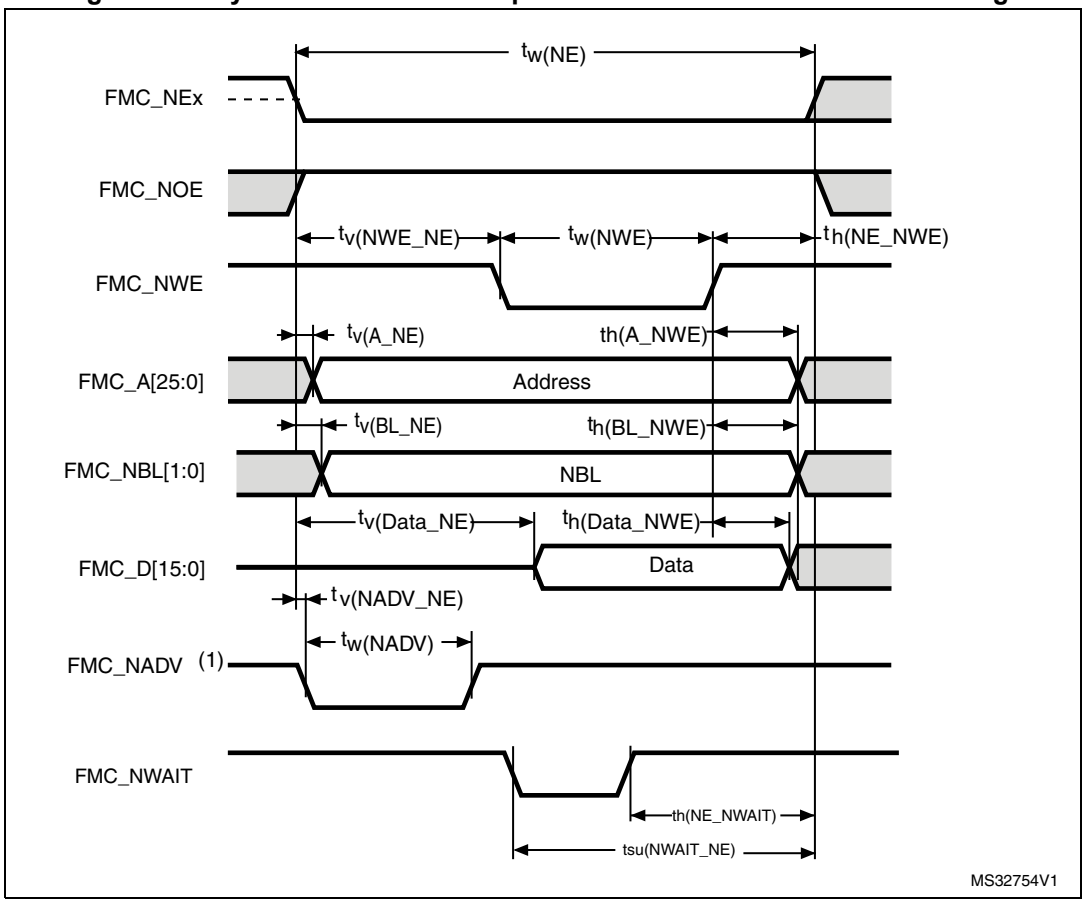
1. Based on characterization, not tested in production

Table 46. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	7THCLK +0.5	7THCLK+ 1	ns
$t_{w(NOE)}$	FMC_NWE low time	6THCLK -1.5	6THCLK +2	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	4THCLK +5	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4THCLK-3	-	

1. Based on characterization, not tested in production.

Figure 21. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 47. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	3THCLK-1	3THCLK+2	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	THCLK+0.5	THCLK+1	
$t_{w(NWE)}$	FMC_NWE low time	THCLK-2	THCLK+1	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	THCLK-0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	THCLK-1.5	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	1	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	THCLK-0.5	-	
$t_{v(Data\_NE)}$	Data to FMC_NEx low to Data valid	-	THCLK+ 3	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	THCLK+0.5	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	2.5	
$t_{w(NADV)}$	FMC_NADV low time	-	THCLK+2	

1. Based on characterization, not tested in production.

Table 48. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	8THCLK+1	8THCLK+2	ns
$t_{w(NWE)}$	FMC_NWE low time	6THCLK-1	6THCLK+2	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	5THCLK-0.5	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4THCLK+2	-	

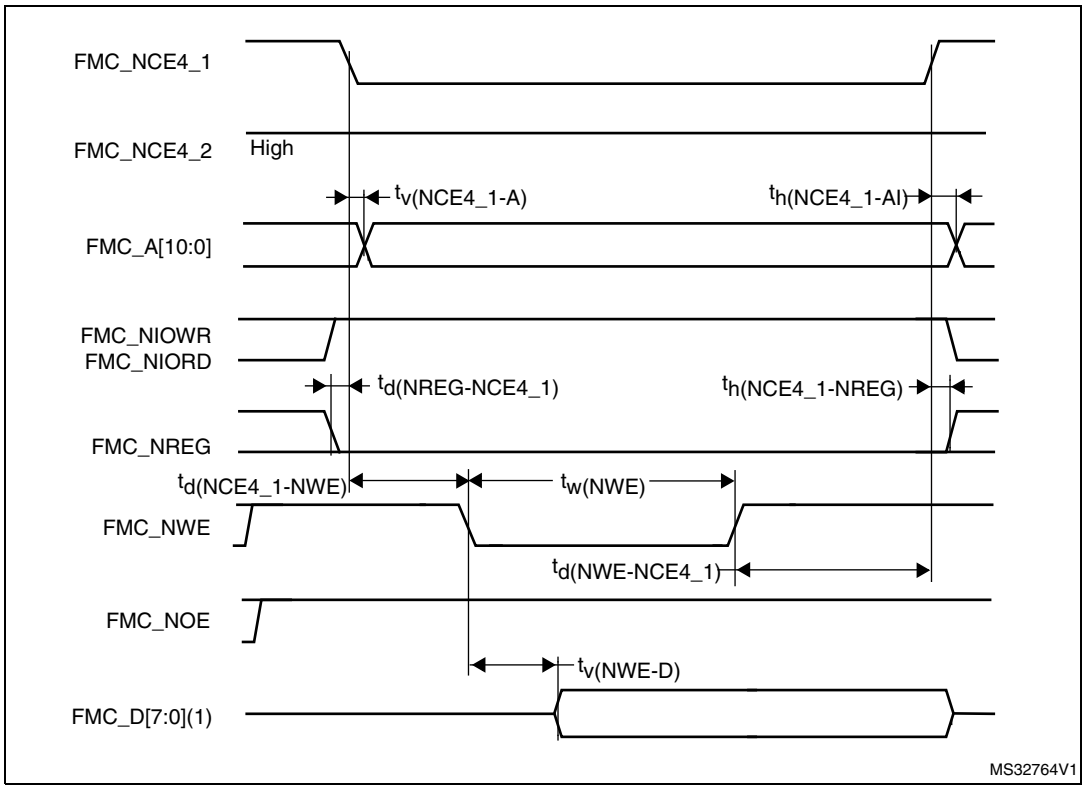
1. Based on characterization, not tested in production.

Table 49. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	8THCLK+2	8THCLK+2	ns
$t_{w(NOE)}$	FMC_NWE low time	6THCLK-1	6THCLK+1.5	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	4THCLK+6	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4THCLK-4	-	

1. Based on characterization, not tested in production.

Figure 31. PC Card/CompactFlash controller waveforms for attribute memory write access



1. Only data bits 0...7 are driven (bits 8...15 remains Hi-Z).

Table 58. Switching characteristics for PC Card/CF read and write cycles in I/O space(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NIOWR)}$	FMC_NIOWR low width	8THCLK-0.5	-	ns
$t_{v(NIOWR-D)}$	FMC_NIOWR low to FMC_D[15:0] valid	-	5.5	
$t_{h(NIOWR-D)}$	FMC_NIOWR high to FMC_D[15:0] invalid	4THCLK-0.5	-	
$t_{d(NCE4\_1-NIOWR)}$	FMC_NCE4_1 low to FMC_NIOWR valid	-	5THCLK+1	
$t_{h(NCEx-NIOWR)}$	FMC_NCEx high to FMC_NIOWR invalid	4THCLK+0.5	-	
$t_{d(NIORD-NCEx)}$	FMC_NCEx low to FMC_NIORD valid	-	5THCLK	
$t_{h(NCEx-NIORD)}$	FMC_NCEx high to FMC_NIORD) valid	6THCLK+2	-	
$t_{w(NIORD)}$	FMC_NIORD low width	8THCLK-1	8THCLK+1	
$t_{su(D-NIORD)}$	FMC_D[15:0] valid before FMC_NIORD high	THCLK+2	-	
$t_{d(NIORD-D)}$	FMC_D[15:0] valid after FMC_NIORD high	0	-	

1. Based on characterization, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 64. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II Level A

6.3.14 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

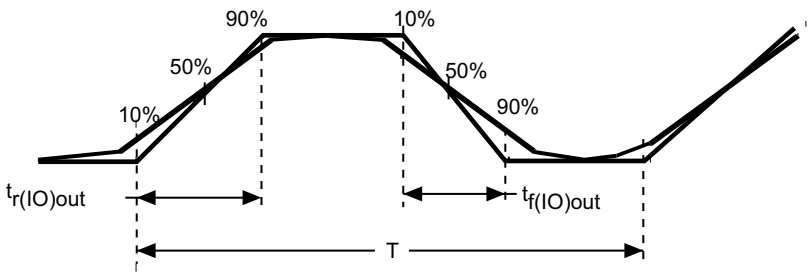
The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The test results are given in *Table 65*.

Table 65. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	-0	NA	mA
	Injected current on PF3, PC1, PC2, PA1, PA2, PA3, PA4, PA5, PA6, PA7, PB0, PB1, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PB13, PB14, PB15, PD8, PD9, PD10, PD11, PD12, PD13, PD14 pins with induced leakage current on adjacent pins less than -50 µA or more than +400 µA	-5	+5	
	Injected current on PF2, PF4, PC0, PC1, PC2, PC3, PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7, PC4, PC5, PB2, PB11 with induced leakage current on other pins from this group less than -50 µA or more than +400 µA	-5	+5	

Figure 40. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \le 2/3)T$ and if the duty cycle is (45-55%) when loaded by C_L (1)

MS36445V1

1. See *Table 68: I/O AC characteristics*.

6.3.16 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 66*).

Unless otherwise specified, the parameters given in *Table 69* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 19*.

Table 69. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$ (1)	NRST Input low level voltage	-	-	-	$0.3V_{DD}+0.07$ (1)	V
$V_{IH(NRST)}$ (1)	NRST Input high level voltage	-	$0.445V_{DD}+0.398$ (1)	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor (2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$ (1)	NRST Input filtered pulse	-	-	-	100 (1)	ns
$V_{NF(NRST)}$ (1)	NRST Input not filtered pulse	-	500 (1)	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Table 73. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Pulse width of spikes that are suppressed by the analog filter	50	260	ns

1. Guaranteed by design, not tested in production.

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 74* for SPI or in *Table 75* for I²S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 19*.

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 74. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode 2.7 V<V_{DD}<3.6 V, SPI1/4	-	-	24	MHz
		Master mode 2 V<V_{DD}<3.6 V, SPI1/2/3/4			18	
		Slave mode 2 V<V_{DD}<3.6 V, SPI1/4			24	
		Slave mode 2 V<V_{DD}<3.6 V, SPI1/2/3/4			18	
		Slave mode transmitter/full duplex 2 V<V_{DD}<3.6 V, SPI1/2/3/4			16.5(2)	
		Slave mode transmitter/full duplex 2.7 V<V_{DD}<3.6 V, SPI1/4			22.5(2))	-
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	3	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	6.5	-	-	
$t_{h(SI)}$		Slave mode	4.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	10	-	30	
$t_{dis(SO)}$	Data output disable time	Slave mode	8	-	7	

Table 79. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{REF}	Current on VREF+ pin (see *Figure 49*)	Single-ended mode, 5 MSPS	-	104	139	µA
		Single-ended mode, 1 MSPS	-	20.4	37	
		Single-ended mode, 200 KSPS	-	3.3	11.3	
		Differential mode, 5 MSPS	-	174	235	
		Differential mode, 1 MSPS	-	34.6	52.6	
		Differential mode, 200 KSPS	-	6	13.6	
V_{REF+}	Positive reference voltage	-	2	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	-	0.14	-	72	MHz
f_S(1)	Sampling rate	Resolution = 12 bits, Fast Channel	0.01	-	5.14	MSPS
		Resolution = 10 bits, Fast Channel	0.012	-	6	
		Resolution = 8 bits, Fast Channel	0.014	-	7.2	
		Resolution = 6 bits, Fast Channel	0.0175	-	9	
f_{TRIG}(1)	External trigger frequency	f_{ADC} = 72 MHz Resolution = 12 bits	-	-	5.14	MHz
		Resolution = 12 bits	-	-	14	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(2)	-	0	-	V_{REF+}	V
R_{AIN}(1)	External input impedance	-	-	-	100	kΩ
C_{ADC}(1)	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}(1)	Power-up time	-	0	0	1	µs
t_{CAL}(1)	Calibration time	f_{ADC} = 72 MHz	1.56			µs
		-	112			$1/f_{ADC}$
t_{latr}(1)	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2	$1/f_{ADC}$
		CKMODE = 10	-	-	2.25	$1/f_{ADC}$
		CKMODE = 11	-	-	2.125	$1/f_{ADC}$
$t_{latrinj}$(1)	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3	$1/f_{ADC}$
		CKMODE = 10	-	-	3.25	$1/f_{ADC}$
		CKMODE = 11	-	-	3.125	$1/f_{ADC}$

Table 80. Maximum ADC R_{AIN} (1) (continued)

Resolution	Sampling cycle @ 72 MHz	Sampling time [ns] @ 72 MHz	R_{AIN} max (kΩ)		
			Fast channels(2)	Slow channels	Other channels(3)
8 bits	1.5	20.83	0.150	NA	0.039
	2.5	34.72	0.390	0.180	0.180
	4.5	62.50	0.820	0.560	0.470
	7.5	104.17	1.50	1.20	1.00
	19.5	270.83	3.90	3.30	2.70
	61.5	854.17	12.00	12.00	8.20
	181.5	2520.83	39.00	33.00	27.00
	601.5	8354.17	100.00	100.00	82.00
6 bits	1.5	20.83	0.270	0.100	0.150
	2.5	34.72	0.560	0.390	0.330
	4.5	62.50	1.200	0.820	0.820
	7.5	104.17	2.20	1.80	1.50
	19.5	270.83	5.60	4.70	3.90
	61.5	854.17	18.0	15.0	12.0
	181.5	2520.83	56.0	47.0	39.0
	601.5	8354.17	100.00	100.0	100.0

1. Data based on characterization results, not tested in production.
2. All fast channels, expect channels on PA2, PA6, PB1, PB12.
3. Fast channels available on PA2, PA6, PB1, PB12.

Table 83. ADC accuracy - limited test conditions, 64-pin packages(1)(2)

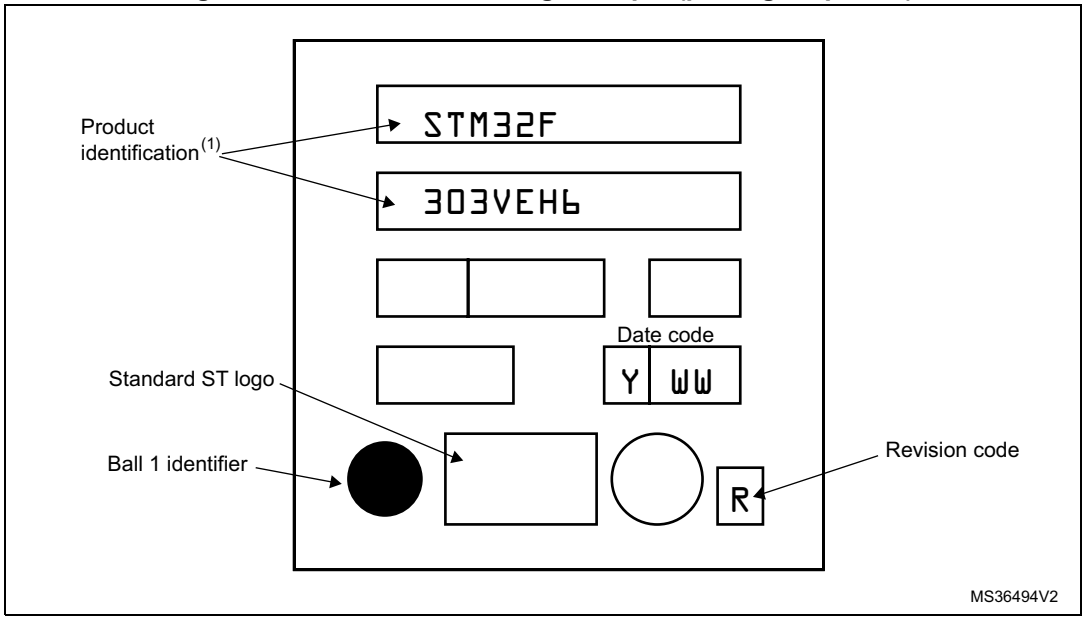
Symbol	Parameter	Conditions			Min (3)	Typ	Max (3)	Unit
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz Sampling freq. ≤ 5 Msps V_{DDA} = 3.3 V 25°C 64-pin package	Single ended	Fast channel 5.1 Ms	-	±4	±4.5	LSB
				Slow channel 4.8 Ms	-	±5.5	±6	
			Differential	Fast channel 5.1 Ms	-	±3.5	±4	
				Slow channel 4.8 Ms	-	±3.5	±4	
EO	Offset error		Single ended	Fast channel 5.1 Ms	-	±2	±2	
				Slow channel 4.8 Ms	-	±1.5	±2	
			Differential	Fast channel 5.1 Ms	-	±1.5	±2	
				Slow channel 4.8 Ms	-	±1.5	±2	
EG	Gain error		Single ended	Fast channel 5.1 Ms	-	±3	±4	
				Slow channel 4.8 Ms	-	±5	±5.5	
			Differential	Fast channel 5.1 Ms	-	±3	±3	
				Slow channel 4.8 Ms	-	±3	±3.5	
ED	Differential linearity error		Single ended	Fast channel 5.1 Ms	-	±1	±1	
				Slow channel 4.8 Ms	-	±1	±1	
			Differential	Fast channel 5.1 Ms	-	±1	±1	
				Slow channel 4.8 Ms	-	±1	±1	
EL	Integral linearity error		Single ended	Fast channel 5.1 Ms	-	±1.5	±2	
				Slow channel 4.8 Ms	-	±2	±3	
			Differential	Fast channel 5.1 Ms	-	±1.5	±1.5	
				Slow channel 4.8 Ms	-	±1.5	±2	
ENOB (4)	Effective number of bits		Single ended	Fast channel 5.1 Ms	10.8	10.8	-	bit
				Slow channel 4.8 Ms	10.8	10.8	-	
			Differential	Fast channel 5.1 Ms	11.2	11.3	-	
				Slow channel 4.8 Ms	11.2	11.3	-	
SINAD (4)	Signal-to-noise and distortion ratio		Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	

Device marking for UFBGA100

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 59. UFBGA100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.