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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	86
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 39x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f303vdt6

2 Description

The STM32F303xD/E family is based on the high-performance ARM® Cortex®-M4 32-bit RISC core with FPU operating at a frequency of 72 MHz, and embedding a floating point unit (FPU), a memory protection unit (MPU) and an embedded trace macrocell (ETM). The family incorporates high-speed embedded memories (512-Kbyte Flash memory, 80-Kbyte SRAM), a flexible memory controller (FSMC) for static memories (SRAM, PSRAM, NOR and NAND), and an extensive range of enhanced I/Os and peripherals connected to an AHB and two APB buses.

The devices offer four fast 12-bit ADCs (5 Msps), seven comparators, four operational amplifiers, two DAC channels, a low-power RTC, up to five general-purpose 16-bit timers, one general-purpose 32-bit timer, and up,to three timers dedicated to motor control. They also feature standard and advanced communication interfaces: up to three I^2Cs, up to four SPIs (two SPIs are with multiplexed full-duplex I^2Ss), three USARTs, up to two UARTs, CAN and USB. To achieve audio class accuracy, the I^2S peripherals can be clocked via an external PLL.

The STM32F303xD/E family operates in the -40 to +85°C and -40 to +105°C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F303xD/E family offers devices in different packages ranging from 64 to 144 pins.

Depending on the device chosen, different sets of peripherals are included.

Table 2. STM32F303xD/E family device features and peripheral counts

Peripheral		STM32F303Rx		STM32F303Vx		STM32F303Zx	
Flash (Kbytes)		384	512	384	512	384	512
SRAM (Kbytes) on data bus		64					
CCM (Core Coupled Memory) RAM (Kbytes)		16					
FMC (flexible memory controller)		NO		YES			
Timers	Advanced control	2 (16-bit)(1)		3 (16-bit)			
	General purpose	5 (16-bit) 1 (32-bit)					
	PWM channels (all) (2)	31		40		40	
	Basic	2 (16-bit)					
	PWM channels (except complementary)	22		28		28	
Communication interfaces	SPI (I^2S)(3)	4(2)					
	I^2C	3					
	USART	3					
	UART	2					
	CAN	1					
	USB	1					
GPIOs	Normal I/Os (TC, TTa)	26		37 in WLCSP100,44 in LQFP100 and UFBGA100		45	
	5-volt tolerant I/Os (FT, FTf)	25		42 in LQFP100 40 in WLCSP100 and UFBGA100		70	
DMA channels		12					
Capacitive sensing channels		18		24			
12-bit ADCs		4 22 channels		4 39 channels in LQFP100-pin and UFBGA100 33 channels in WLCSP100		4 40 channels	
12-bit DAC channels							
Analog comparator							
Operational amplifiers							
CPU frequency		72 MHz					
Operating voltage		2.0 to 3.6 V					

3.7 Power management

3.7.1 Power supply schemes

- V_{SS}, V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. It is provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supply for ADC, DAC, comparators, operational amplifier, reset blocks, RCs and PLL. The minimum voltage to be applied to V_{DDA} differs from one analog peripheral to another. *Table 3* provides the summary of the V_{DDA} ranges for analog peripherals. The V_{DDA} voltage level must always be greater than or equal to the V_{DD} voltage level and must be provided first.

Table 3. External analog supply values for analog peripherals

Analog peripheral	Minimum V_{DDA} supply	Maximum V_{DDA} supply
ADC/COMP	2.0 V	3.6 V
DAC/OPAMP	2.4 V	3.6 V

- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.7.2 Power supply supervisor

The device has an integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.7.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR), and power-down.

- The MR mode is used in the nominal regulation mode (Run)
- The LPR mode is used in Stop mode.
- The power-down mode is used in Standby mode: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The voltage regulator is always enabled after reset. It is disabled in Standby mode.

Table 13. STM32F303xD/E pin definitions (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	UFBGA100	WLCSP100	LQFP144						
-	56	K8	G4	78	PD9	I/O	TTa	(1)	EVENTOUT, USART3_RX, FMC_D14	ADC4_IN13
-	57	J12	H3	79	PD10	I/O	TTa	(1)	EVENTOUT, USART3_CK, FMC_D15	ADC34_IN7, COMP6_INM
-	58	J11	H2	80	PD11	I/O	TTa	(1)	EVENTOUT, USART3_CTS, FMC_A16	ADC34_IN8, OPAMP4_VINP
-	59	J10	H1	81	PD12	I/O	TTa	(1)	EVENTOUT, TIM4_CH1, TSC_G8_IO1, USART3_RTS, FMC_A17	ADC34_IN9
-	60	H12	G3	82	PD13	I/O	TTa	(1)	EVENTOUT, TIM4_CH2, TSC_G8_IO2, FMC_A18	ADC34_IN10, COMP5_INM
-	-	-	-	83	VSS	S	-	(1)	-	-
-	-	-	-	84	VDD	S	-	(1)	-	-
-	61	H11	G2	85	PD14	I/O	TTa	(1)	EVENTOUT, TIM4_CH3, TSC_G8_IO3, FMC_D0	ADC34_IN11, OPAMP2_VINP
-	62	H10	G1	86	PD15	I/O	TTa	(1)	EVENTOUT, TIM4_CH4, TSC_G8_IO4, SPI2_NSS, FMC_D1	COMP3_INM
-	-	-	-	87	PG2	I/O	FT	(1)	EVENTOUT, TIM20_CH3N, FMC_A12	-
-	-	-	-	88	PG3	I/O	FT	(1)	EVENTOUT, TIM20_BKIN, FMC_A13	-
-	-	-	-	89	PG4	I/O	FT	(1)	EVENTOUT, TIM20_BKIN2, FMC_A14	-
-	-	-	-	90	PG5	I/O	FT	(1)	EVENTOUT, TIM20_ETR, FMC_A15	-
-	-	-	-	91	PG6	I/O	FT	(1)	EVENTOUT, FMC_INT2	-
-	-	-	-	92	PG7	I/O	FT	(1)	EVENTOUT, FMC_INT3	-
-	-	-	-	93	PG8	I/O	FT	(1)	EVENTOUT	-
-	-	-	-	94	VSS	S	-	(1)	-	-
-	-	-	-	95	VDD	S	-	(1)	-	-

Table 14. STM32F303xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3/TIM8/20/15/GPCOMP7/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/TIM8/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP3/5/6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port E	PE0	-	EVENT OUT	TIM4_ETR	-	TIM16_CH1	-	TIM20_ETR	USART1_TX	-	-	-	-	FMC_NBL0	-	-	-
	PE1	-	EVENT OUT	-	-	TIM17_CH1	-	TIM20_CH4	USART1_RX	-	-	-	-	FMC_NBL1	-	-	-
	PE2	TRACECK	EVENT OUT	TIM3_CH1	TSC_G7_IO1	-	SPI4_SCK	TIM20_CH1	-	-	-	-	-	FMC_A23	-	-	-
	PE3	TRACED0	EVENT OUT	TIM3_CH2	TSC_G7_IO2	-	SPI4_NSS	TIM20_CH2	-	-	-	-	-	FMC_A19	-	-	-
	PE4	TRACED1	EVENT OUT	TIM3_CH3	TSC_G7_IO3	-	SPI4_NSS	TIM20_CH1N	-	-	-	-	-	FMC_A20	-	-	-
	PE5	TRACED2	EVENT OUT	TIM3_CH4	TSC_G7_IO4	-	SPI4_MISO	TIM20_CH2N	-	-	-	-	-	FMC_A21	-	-	-
	PE6	TRACED3	EVENT OUT	-	-	-	SPI4_MOSI	TIM20_CH3N	-	-	-	-	-	FMC_A22	-	-	-
	PE7	-	EVENT OUT	TIM1_ETR	-	-	-	-	-	-	-	-	-	FMC_D4	-	-	-
	PE8	-	EVENT OUT	TIM1_CH1N	-	-	-	-	-	-	-	-	-	FMC_D5	-	-	-
	PE9	-	EVENT OUT	TIM1_CH1	-	-	-	-	-	-	-	-	-	FMC_D6	-	-	-
	PE10	-	EVENT OUT	TIM1_CH2N	-	-	-	-	-	-	-	-	-	FMC_D7	-	-	-
	PE11	-	EVENT OUT	TIM1_CH2	-	-	SPI4_NSS	-	-	-	-	-	-	FMC_D8	-	-	-

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Note: The total current consumption is the sum of I_{DD} and I_{DDA}.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz,1 wait state from 24 to 48 MHz and 2 wait states from 48 to 72 MHz)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK2} = f_{HCLK}$ and $f_{PCLK1} = f_{HCLK/2}$
- When f_{HCLK} > 8 MHz, the PLL is ON and the PLL input is equal to HSI/2 (4 MHz) or HSE (8 MHz) in bypass mode.

The parameters given in *Table 25* to *Table 29* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 19*.

Table 25. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6V

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, executing from Flash	External clock (HSE bypass)	72 MHz	66.4	76.5	76.9	77.4	33.0	37.2	38.1	38.9	mA
			64 MHz	59.8	66.4	67.7	68.6	29.7	33.5	34.3	35.0	
			48 MHz	47.3	53.7	53.8	55.1	23.2	26.2	27.1	28.0	
			32 MHz	33.3	36.8	37.4	38.5	16.8	19.8	20.6	21.4	
			24 MHz	26.0	29.4	30.0	31.2	13.5	16.6	17.4	18.6	
			8 MHz	10.7	13.8	14.4	15.3	6.63	10.2	10.5	11.2	
			1 MHz	4.27	7.47	8.13	8.90	3.78	7.40	7.70	8.50	
		Internal clock (HSI)	64 MHz	55.6	59.6	62.8	63.2	29.4	33.1	34.5	35.0	
			48 MHz	43.6	47.0	49.2	50.1	23.1	26.2	27.1	28.0	
			32 MHz	30.8	33.6	35.3	35.8	16.7	19.8	20.6	21.5	
			24 MHz	24.0	28.0	28.2	29.7	13.5	16.5	17.5	18.4	
			8 MHz	10.5	13.6	14.7	15.2	6.63	9.74	10.6	11.2	
I_{DD}	Supply current in Run mode, executing from RAM	External clock (HSE bypass)	72 MHz	66.2	76.2(2)	76.7	77.2(2)	32.8	36.9(2)	37.7	38.5(2)	
			64 MHz	59.6	66.2	67.6	68.4	29.3	33.1	33.9	34.4	
			48 MHz	47.0	53.4	53.6	54.9	22.4	25.6	26.2	27.2	
			32 MHz	33.0	36.6	37.2	38.1	16.0	19.0	19.5	20.4	
			24 MHz	25.6	29.0	29.5	30.6	12.8	15.7	16.3	17.6	
			8 MHz	10.3	13.4	13.8	14.7	6.40	9.48	9.93	10.90	

Table 33. Peripheral current consumption

Peripheral	Typical consumption(1)	Unit
	I_{DD}	
BusMatrix (2)	8.3	µA/MHz
DMA1	7.0	
DMA2	5.4	
FSMC	35.0	
CRC	1.5	
GPIOH	1.3	
GPIOA	5.4	
GPIOB	5.3	
GPIOC	5.4	
GPIOD	5.0	
GPIOE	5.4	
GPIOF	5.2	
GPIOG	5.0	
TSC	5.2	
ADC1&2	15.4	
ADC3&4	16.2	
APB2-Bridge (3)	3.1	
SYSCFG	4.0	
TIM1	26.0	
SPI1	6.2	
TIM8	26.4	
USART1	17.7	
SPI4	6.2	
TIM15	11.9	
TIM16	8.0	
TIM17	8.5	
TIM20	25.3	

Table 33. Peripheral current consumption (continued)

Peripheral	Typical consumption(1)	Unit
	I_{DD}	
APB1-Bridge (3)	6.7	µA/MHz
TIM2	39.2	
TIM3	30.8	
TIM4	31.3	
TIM6	4.3	
TIM7	4.3	
WWDG	1.3	
SPI2	33.6	
SPI3	33.9	
USART2	39.3	
USART3	39.3	
UART4	29.8	
UART5	27.0	
I2C1	6.7	
I2C2	6.4	
USB	14.7	
CAN	25.6	
PWR	3.7	
DAC	22.1	
I2C3	6.8	

1. The power consumption of the analog part (I_{DDA}) of peripherals such as ADC, DAC, Comparators, OpAmp is not included. Refer to the tables of characteristics in the subsequent sections.
2. BusMatrix is automatically active when at least one master is ON (CPU, DMA1 or DMA2).
3. The APBx bridge is automatically active when at least one peripheral is ON on the same bus.

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

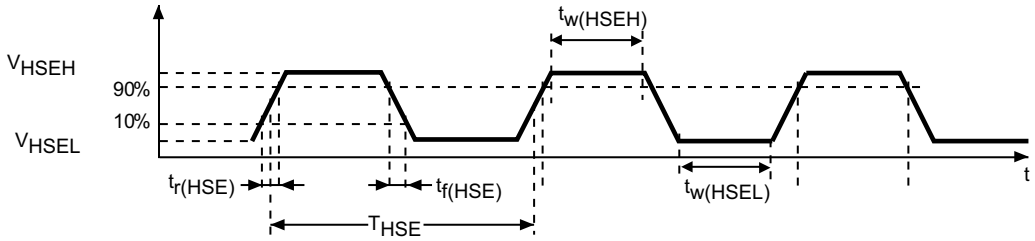
In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.15*. However, the recommended clock input waveform is shown in *Figure 15*.

Table 36. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)	-	1	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time(1)		15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	

1. Guaranteed by design, not tested in production.

Figure 15. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.15*. However, the recommended clock input waveform is shown in *Figure 16*.

Table 37. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	

1. Guaranteed by design, not tested in production.

Figure 16. Low-speed external clock source AC timing diagram

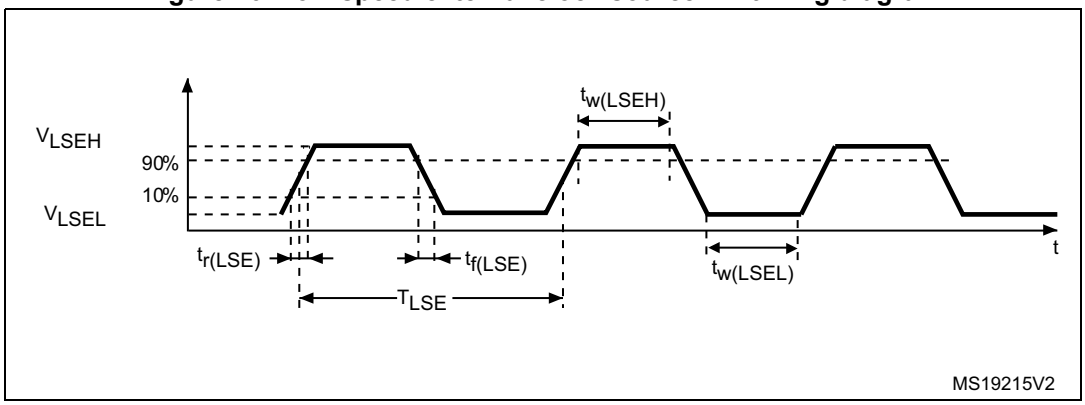
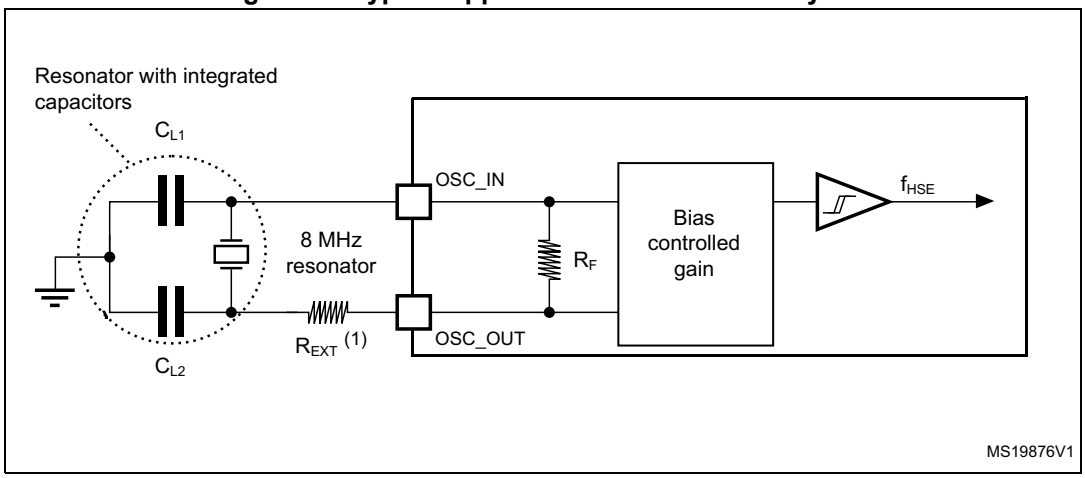


Figure 17. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 39*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

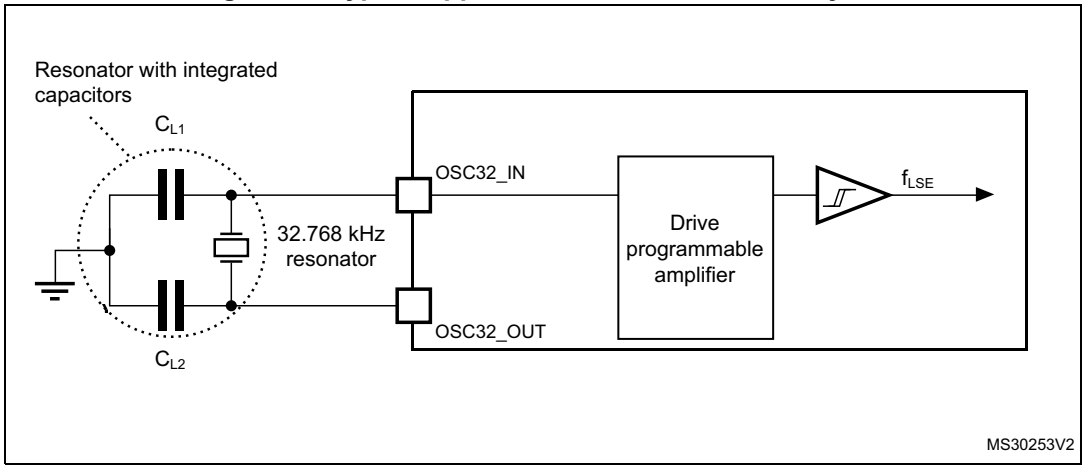
Table 39. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability	-	0.5	0.9	µA
		LSEDRV[1:0]=01 medium low driving capability	-	-	1	
		LSEDRV[1:0]=10 medium high driving capability	-	-	1.3	
		LSEDRV[1:0]=11 higher driving capability	-	-	1.6	
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5	-	-	µA/V
		LSEDRV[1:0]=01 medium low driving capability	8	-	-	
		LSEDRV[1:0]=10 medium high driving capability	15	-	-	
		LSEDRV[1:0]=11 higher driving capability	25	-	-	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 18. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in *Table 40* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 19*.

High-speed internal (HSI) RC oscillator

Table 40. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1(2)	%
$DuCy_{(HSI)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -40 to 105°C	-2.8(3)	-	3.8(3)	%
		T_A = -10 to 85°C	-1.9(3)	-	2.3(3)	
		T_A = 0 to 85°C	-1.9(3)	-	2(3)	
		T_A = 0 to 70°C	-1.3(3)	-	2(3)	
		T_A = 0 to 55°C	-1(3)	-	2(3)	
		T_A = 25°C(4)	-1	-	1	
$t_{SU(HSI)}$	HSI oscillator startup time	-	1(2)	-	2(2)	µs
$I_{DDA(HSI)}$	HSI oscillator power consumption	-	-	80	100(2)	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.
4. Factory calibrated, parts not soldered.

6.3.10 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 43. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	53.5	60	µs
t_{ERASE}	Page (2 KB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design, not tested in production.

Table 44. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycle(2) at T_A = 55 °C	20	

1. Data based on characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.11 FSMC characteristics

Unless otherwise specified, the parameters given in *Table 45* to *Table 60* for the FSMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 19* with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5VDD

Refer to *Section 6.3.15: I/O port characteristics*: for more details on the input/output characteristics.

Table 79. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S(1)	Sampling time	f_{ADC} = 72 MHz	0.021	-	8.35	µs
		-	1.5	-	601.5	$1/f_{ADC}$
$T_{ADCVREG\_STUP}$(1)	ADC Voltage Regulator Start-up time	-	-	-	10	µs
t_{CONV}(1)	Total conversion time (including sampling time)	f_{ADC} = 72 MHz Resolution = 12 bits	0.19	-	8.52	µs
		Resolution = 12 bits	14 to 614 (t_S for sampling + 12.5 for successive approximation)			$1/f_{ADC}$
CMIR	Common Mode Input signal range	ADC differential mode	(V_{SSA} + V_{REF}+)/2 – 0.18	(V_{SSA} + V_{REF}+)/2	(V_{SSA} + V_{REF}+)/2 + 0.18	V

1. Data guaranteed by design, not tested in Production.
2. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 4: Pinout and pin description* for further details.

Figure 48. ADC typical current consumption on VDDA pin

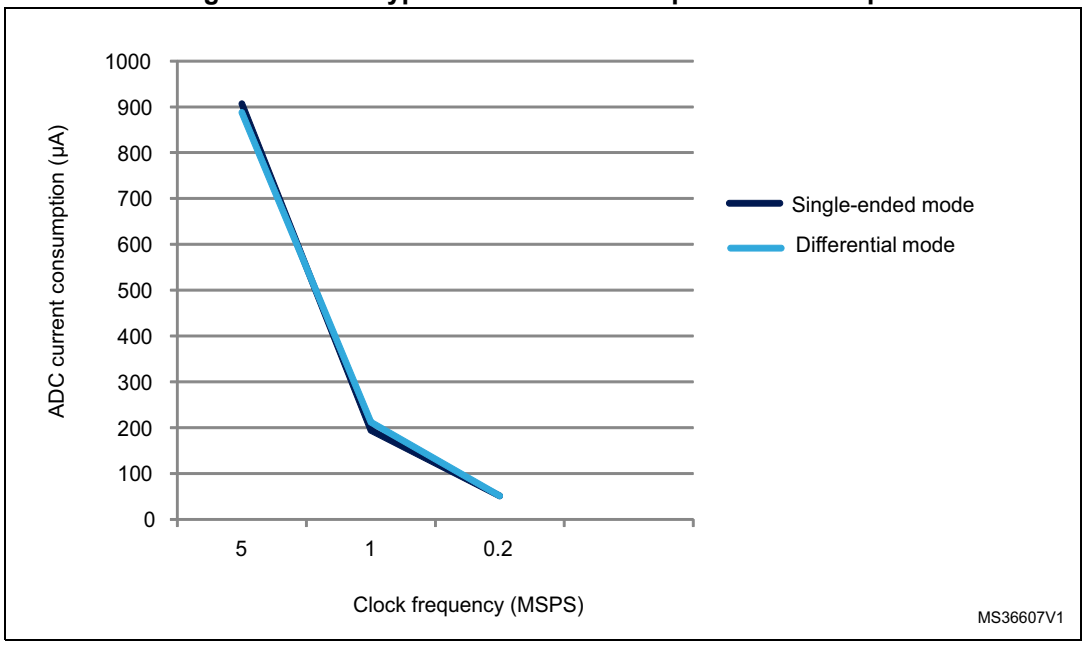


Table 85. ADC accuracy at 1MSPS(1)(2)

Symbol	Parameter	Test conditions		Typ	Max(3)	Unit
ET	Total unadjusted error	ADC Freq ≤ 72 MHz Sampling Freq ≤ 1MSPS 2.4 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V Single-ended mode	Fast channel	±2.5	±5	LSB
			Slow channel	±3.5	±5	
EO	Offset error		Fast channel	±1	±2.5	
			Slow channel	±1.5	±2.5	
EG	Gain error		Fast channel	±2	±3	
			Slow channel	±3	±4	
ED	Differential linearity error		Fast channel	±0.7	±2	
			Slow channel	±0.7	±2	
EL	Integral linearity error		Fast channel	±1	±3	
			Slow channel	±1.2	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for IINJ(PIN) and ∑IINJ(PIN) in *Section 6.3.15: I/O port characteristics* does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.

Figure 50. ADC accuracy characteristics

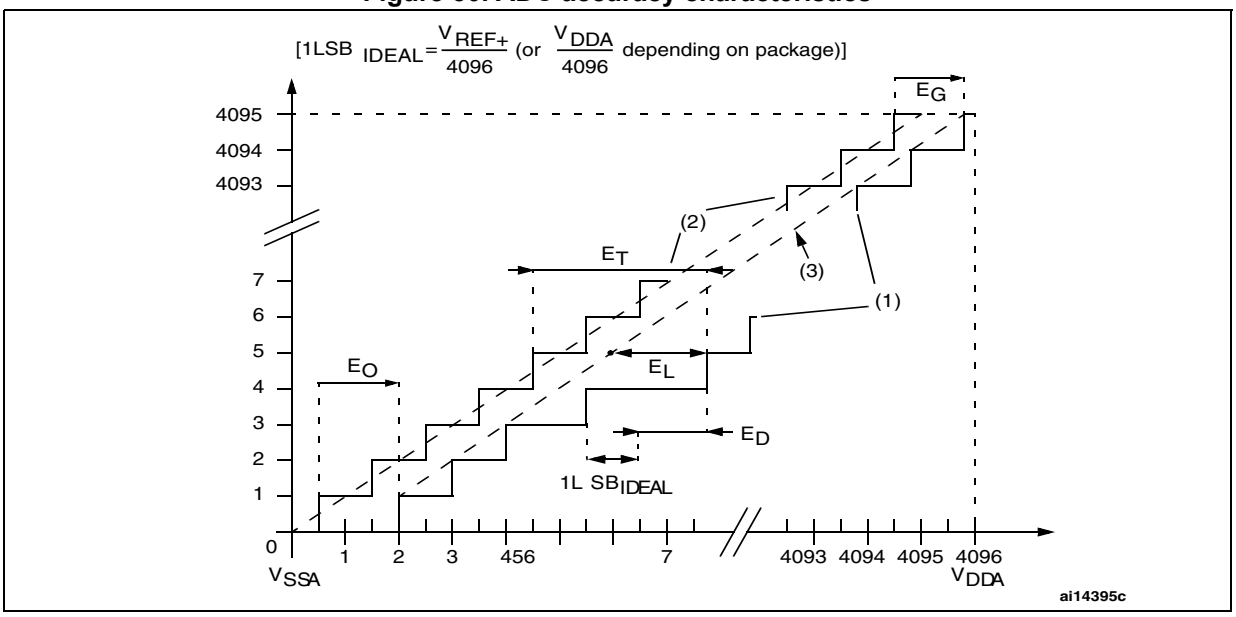


Table 86. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{REF}	DAC DC current consumption in quiescent mode (Standby mode)	With no load, worst code (0xF1C) on the input	-	-	220	µA
I_{DDA}(3)	DAC DC current consumption in quiescent mode (Standby mode)(2)	With no load, middle code (0x800) on the input.	-	-	380	µA
		With no load, worst code (0xF1C) on the input.	-	-	480	µA
DNL(3)	Differential non linearity Difference between two consecutive code-1LSB)	Given for a 10-bit input code	-	-	±0.5	LSB
		Given for a 12-bit input code	-	-	±2	LSB
INL(3)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095)	Given for a 10-bit input code	-	-	±1	LSB
		Given for a 12-bit input code	-	-	±4	LSB
Offset(3)	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{DDA}/2$)	-	-	-	±10	mV
		Given for a 10-bit input code at V_{DDA} = 3.6 V	-	-	±3	LSB
		Given for a 12-bit input code at V_{DDA} = 3.6 V	-	-	±12	LSB
Gain error(3)	Gain error	Given for a 12-bit input code	-	-	±0.5	%
$t_{SETTLING}$(3)	Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	$C_{LOAD} \leq$50 pF, $R_{LOAD} \geq$ 5 kΩ	-	3	4	µs
t_{STAB}	Power-up time	-	1			conversion cycle
Update rate(3)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	$C_{LOAD} \leq$50 pF, $R_{LOAD} \geq$ 5 kΩ	-	-	1	MS/s
t_{WAKEUP}(3)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	$C_{LOAD} \leq$50 pF, $R_{LOAD} \geq$ 5 kΩ	-	6.5	10	µs
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	C_{LOAD} = 50 pF, No $R_{LOAD} \geq$ 5 kΩ,	-	–67	–40	dB
I_{skink}(1)	Output sink current	DAC buffer ON Output level higher than 0.2 V	100	-	-	µA

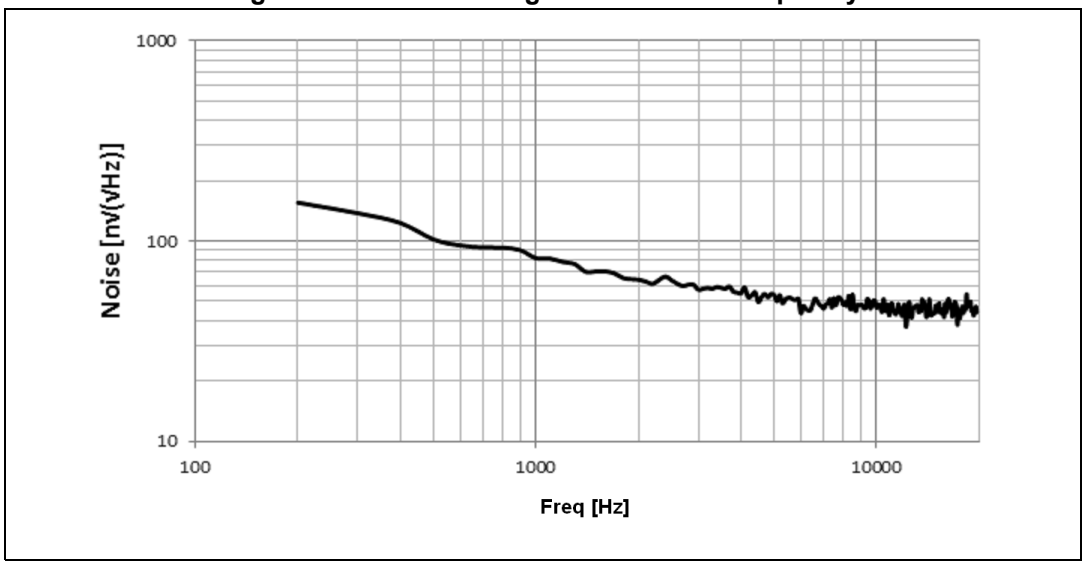
1. Guaranteed by design, not tested in production.

Table 87. Comparator characteristics(1) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
TV_{OFFSET}	Total offset variation	Full temperature range	-	-	3	mV
I_{DDA}	COMP current consumption	-	-	400	600	µA

1. Guaranteed by design, not tested in production.

Figure 53. OPAMP voltage noise versus frequency



6.3.23 Temperature sensor characteristics

Table 89. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(1)	Startup time	4	-	10	µs
T_{S_temp}(1)(2)	ADC sampling time when reading the temperature	2.2	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

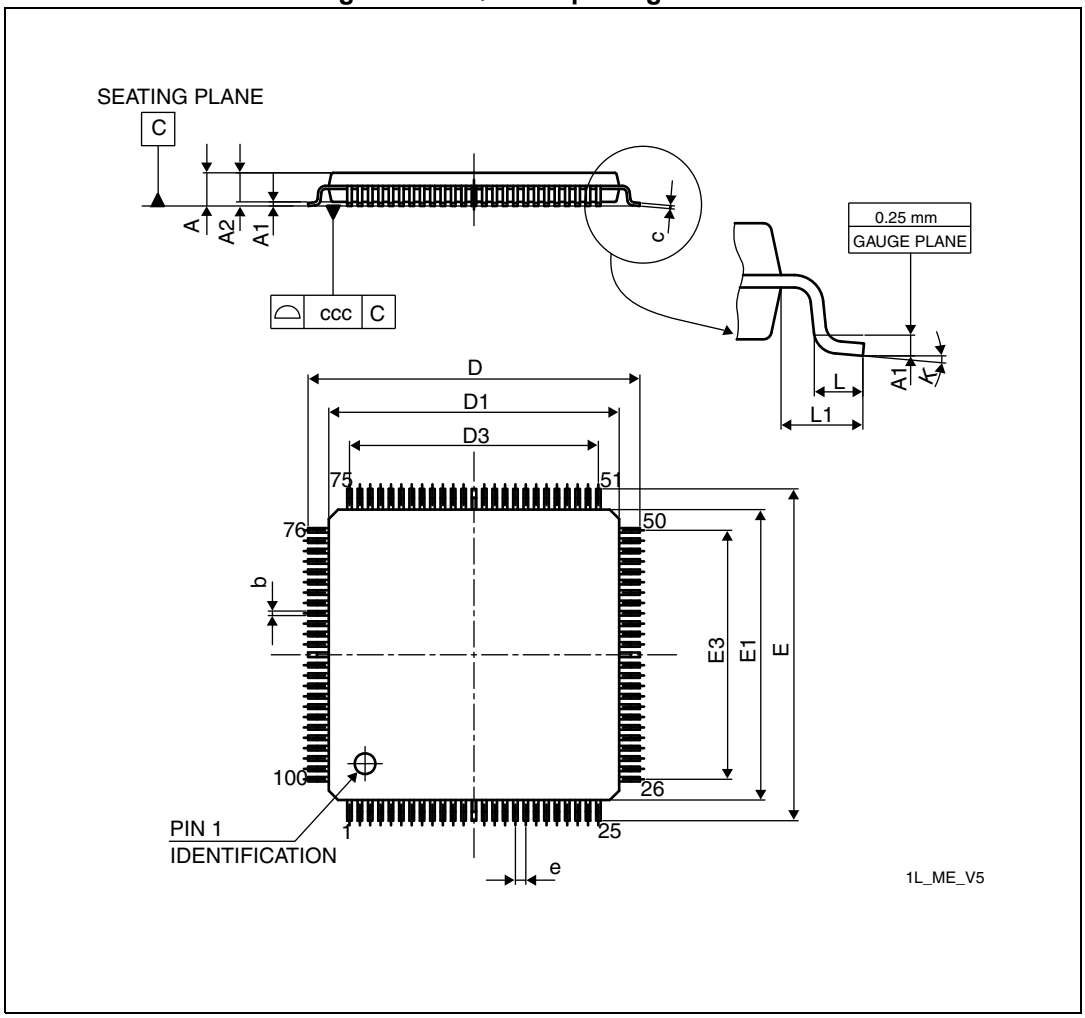
Table 90. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

7.4 LQFP100 package information

LQFP100 is a 100-pin, 14 x 14 mm low-profile quad flat package.

Figure 60. LQFP100 package outline



1. Drawing is not to scale.

Table 95. LQPF100 package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378

Table 96. WLCSP100 package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Typ	Min	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.38	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
Ø b[3]	0.22	0.25	0.28	-	0.0098	0.0110
D	4.74	4.775	4.81	-	0.1880	0.1894
E	5.006	5.041	5.076	-	0.1985	0.1998
e	-	0.4	-	-	0.0157	-
e1	-	3.6	-	-	0.1417	-
e2	-	3.6	-	-	0.1417	-
F	-	0.5875	-	-	0.0231	-
G	-	0.7205	-	-	0.0284	-
N	-	100	-	-	3.9370	-
aaa	-	0.1	-	-	0.0039	-
bbb	-	0.1	-	-	0.0039	-
ccc	-	0.1	-	-	0.0039	-
ddd	-	0.05	-	-	0.0020	-
eee	-	0.05	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 64. Recommended footprint for the WLCSP100 package