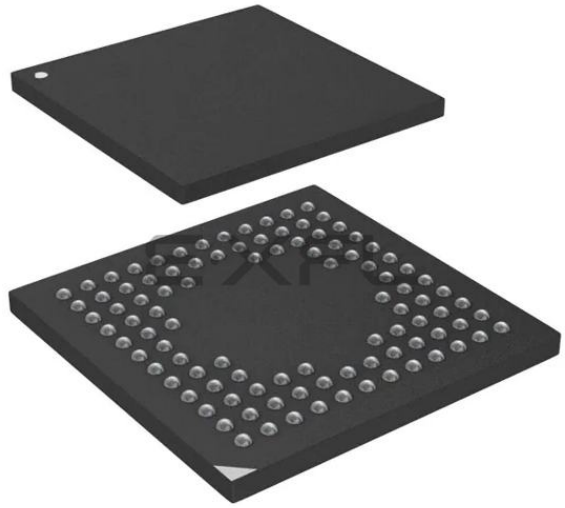

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	84
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 39x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f303veh6

Table 4. STM32F303xD/E peripheral interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action
GPIO RTCCLK HSE/32 MC0	TIM16	Clock source used as input channel for HSI and LSI calibration
CSS CPU (hard fault) COMPx GPIO	TIM1, TIM8, TIM20 TIM15, 16, 17	Timer break
GPIO	TIMx	External trigger, timer break
	ADCx DAC1	Conversion external trigger
DAC1	COMPx	Comparator inverting input

Note: For more details about the interconnect actions, refer to the corresponding sections in the STM32F303xD/Ereference manual (RM0316).

3.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability (for each channel)
- External triggers for conversion
- Input voltage reference VREF+

3.16 Operational amplifier (OPAMP)

The STM32F303xD/E embed four operational amplifiers with external or internal follower routing and PGA capability (or even amplifier and filter capability with external components). When an operational amplifier is selected, an external ADC channel is used to enable output measurement.

The operational amplifier features:

- 8.2 MHz bandwidth
- 0.5 mA output capability
- Rail-to-rail input/output
- In PGA mode, the gain is programmed to be 2, 4, 8 or 16.

3.17 Ultra-fast comparators (COMP)

The STM32F303xD/E devices embed seven ultra-fast rail-to-rail comparators with programmable reference voltage (internal or external) and selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pin
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to *Table 23: Embedded internal reference voltage* for the value and precision of the internal reference voltage.

All comparators can wake up from STOP mode, generate interrupts and breaks for the timers.

3.18 Timers and watchdogs

The STM32F303xD/E include three advanced control timers, up to six general-purpose timers, two basic timers, two watchdog timers and one SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

3.18.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.19 Real-time clock (RTC) and backup registers

The RTC and the 16 backup registers are supplied through a switch that takes power from either the V_{DD} supply when present or the V_{BAT} pin. The backup registers are sixteen 32-bit registers used to store 64 bytes of user application data when V_{DD} power is not present.

They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Automatic correction for 28, 29 (leap year), 30 and 31 days of the month.
- Two programmable alarms with wake up from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.
- 17-bit Auto-reload counter for periodic interrupt with wakeup from STOP/STANDBY capability.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

3.20 Inter-integrated circuit interface (I^2C)

Up to three I^2C bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes.

Table 13. STM32F303xD/E pin definitions

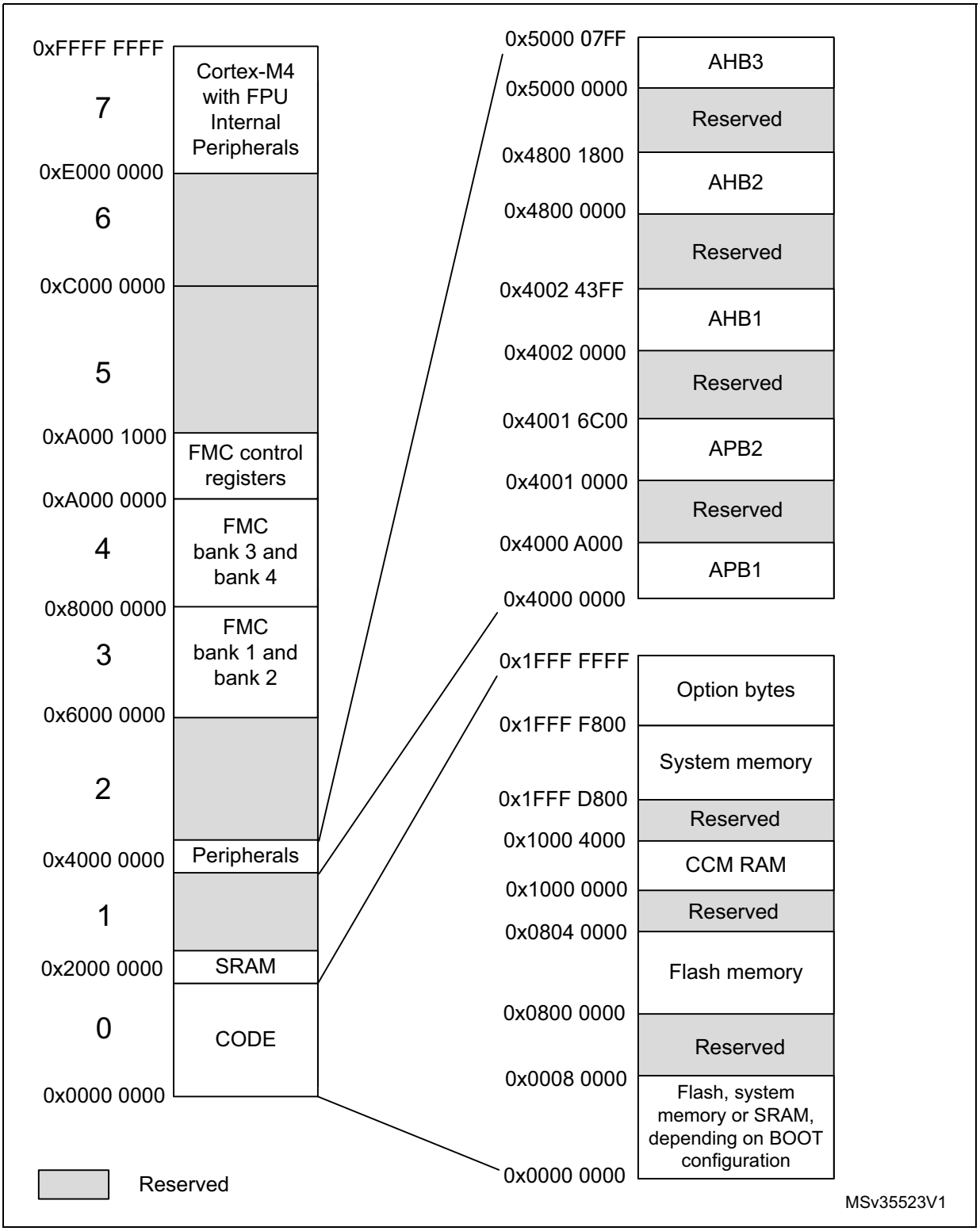
Pin number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	UFBGA100	WLCSP100	LQFP144						
-	1	B2	D6	1	PE2	I/O	FT	(1)	TRACECK, EVENTOUT, TIM3_CH1, TSC_G7_IO1, SPI4_SCK, TIM20_CH1, FMC_A23	-
-	2	A1	D7	2	PE3	I/O	FT	(1)	TRACED0, EVENTOUT, TIM3_CH2, TSC_G7_IO2, SPI4_NSS, TIM20_CH2, FMC_A19	-
-	3	B1	C8	3	PE4	I/O	FT	(1)	TRACED1, EVENTOUT, TIM3_CH3, TSC_G7_IO3, SPI4_NSS, TIM20_CH1N, FMC_A20	-
-	4	C2	B9	4	PE5	I/O	FT	(1)	TRACED2, EVENTOUT, TIM3_CH4, TSC_G7_IO4, SPI4_MISO, TIM20_CH2N, FMC_A21	-
-	5	D2	E7	5	PE6	I/O	FT	(1)	TRACED3, EVENTOUT, SPI4_MOSI, TIM20_CH3N, FMC_A22	WKUP3, RTC_TAMP3
1	6	E2	D8	6	VBAT	S	-	-	-	-
2	7	C1	C9	7	PC13(2)	I/O	TC	-	EVENTOUT, TIM1_CH1N	WKUP2,RTC_TAMP1, RTC_TS, RTC_OUT
3	8	D1	C10	8	PC14 - OSC32_IN (2)	I/O	TC	-	EVENTOUT	OSC32_IN
4	9	E1	D9	9	PC15 - OSC32_OUT(2)	I/O	TC	-	EVENTOUT	OSC32_OUT
-	-	-	-	10	PH0	I/O	FT	(1)	EVENTOUT, TIM20_CH1, FMC_A0	-
-	-	-	-	11	PH1	I/O	FT	(1)	EVENTOUT, TIM20_CH2, FMC_A1	-
-	19	J1	E8	12	PF2	I/O	TTa	(1)	EVENTOUT, TIM20_CH3, FMC_A2	ADC12_IN10
-	-	-	-	13	PF3	I/O	FT	(1)	EVENTOUT, TIM20_CH4, FMC_A3	-

Table 14. STM32F303xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3/TIM8/20/15/GPCOMP7/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/TIM8/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP3/5/6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port E	PE12	-	EVENT OUT	TIM1_CH3N	-	-	SPI4_SCK	-	-	-	-	-	-	FMC_D9	-	-	-
	PE13	-	EVENT OUT	TIM1_CH3	-	-	SPI4_MISO	-	-	-	-	-	-	FMC_D10	-	-	-
	PE14	-	EVENT OUT	TIM1_CH4	-	-	SPI4_MOSI	TIM1_BKIN2	-	-	-	-	-	FMC_D11	-	-	-
	PE15	-	EVENT OUT	TIM1_BKIN	-	-	-	-	USART3_RX	-	-	-	-	FMC_D12	-	-	-
Port F	PF0	-	EVENT OUT	-	-	I2C2_SDA	SPI2_NSS/I2S2_WS	TIM1_CH3N	-	-	-	-	-	-	-	-	-
	PF1	-	EVENT OUT	-	-	I2C2_SCL	SPI2_SCK/I2S2_CK	-	-	-	-	-	-	-	-	-	-
	PF2	-	EVENT OUT	TIM20_CH3	-	-	-	-	-	-	-	-	-	FMC_A2	-	-	-
	PF3	-	EVENT OUT	TIM20_CH4	-	-	-	-	-	-	-	-	-	FMC_A3	-	-	-
	PF4	-	EVENT OUT	COMP1_OUT	TIM20_CH1N	-	-	-	-	-	-	-	-	FMC_A4	-	-	-
	PF5	-	EVENT OUT	TIM20_CH2N	-	-	-	-	-	-	-	-	-	FMC_A5	-	-	-
	PF6	-	EVENT OUT	TIM4_CH4	-	I2C2_SCL	-	-	USART3_RTS	-	-	-	-	FMC_NIORD	-	-	-
	PF7	-	EVENT OUT	TIM20_BKIN	-	-	-	-	-	-	-	-	-	FMC_NREG	-	-	-

5 Memory mapping

Figure 9. STM32F303xD/E memory map



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 38*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 38. HSE oscillator characteristics

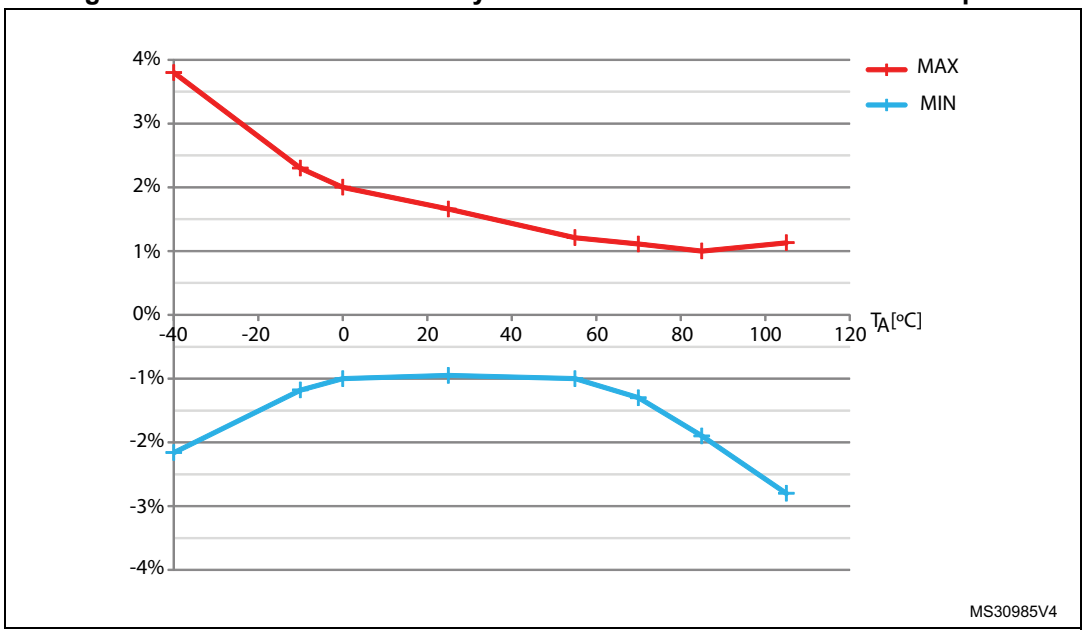
Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
I_{DD}	HSE current consumption	During startup(3)	-	-	8.5	mA
		V_{DD}= 3.3 V, Rm= 30Ω, CL=10 pF@8 MHz	-	0.4	-	
		V_{DD}= 3.3 V, Rm= 45Ω, CL=10 pF@8 MHz	-	0.5	-	
		V_{DD}= 3.3 V, Rm= 30Ω, CL=5 pF@32 MHz	-	0.8	-	
		V_{DD}= 3.3 V, Rm= 30Ω, CL=10 pF@32 MHz	-	1	-	
		V_{DD}= 3.3 V, Rm= 30Ω, CL=20 pF@32 MHz	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 17*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 19. HSI oscillator accuracy characterization results for soldered parts



Low-speed internal (LSI) RC oscillator

Table 41. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption	-	0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

The parameters given in *Table 42* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 19*.

Table 42. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)	-	24(2)	MHz
	PLL input clock duty cycle	40(2)	-	60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)	-	72	MHz
t_{LOCK}	PLL lock time	-	-	200(2)	µs
Jitter	Cycle-to-cycle jitter	-	-	300(2)	ps

1. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design, not tested in production.

Table 51. Asynchronous multiplexed PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	4THCLK-1	4THCLK+1	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	THCLK	THCLK+0.5	
$t_{w(NWE)}$	FMC_NWE low time	2THCLK-0.5	2THCLK+1	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	THCLK-0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	5	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	1	2.5	
$t_{w(NADV)}$	FMC_NADV low time	THCLK-2	THCLK+2	
$t_{h(AD\_NADV)}$	FMC_AD(adress) valid hold time after FMC_NADV high)	THCLK-2	-	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	THCLK-1	-	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	THCLK-0.5	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	1	
$t_{v(Data\_NADV)}$	FMC_NADV high to Data valid	-	THCLK +3.5	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	THCLK +0.5	-	

1. Based on characterization, not tested in production.

Table 52. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	9THCLK	9THCLK+0.5	ns
$t_{w(NWE)}$	FMC_NWE low time	6THCLK	6THCLK+2	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	5THCLK+6	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	5THCLK-5	-	

1. Based on characterization, not tested in production.

Synchronous waveforms and timings

Figure 24 and *Figure 27* present the synchronous waveforms and *Table 53* to *Table 56* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1;
- DataLatency = 2 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the THCLK is the HCLK clock period (with maximum FMC_CLK = 36 MHz).

Table 55. Synchronous non-multiplexed NOR/PSRAM read timings(1) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	5	-	ns
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. Based on characterization, not tested in production.

Figure 27. Synchronous non-multiplexed PSRAM write timings

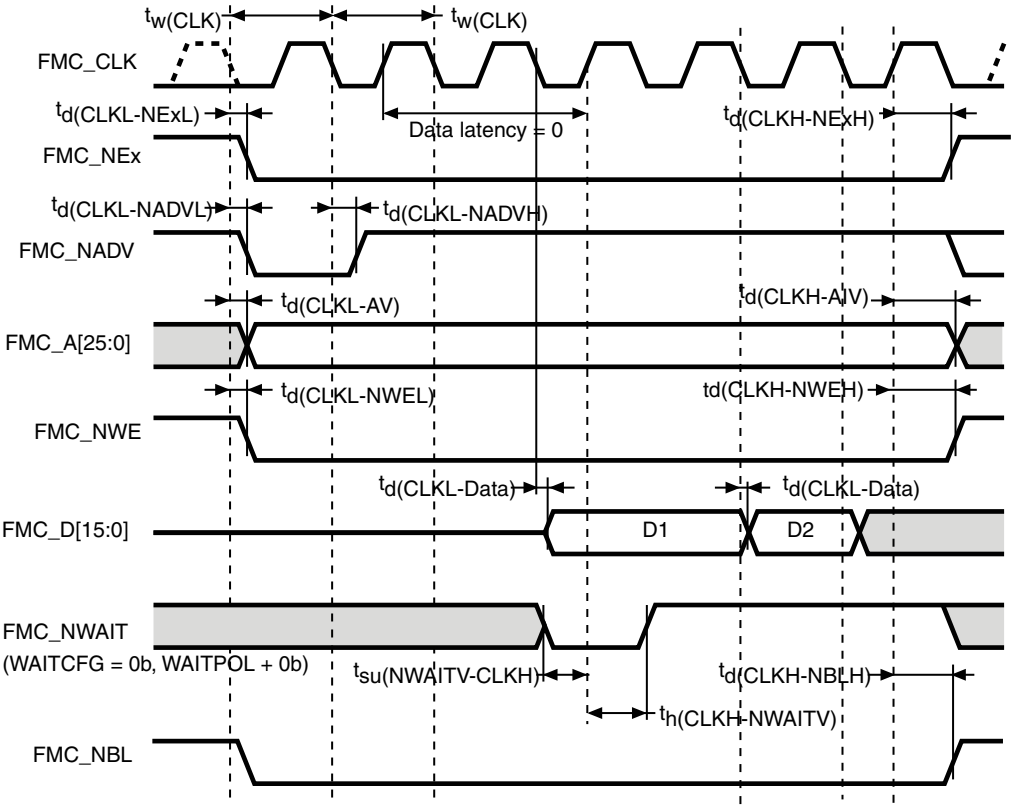


Figure 32. PC Card/CompactFlash controller waveforms for I/O space read access

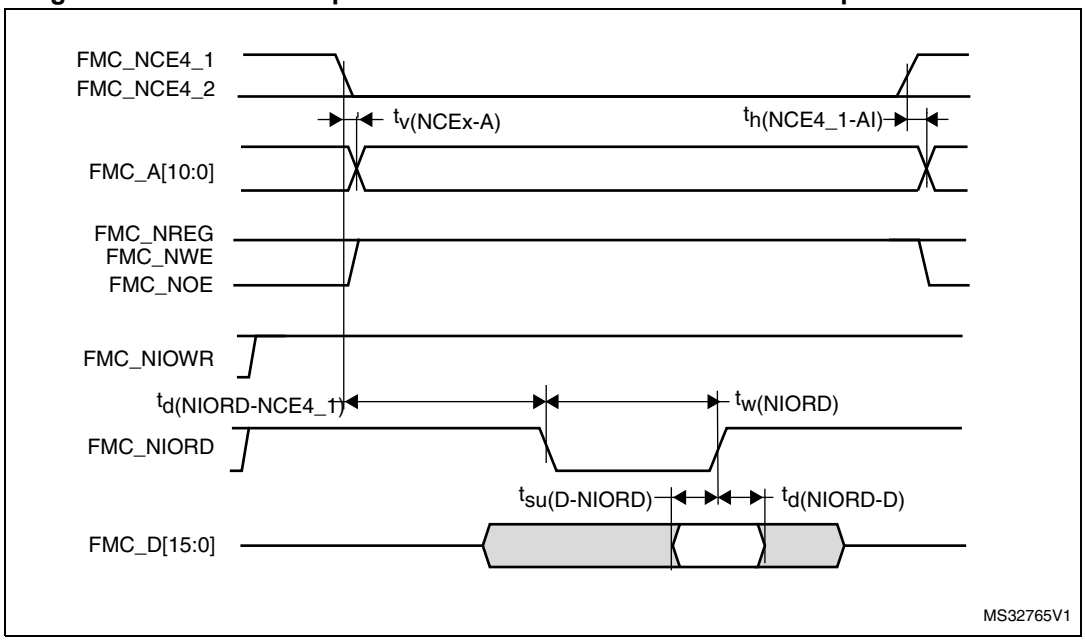
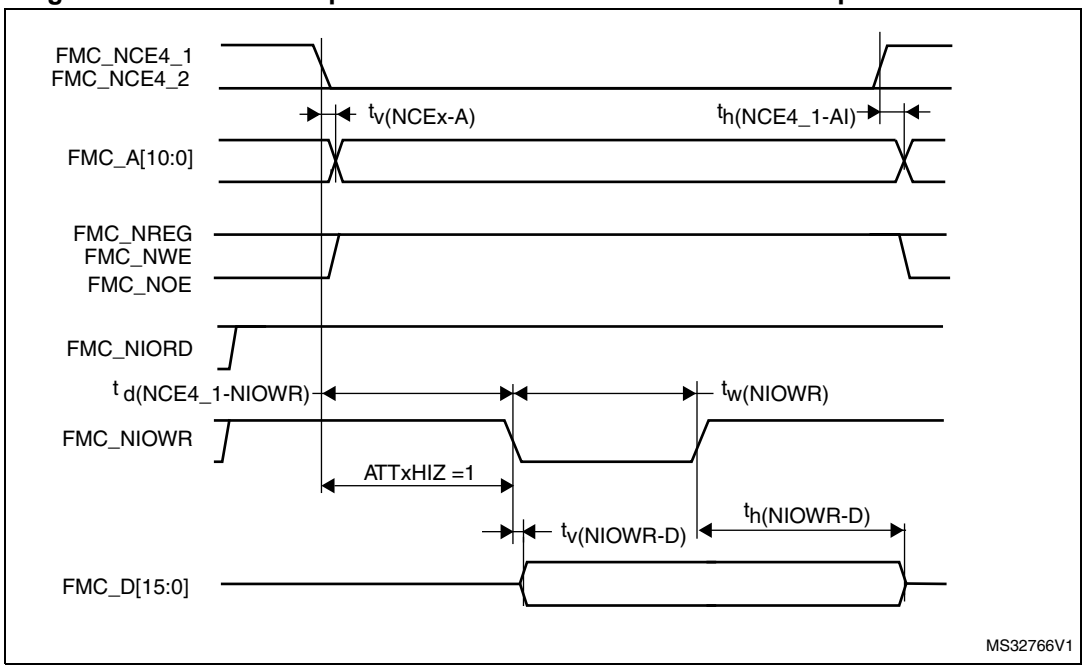


Figure 33. PC Card/CompactFlash controller waveforms for I/O space write access



Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 40* and *Table 68*, respectively.

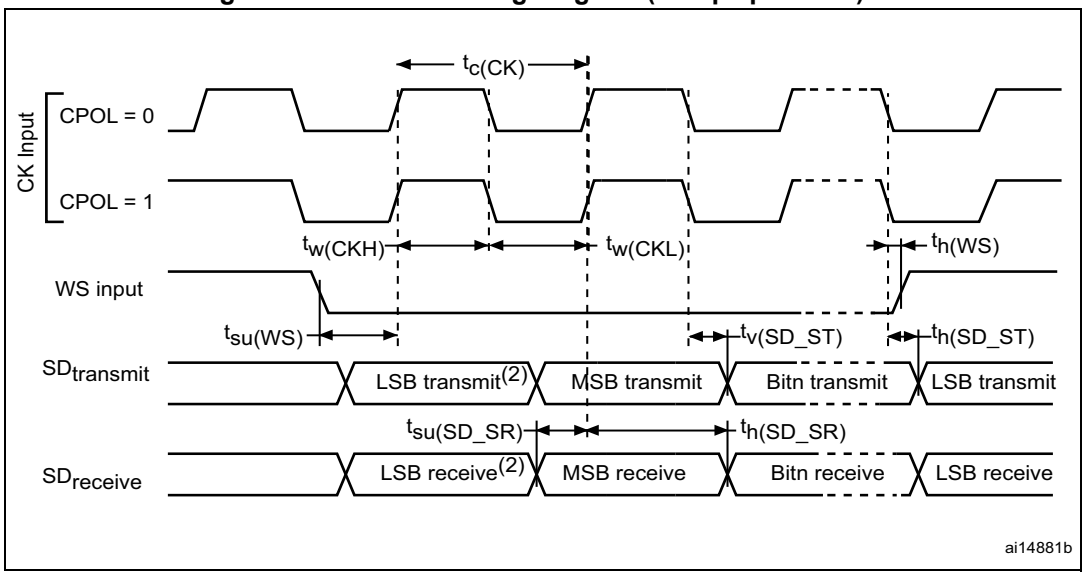
Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 19*.

Table 68. I/O AC characteristics(1)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	2(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	10(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25(3)	
11	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	50(3)	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	30(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	20(3)	
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
FM+ configuration(4)	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 to 3.6 V	-	2(4)	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	12(4)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	34(4)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10(3)	-	ns

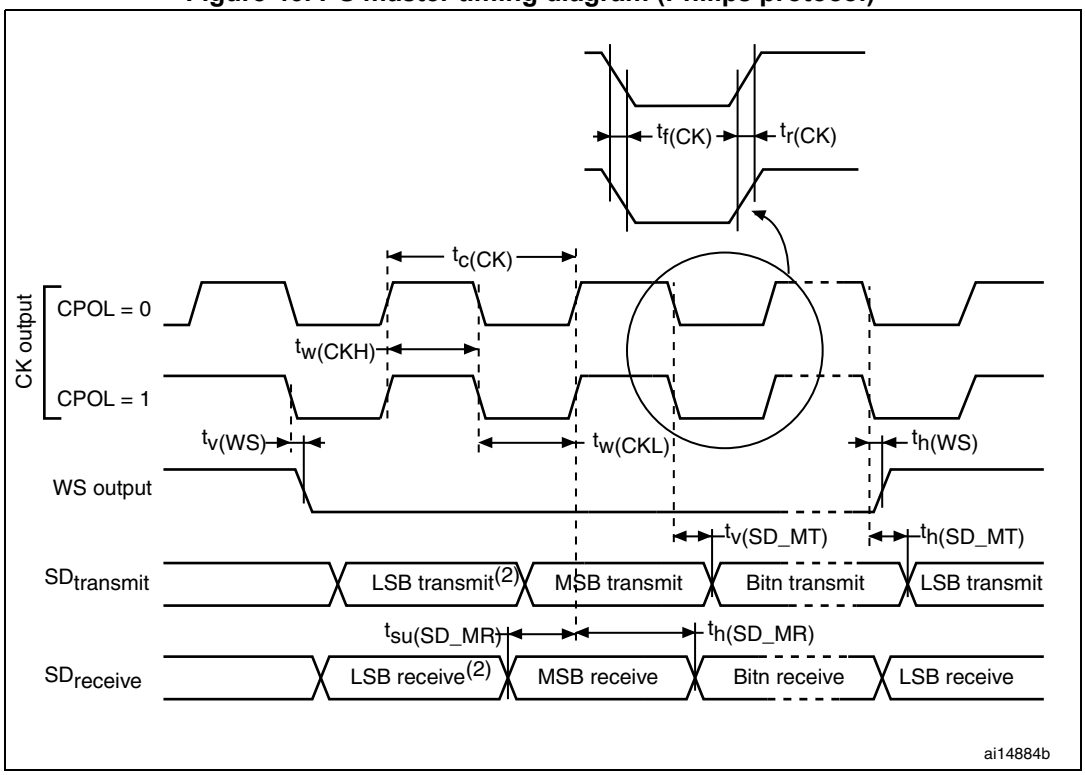
1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0316 reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 40*.
3. Guaranteed by design, not tested in production.
4. The I/O speed configuration is bypassed in FM+ I/O mode. Refer to the reference manual RM0316 for a description of FM+ I/O mode configuration.

Figure 45. I²S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L=30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 46. I²S master timing diagram (Philips protocol)(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L=30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Table 80. Maximum ADC R_{AIN} (1) (continued)

Resolution	Sampling cycle @ 72 MHz	Sampling time [ns] @ 72 MHz	R_{AIN} max (kΩ)		
			Fast channels(2)	Slow channels	Other channels(3)
8 bits	1.5	20.83	0.150	NA	0.039
	2.5	34.72	0.390	0.180	0.180
	4.5	62.50	0.820	0.560	0.470
	7.5	104.17	1.50	1.20	1.00
	19.5	270.83	3.90	3.30	2.70
	61.5	854.17	12.00	12.00	8.20
	181.5	2520.83	39.00	33.00	27.00
	601.5	8354.17	100.00	100.00	82.00
6 bits	1.5	20.83	0.270	0.100	0.150
	2.5	34.72	0.560	0.390	0.330
	4.5	62.50	1.200	0.820	0.820
	7.5	104.17	2.20	1.80	1.50
	19.5	270.83	5.60	4.70	3.90
	61.5	854.17	18.0	15.0	12.0
	181.5	2520.83	56.0	47.0	39.0
	601.5	8354.17	100.00	100.0	100.0

1. Data based on characterization results, not tested in production.
2. All fast channels, expect channels on PA2, PA6, PB1, PB12.
3. Fast channels available on PA2, PA6, PB1, PB12.

Table 81. ADC accuracy - limited test conditions, 100-/144-pin packages (1)(2) (continued)

Symbol	Parameter	Conditions			Min (3)	Typ	Max (3)	Unit
SNR(4)	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz Sampling freq ≤ 5 Msps $V_{DDA} = V_{REF+} = 3.3$ V 25°C 100-pin/144-pin package	Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	
THD(4)	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-76	-76	
				Slow channel 4.8 Ms	-	-76	-76	
			Differential	Fast channel 5.1 Ms	-	-80	-80	
				Slow channel 4.8 Ms	-	-80	-80	

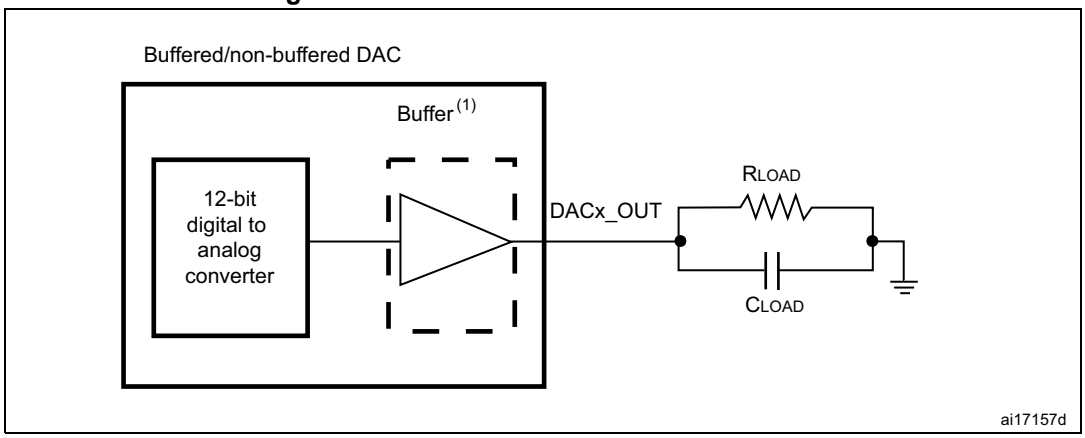
1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.15* does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.
4. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Table 82. ADC accuracy, 100-pin/144-pin packages(1)(2)(3)

Symbol	Parameter	Conditions			Min (4)	Max(4)	Unit
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps 2.0 V ≤ V_{DDA}, V_{REF+} ≤ 3.6 V 100-pin/144-pin package	Single Ended	Fast channel 5.1 Ms	-	±6.5	LSB
				Slow channel 4.8 Ms	-	±6.5	
			Differential	Fast channel 5.1 Ms	-	±4	
				Slow channel 4.8 Ms	-	±4	
EO	Offset error		Single Ended	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2	
EG	Gain error		Single Ended	Fast channel 5.1 Ms	-	±6	
				Slow channel 4.8 Ms	-	±6	
			Differential	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3	
ED	Differential linearity error		Single Ended	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
			Differential	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	

2. Quiescent mode refers to the state of the DAC a keeping steady value on the output, so no dynamic consumption is involved.
3. Data based on characterization results, not tested in production.

Figure 52. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.21 Comparator characteristics

Table 87. Comparator characteristics(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage	-	2	-	3.6	V
V_{IN}	Comparator input voltage range	-	0	-	V_{DDA}	
V_{BG}	Scaler input voltage	-	-	$V_{REFINIT}$	-	
V_{SC}	Scaler offset voltage	-	-	±5	±10	mV
t_{S_SC}	Scaler startup time from power down	-	-	-	0.2	ms
t_{START}	Comparator startup time	$V_{DDA} \geq 2.7$ V	-	-	4	µs
		$V_{DDA} < 2.7$ V	-	-	10	
t_D	Propagation delay for 200 mV step with 100 mV overdrive	$V_{DDA} \geq 2.7$ V	-	25	28	ns
		$V_{DDA} < 2.7$ V	-	28	30	
	Propagation delay for full range step with 100 mV overdrive	$V_{DDA} \geq 2.7$ V	-	32	35	
		$V_{DDA} < 2.7$ V	-	35	40	
V_{OFFSET}	Comparator offset error	$V_{DDA} \geq 2.7$ V	-	±5	±10	mV
		$V_{DDA} < 2.7$ V	-	-	±25	

Table 87. Comparator characteristics(1) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
TV_{OFFSET}	Total offset variation	Full temperature range	-	-	3	mV
I_{DDA}	COMP current consumption	-	-	400	600	µA

1. Guaranteed by design, not tested in production.

Table 88. Operational amplifier characteristics(1) (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
PGA gain	Non inverting gain value	-	-	2	-	-
			-	4	-	-
			-	8	-	-
			-	16	-	-
$R_{network}$	R2/R1 internal resistance values in PGA mode (3)	Gain=2	-	5.4/5.4	-	kΩ
		Gain=4	-	16.2/5.4	-	
		Gain=8	-	37.8/5.4	-	
		Gain=16	-	40.5/2.7	-	
PGA gain error	PGA gain error	-	-1%	-	1%	-
I_{bias}	OPAMP input bias current	-	-	-	±0.2(4)	µA
PGA BW	PGA bandwidth for different non inverting gain	PGA Gain = 2, Cload = 50pF, Rload = 4 KΩ	-	4	-	MHz
		PGA Gain = 4, Cload = 50pF, Rload = 4 KΩ	-	2	-	
		PGA Gain = 8, Cload = 50pF, Rload = 4 KΩ	-	1	-	
		PGA Gain = 16, Cload = 50pF, Rload = 4 KΩ	-	0.5	-	
en	Voltage noise density	@ 1KHz, Output loaded with 4 KΩ	-	109	-	$\frac{nV}{\sqrt{Hz}}$
		@ 10KHz, Output loaded with 4 KΩ	-	43	-	

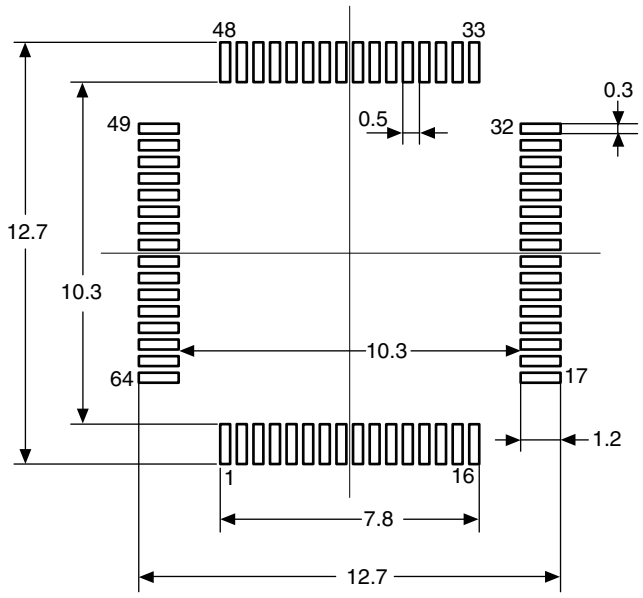
1. Guaranteed by design, not tested in production.
2. The saturation voltage can be also limited by the Iload (drive current).
3. R2 is the internal resistance between OPAMP output and OPAMP inverting input.
   R1 is the internal resistance between OPAMP inverting input and ground.
   The PGA gain =1+R2/R1
4. Mostly TTa I/O leakage, when used in analog mode.

Table 98. LQFP64 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 67. Recommended footprint for the LQFP64 package



1. Dimensions are expressed in millimeters.

Refer to *Figure 69* to select the required temperature range (suffix 6 or 7) according to your temperature or power requirements.

Figure 69. LQFP100 P_D max vs. T_A