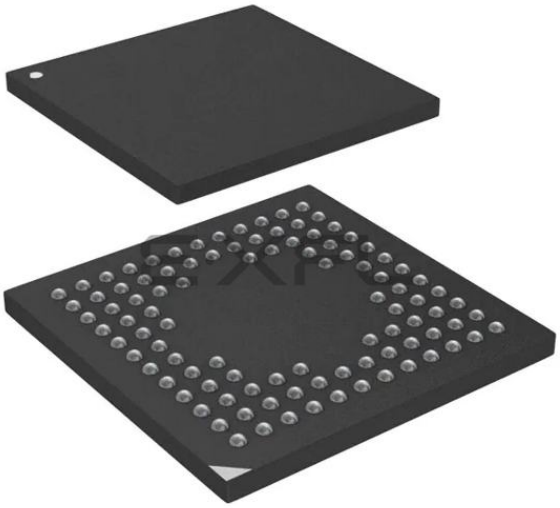

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	84
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 39x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f303veh7tr

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced	TIM1, TIM8, TIM20	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	Yes
General-purpose	TIM2	32-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3, TIM4	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Note: TIM1/8/20/2/3/4/15/16/17 can have PLL as clock source, and therefore can be clocked at 144 MHz.

3.18.1 Advanced timers (TIM1, TIM8, TIM20)

The advanced-control timers (TIM1, TIM8, TIM20) can each be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timers (described in *Section 3.18.2*) using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

3.18.2 General-purpose timers (TIM2, TIM3, TIM4, TIM15, TIM16, TIM17)

There are up to six synchronizable general-purpose timers embedded in the STM32F303xD/E (see *Table 5* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

3.18.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.19 Real-time clock (RTC) and backup registers

The RTC and the 16 backup registers are supplied through a switch that takes power from either the V_{DD} supply when present or the V_{BAT} pin. The backup registers are sixteen 32-bit registers used to store 64 bytes of user application data when V_{DD} power is not present.

They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Automatic correction for 28, 29 (leap year), 30 and 31 days of the month.
- Two programmable alarms with wake up from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.
- 17-bit Auto-reload counter for periodic interrupt with wakeup from STOP/STANDBY capability.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

3.20 Inter-integrated circuit interface (I^2C)

Up to three I^2C bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes.

Table 13. STM32F303xD/E pin definitions (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	UFBGA100	WLCSP100	LQFP144						
21	30	K4	H7	41	PA5	I/O	TTa	(5)	TIM2_CH1/TIM2_ETR, TSC_G2_IO2, SPI1_SCK, EVENTOUT	ADC2_IN2(3), DAC1_OUT2, COMP1_INM, COMP2_INM, COMP3_INM, COMP4_INM, COMP5_INM, COMP6_INM, COMP7_INM, OPAMP1_VINP, OPAMP2_VINM, OPAMP3_VINP
22	31	L4	H6	42	PA6	I/O	TTa	(5)	TIM16_CH1, TIM3_CH1, TSC_G2_IO3, TIM8_BKIN, SPI1_MISO, TIM1_BKIN, COMP1_OUT, EVENTOUT	ADC2_IN3(3), OPAMP2_VOUT
23	32	M4	K7	43	PA7	I/O	TTa	-	TIM17_CH1, TIM3_CH2, TSC_G2_IO4, TIM8_CH1N, SPI1_MOSI, TIM1_CH1N, EVENTOUT	ADC2_IN4(3), COMP2_INP, OPAMP1_VINP, OPAMP2_VINP
24	33	K5	G6	44	PC4	I/O	TTa	-	EVENTOUT, TIM1_ETR, USART1_TX	ADC2_IN5(3)
25	34	L5	F6	45	PC5	I/O	TTa	-	EVENTOUT, TIM15_BKIN, TSC_G3_IO1, USART1_RX	ADC2_IN11, OPAMP1_VINM, OPAMP2_VINM
26	35	M5	J6	46	PB0	I/O	TTa	-	TIM3_CH3, TSC_G3_IO2, TIM8_CH2N, TIM1_CH2N, EVENTOUT	ADC3_IN12, COMP4_INP, OPAMP2_VINP, OPAMP3_VINP
27	36	M6	K6	47	PB1	I/O	TTa	(5)	TIM3_CH4, TSC_G3_IO3, TIM8_CH3N, TIM1_CH3N, COMP4_OUT, EVENTOUT	ADC3_IN1(3), OPAMP3_VOUT
28	37	L6	K5	48	PB2	I/O	TTa	-	TSC_G3_IO4, EVENTOUT	ADC2_IN12, COMP4_INM, OPAMP3_VINM

Table 13. STM32F303xD/E pin definitions (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	UFBGA100	WLCSP100	LQFP144						
-	-	-	-	49	PF11	I/O	FT	(1)	EVENTOUT, TIM20_ETR	-
-	-	-	-	50	PF12	I/O	FT	(1)	EVENTOUT, TIM20_CH1, FMC_A6	-
-	-	-	-	51	VSS	S	-	-	-	-
-	-	-	-	52	VDD	S	-	(1)	-	-
-	-	-	-	53	PF13	I/O	FT	(1)	EVENTOUT, TIM20_CH2, FMC_A7	-
-	-	-	-	54	PF14	I/O	FT	(1)	EVENTOUT, TIM20_CH3, FMC_A8	-
-	-	-	-	55	PF15	I/O	FT	(1)	EVENTOUT, TIM20_CH4, FMC_A9	-
-	-	-	-	56	PG0	I/O	FT	(1)	EVENTOUT, TIM20_CH1N, FMC_A10	-
-	-	-	-	57	PG1	I/O	FT	(1)	EVENTOUT, TIM20_CH2N, FMC_A11	-
-	38	M7	F8	58	PE7	I/O	TTa	(1)	EVENTOUT, TIM1_ETR, FMC_D4	ADC3_IN13
-	39	L7	E6	59	PE8	I/O	TTa	(1)	EVENTOUT, TIM1_CH1N, FMC_D5	ADC34_IN6, COMP4_INM
-	40	M8	-	60	PE9	I/O	TTa	(1)	EVENTOUT, TIM1_CH1, FMC_D6	ADC3_IN2(3)
-	-	-	-	61	VSS	S	-	(1)	-	-
-	-	-	-	62	VDD	S	-	(1)	-	-
-	41	L8	-	63	PE10	I/O	TTa	(1)	EVENTOUT, TIM1_CH2N, FMC_D7	ADC3_IN14
-	42	M9	H5	64	PE11	I/O	TTa	(1)	EVENTOUT, TIM1_CH2, SPI4_NSS, FMC_D8	ADC3_IN15
-	43	L9	G5	65	PE12	I/O	TTa	(1)	EVENTOUT, TIM1_CH3N, SPI4_SCK, FMC_D9	ADC3_IN16
-	44	M10	-	66	PE13	I/O	TTa	(1)	EVENTOUT, TIM1_CH3, SPI4_MISO, FMC_D10	ADC3_IN3(3)

Table 13. STM32F303xD/E pin definitions (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	UFBGA100	WLCSP100	LQFP144						
37	63	E12	F4	96	PC6	I/O	FT	-	EVENTOUT, TIM3_CH1, TIM8_CH1, I2S2_MCK, COMP6_OUT	-
38	64	E11	F2	97	PC7	I/O	FT	-	EVENTOUT, TIM3_CH2, TIM8_CH2, I2S3_MCK, COMP5_OUT	-
39	65	E10	F1	98	PC8	I/O	FT	-	EVENTOUT, TIM3_CH3, TIM8_CH3, COMP3_OUT	-
40	66	D12	F3	99	PC9	I/O	FTf	-	EVENTOUT, TIM3_CH4, I2C3_SDA, TIM8_CH4, I2SCKIN, TIM8_BKIN2	-
41	67	D11	F5	100	PA8	I/O	FTf	-	MCO, I2C3_SCL, I2C2_SMBAL, I2S2_MCK, TIM1_CH1, USART1_CK, COMP3_OUT, TIM4_ETR, EVENTOUT	-
42	68	D10	E5	101	PA9	I/O	FTf	-	I2C3_SMBAL, TSC_G4_IO1, I2C2_SCL, I2S3_MCK, TIM1_CH2, USART1_TX, COMP5_OUT, TIM15_BKIN, TIM2_CH3, EVENTOUT	-
43	69	C12	E1	102	PA10	I/O	FTf	-	TIM17_BKIN, TSC_G4_IO2, I2C2_SDA, SPI2_MISO/I2S2ext_SD, TIM1_CH3, USART1_RX, COMP6_OUT, TIM2_CH4, TIM8_BKIN, EVENTOUT	-
44	70	B12	E2	103	PA11	I/O	FT	-	SPI2_MOSI/I2S2_SD, TIM1_CH1N, USART1_CTS, COMP1_OUT, CAN_RX, TIM4_CH1, TIM1_CH4, TIM1_BKIN2, EVENTOUT	USB_DM

Table 13. STM32F303xD/E pin definitions (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	UFBGA100	WLCSP100	LQFP144						
-	-	-	-	129	PG14	I/O	FT	(1)	EVENTOUT, FMC_A25	-
-	-	-	-	130	VSS	S	-	(1)	-	-
-	-	-	-	131	VDD	S	-	(1)	-	-
-	-	-	-	132	PG15	I/O	FT	(1)	EVENTOUT	-
55	89	A8	A5	133	PB3	I/O	FT	-	JTDO-TRACESWO, TIM2_CH2, TIM4_ETR, TSC_G5_IO1, TIM8_CH1N, SPI1_SCK, SPI3_SCK/I2S3_CK, USART2_TX, TIM3_ETR, EVENTOUT	-
56	90	A7	B5	134	PB4	I/O	FT	-	JTRST, TIM16_CH1, TIM3_CH1, TSC_G5_IO2, TIM8_CH2N, SPI1_MISO, SPI3_MISO/I2S3ext_SD, USART2_RX, TIM17_BKIN, EVENTOUT	-
57	91	C5	A6	135	PB5	I/O	FTf	-	TIM16_BKIN, TIM3_CH2, TIM8_CH3N, I2C1_SMBAI, SPI1_MOSI, SPI3_MOSI/I2S3_SD, USART2_CK, I2C3_SDA, TIM17_CH1, EVENTOUT	-
58	92	B5	B6	136	PB6	I/O	FTf	-	TIM16_CH1N, TIM4_CH1, TSC_G5_IO3, I2C1_SCL, TIM8_CH1, TIM8_ETR, USART1_TX, TIM8_BKIN2, EVENTOUT	-
59	93	B4	C5	137	PB7	I/O	FTf	-	TIM17_CH1N, TIM4_CH2, TSC_G5_IO4, I2C1_SDA, TIM8_BKIN, USART1_RX, TIM3_CH4, FMC_NADV, EVENTOUT	-
60	94	A4	A7	138	BOOT0	I	-	-	-	-

Table 14. STM32F303xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3/TIM8/20/15/GPCOMP7/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/TIM8/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP3/5/6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port E	PE12	-	EVENT OUT	TIM1_CH3N	-	-	SPI4_SCK	-	-	-	-	-	-	FMC_D9	-	-	-
	PE13	-	EVENT OUT	TIM1_CH3	-	-	SPI4_MISO	-	-	-	-	-	-	FMC_D10	-	-	-
	PE14	-	EVENT OUT	TIM1_CH4	-	-	SPI4_MOSI	TIM1_BKIN2	-	-	-	-	-	FMC_D11	-	-	-
	PE15	-	EVENT OUT	TIM1_BKIN	-	-	-	-	USART3_RX	-	-	-	-	FMC_D12	-	-	-
Port F	PF0	-	EVENT OUT	-	-	I2C2_SDA	SPI2_NSS/I2S2_WS	TIM1_CH3N	-	-	-	-	-	-	-	-	-
	PF1	-	EVENT OUT	-	-	I2C2_SCL	SPI2_SCK/I2S2_CK	-	-	-	-	-	-	-	-	-	-
	PF2	-	EVENT OUT	TIM20_CH3	-	-	-	-	-	-	-	-	-	FMC_A2	-	-	-
	PF3	-	EVENT OUT	TIM20_CH4	-	-	-	-	-	-	-	-	-	FMC_A3	-	-	-
	PF4	-	EVENT OUT	COMP1_OUT	TIM20_CH1N	-	-	-	-	-	-	-	-	FMC_A4	-	-	-
	PF5	-	EVENT OUT	TIM20_CH2N	-	-	-	-	-	-	-	-	-	FMC_A5	-	-	-
	PF6	-	EVENT OUT	TIM4_CH4	-	I2C2_SCL	-	-	USART3_RTS	-	-	-	-	FMC_NIORD	-	-	-
	PF7	-	EVENT OUT	TIM20_BKIN	-	-	-	-	-	-	-	-	-	FMC_NREG	-	-	-

6.3.10 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 43. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	53.5	60	µs
t_{ERASE}	Page (2 KB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design, not tested in production.

Table 44. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycle(2) at T_A = 55 °C	20	

1. Data based on characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

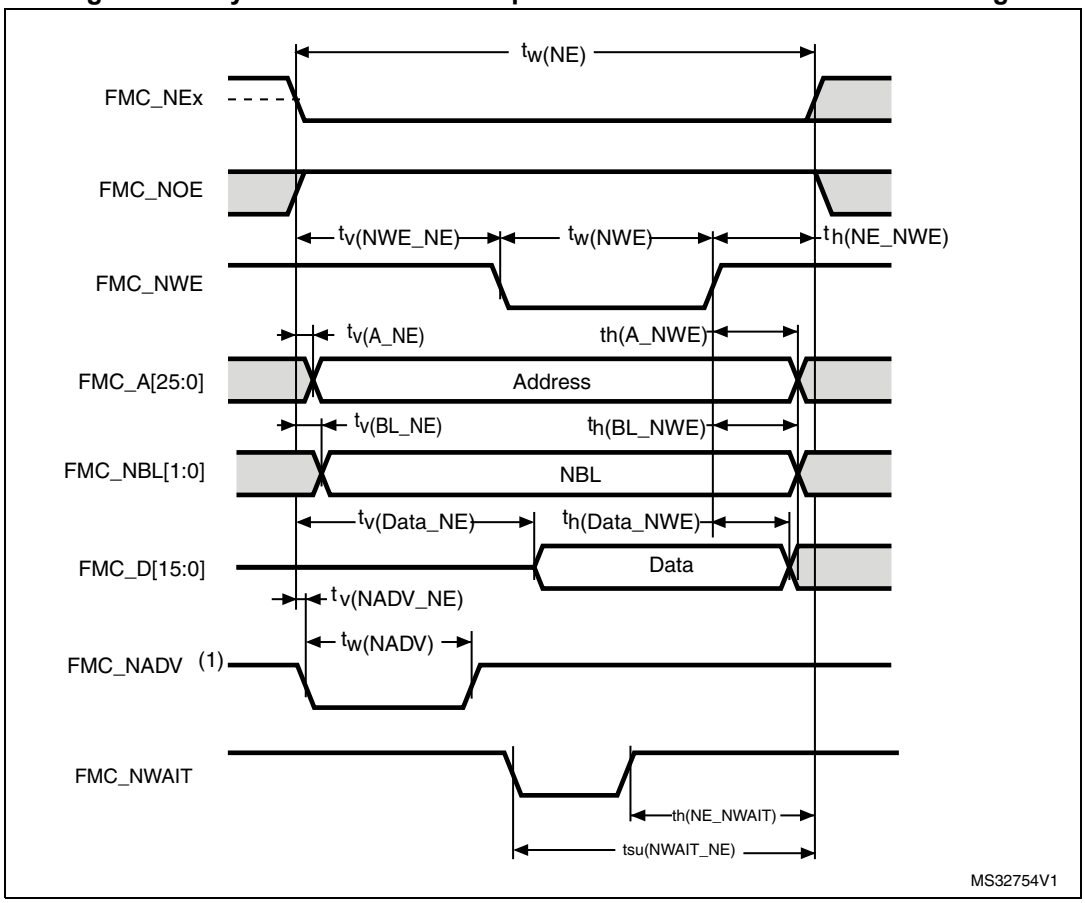
6.3.11 FSMC characteristics

Unless otherwise specified, the parameters given in *Table 45* to *Table 60* for the FSMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 19* with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5VDD

Refer to *Section 6.3.15: I/O port characteristics*: for more details on the input/output characteristics.

Figure 21. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 47. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	3THCLK-1	3THCLK+2	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	THCLK+0.5	THCLK+1	
$t_{w(NWE)}$	FMC_NWE low time	THCLK-2	THCLK+1	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	THCLK-0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	THCLK-1.5	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	1	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	THCLK-0.5	-	
$t_{v(Data\_NE)}$	Data to FMC_NEx low to Data valid	-	THCLK+ 3	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	THCLK+0.5	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	2.5	
$t_{w(NADV)}$	FMC_NADV low time	-	THCLK+2	

1. Based on characterization, not tested in production.

Table 53. Synchronous multiplexed NOR/PSRAM read timings(1) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	ns
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	4	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	6	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. Based on characterization, not tested in production.

Figure 25. Synchronous multiplexed PSRAM write timings

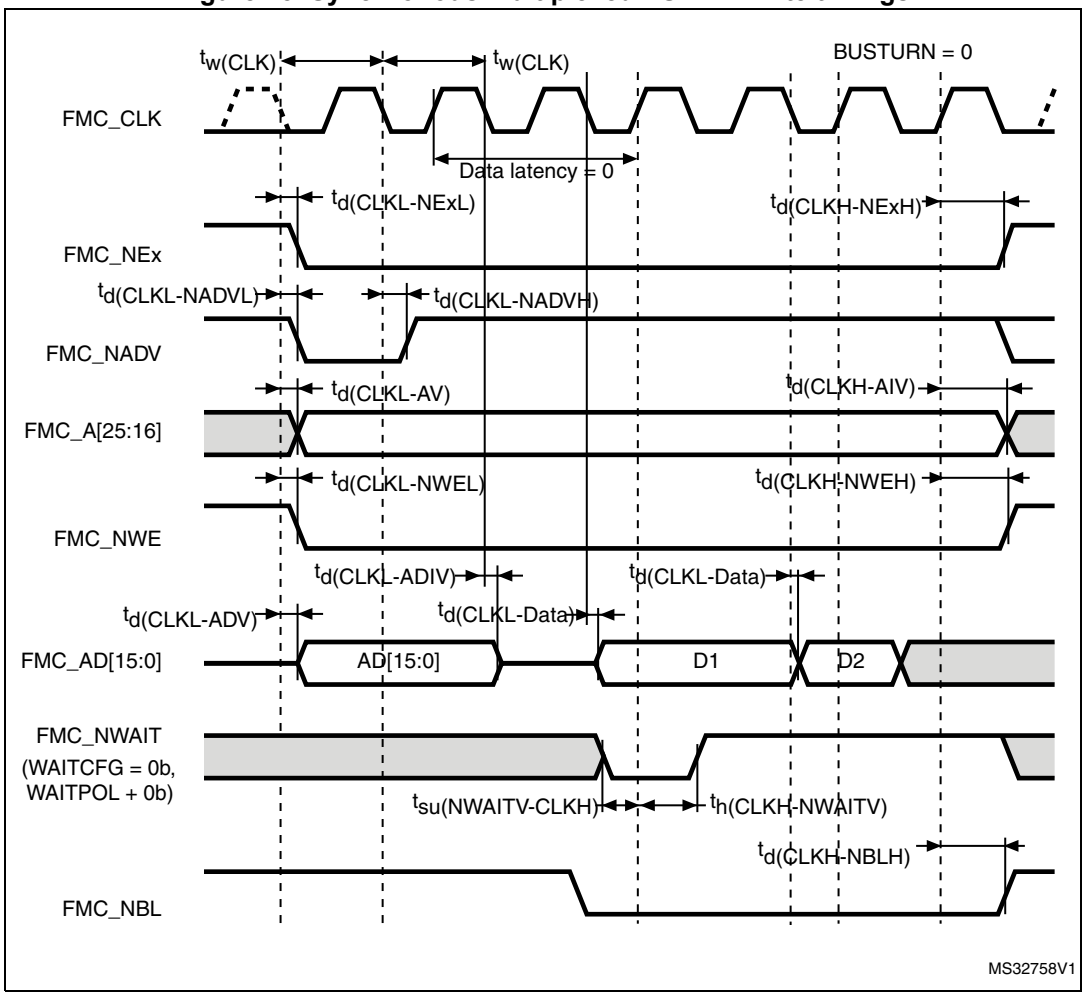


Table 54. Synchronous multiplexed PSRAM write timings(1) (2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period, VDD range= 2.7 to 3.6 V	2THCLK-1	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	5.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	THCLK+1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	7	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	2	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	0	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	0	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	5.5	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	THCLK+1	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	7.5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	8	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	6	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	THCLK+1	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	5	-	

1. Based on characterization, not tested in production.
2. C_L = 30 pF.

6.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling two LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 61*. They are based on the EMS levels and classes defined in application note AN1709.

Table 61. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

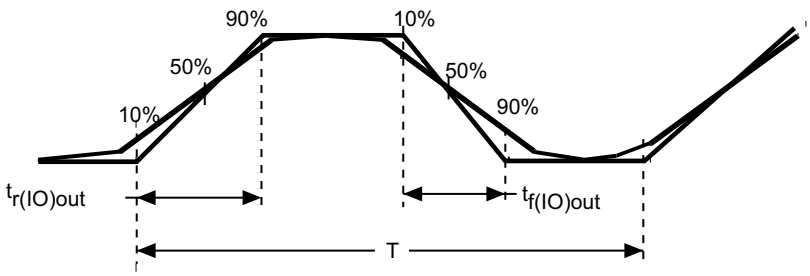
Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Figure 40. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \le 2/3)T$ and if the duty cycle is (45-55%) when loaded by C_L (1)

MS36445V1

1. See *Table 68: I/O AC characteristics*.

6.3.16 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 66*).

Unless otherwise specified, the parameters given in *Table 69* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 19*.

Table 69. NRST pin characteristics

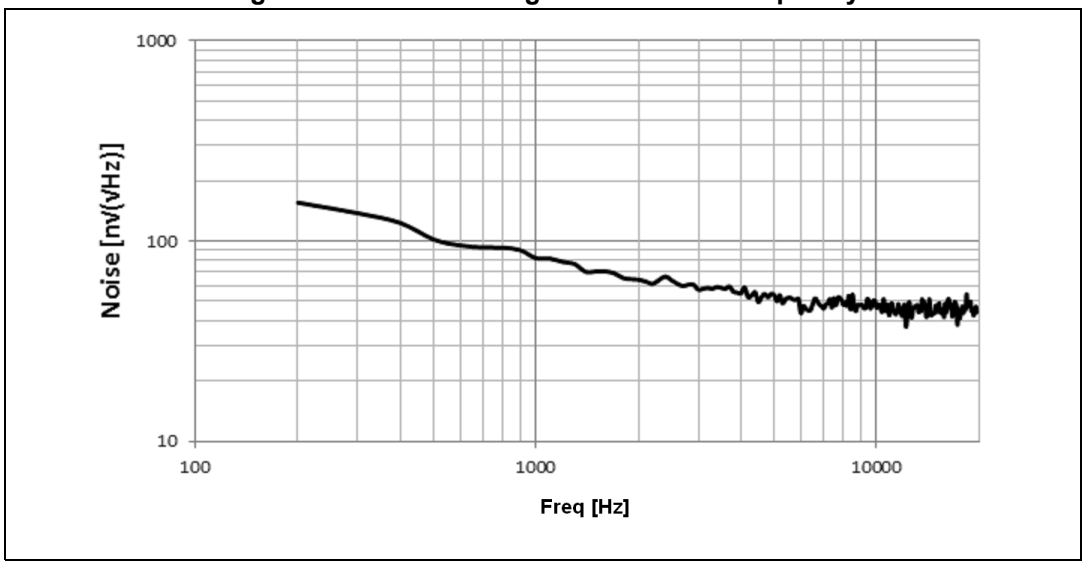
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$ (1)	NRST Input low level voltage	-	-	-	$0.3V_{DD}+0.07$ (1)	V
$V_{IH(NRST)}$ (1)	NRST Input high level voltage	-	$0.445V_{DD}+0.398$ (1)	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor (2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$ (1)	NRST Input filtered pulse	-	-	-	100 (1)	ns
$V_{NF(NRST)}$ (1)	NRST Input not filtered pulse	-	500 (1)	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Table 81. ADC accuracy - limited test conditions, 100-/144-pin packages (1)(2)

Symbol	Parameter	Conditions			Min (3)	Typ	Max (3)	Unit
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz Sampling freq. ≤ 5 Msps $V_{DDA} = V_{REF+} = 3.3$ V 25°C 100-pin/144-pin package	Single ended	Fast channel 5.1 Ms	-	±3.5	±4.5	LSB
				Slow channel 4.8 Ms	-	±4	±4.5	
			Differential	Fast channel 5.1 Ms	-	±3	±3	
				Slow channel 4.8 Ms	-	±3	±3	
EO	Offset error		Single ended	Fast channel 5.1 Ms	-	±1	±1.5	
				Slow channel 4.8 Ms	-	±1	±2.5	
			Differential	Fast channel 5.1 Ms	-	±1	±1.5	
				Slow channel 4.8 Ms	-	±1	±1.5	
EG	Gain error		Single ended	Fast channel 5.1 Ms	-	±3	±4	
				Slow channel 4.8 Ms	-	±3.5	±4	
			Differential	Fast channel 5.1 Ms	-	±1.5	±2.5	
				Slow channel 4.8 Ms	-	±2	±2.5	
ED	Differential linearity error		Single ended	Fast channel 5.1 Ms	-	±1	±1.5	
				Slow channel 4.8 Ms	-	±1	±1.5	
			Differential	Fast channel 5.1 Ms	-	±1	±1	
				Slow channel 4.8 Ms	-	±1	±1	
EL	Integral linearity error		Single ended	Fast channel 5.1 Ms	-	±1.5	±2	
				Slow channel 4.8 Ms	-	±1.5	±3	
			Differential	Fast channel 5.1 Ms	-	±1	±1.5	
				Slow channel 4.8 Ms	-	±1	±1.5	
ENOB(4)	Effective number of bits		Single ended	Fast channel 5.1 Ms	10.7	10.8	-	bits
				Slow channel 4.8 Ms	10.7	10.8	-	
			Differential	Fast channel 5.1 Ms	11.2	11.3	-	
				Slow channel 4.8 Ms	11.1	11.3	-	
SINAD(4)	Signal-to-noise and distortion ratio		Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	

Figure 53. OPAMP voltage noise versus frequency



6.3.23 Temperature sensor characteristics

Table 89. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(1)	Startup time	4	-	10	µs
T_{S_temp}(1)(2)	ADC sampling time when reading the temperature	2.2	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

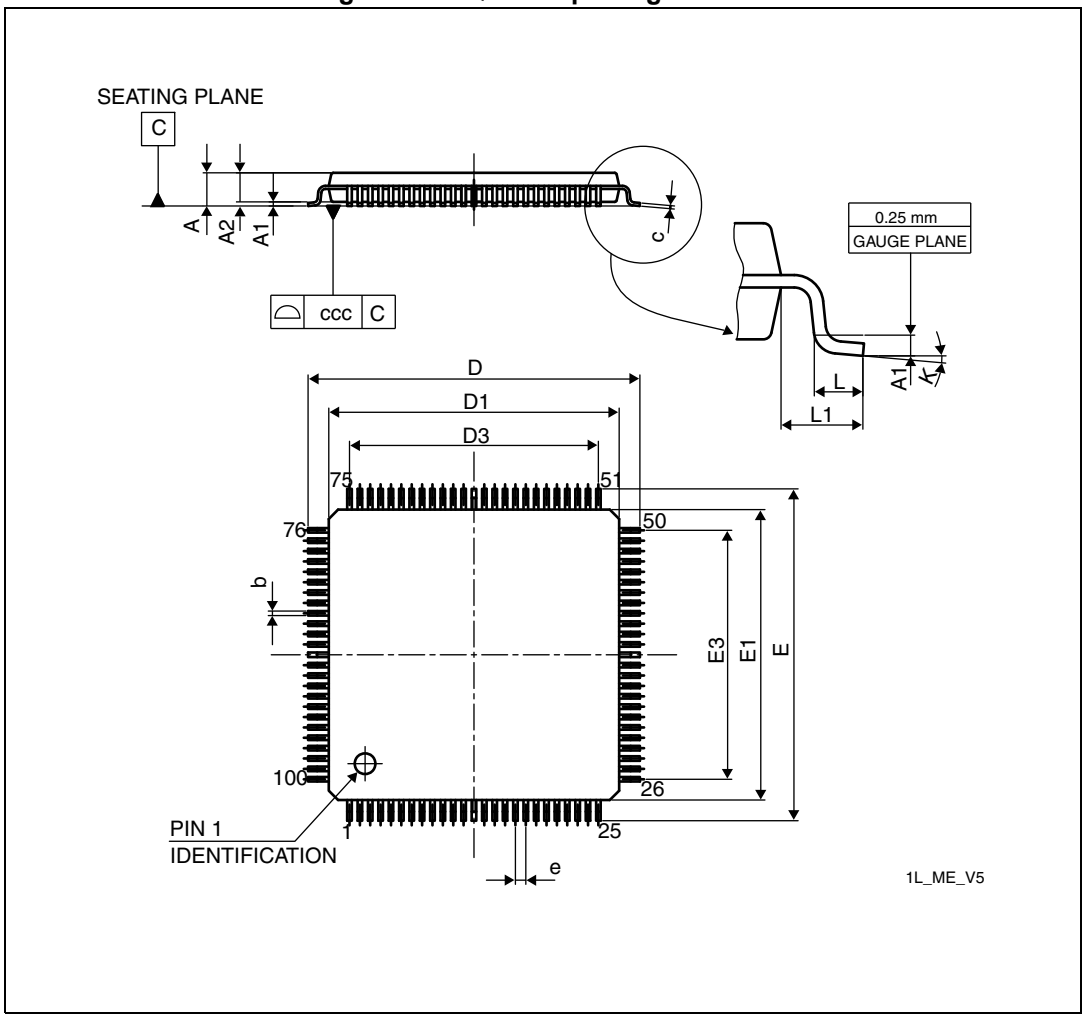
Table 90. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

7.4 LQFP100 package information

LQFP100 is a 100-pin, 14 x 14 mm low-profile quad flat package.

Figure 60. LQFP100 package outline



1. Drawing is not to scale.

Table 95. LQPF100 package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378

7.7 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 19: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum temperature in °C,
- Θ_{JA} is the package junction-to- thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 99. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-** LQFP144 - 20 × 20 mm	33	°C/W
	Thermal resistance junction- UFBGA100 - 7 × 7 mm	59	
	Thermal resistance junction- LQFP100 - 14 × 14 mm	42	
	Thermal resistance junction- WLCSP100 - 0.4 mm pitch	44	
	Thermal resistance junction- LQFP64 - 10 × 10 mm / 0.5 mm pitch	46	

7.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.7.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Part numbering*.

Each temperature range suffix corresponds to a specific guaranteed temperature at maximum dissipation and to a specific maximum junction temperature.

As applications do not commonly use the STM32F303xD/E at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range is best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in *Table 99* T_{Jmax} is calculated as follows:

– For LQFP100, 42 °C/W

T_{Jmax} = 82 °C + (42 °C/W × 447 mW) = 82 °C + 18.774 °C = 100.774 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Part numbering*).

Note: With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 7).

Suffix 6: T_{Amax} = T_{Jmax} - (42°C/W × 447 mW) = 105-18.774 = 86.226 °C

Suffix 7: T_{Amax} = T_{Jmax} - (42°C/W × 447 mW) = 125-18.774 = 106.226 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high temperature with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 99* T_{Jmax} is calculated as follows:

– For LQFP100, 42 °C/W

T_{Jmax} = 100 °C + (42 °C/W × 134 mW) = 100 °C + 5.628 °C = 105.628 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Part numbering*) unless we reduce the power dissipation to be able to use suffix 6 parts.