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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	86
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 39x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f303vet6tr

List of tables

Table 2. STM32F303xD/E family device features and peripheral counts (continued)

Peripheral	STM32F303Rx	STM32F303Vx	STM32F303Zx
Operating temperature	Ambient operating temperature: - 40 to 85 °C / - 40 to 105 °C Junction temperature: - 40 to 125 °C		
Packages	LQFP64	LQFP100 WLCSP100 UFBGA100	LQFP144

1. TIM1 and TIM8 are the two available advanced timers.
2. This total number considers also the PWMs generated on the complementary output channels.
3. The SPI interfaces works in an exclusive way in either the SPI mode or the I^2S audio mode.

3.7.4 Low-power modes

The STM32F303xD/E supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- Sleep mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and wake up the CPU when an interrupt/event occurs.

- Stop mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the USB wakeup, the RTC alarm, COMPx, I2Cx or U(S)ARTx.

- Standby mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin or an RTC alarm occurs.

Note: The RTC, the IWDG and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.8 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Table 4. STM32F303xD/E peripheral interconnect matrix

Interconnect source	Interconnect destination	Interconnect action
TIMx	TIMx	Timers synchronization or chaining
	ADCx DAC1	Conversion triggers
	DMA	Memory to memory transfer trigger
	Compx	Comparator output blanking
COMPx	TIMx	Timer input: OCREF_CLR input, input capture
ADCx	TIMx	Timer triggered by analog watchdog

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced	TIM1, TIM8, TIM20	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	Yes
General-purpose	TIM2	32-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3, TIM4	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Note: TIM1/8/20/2/3/4/15/16/17 can have PLL as clock source, and therefore can be clocked at 144 MHz.

3.18.1 Advanced timers (TIM1, TIM8, TIM20)

The advanced-control timers (TIM1, TIM8, TIM20) can each be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timers (described in *Section 3.18.2*) using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

3.18.2 General-purpose timers (TIM2, TIM3, TIM4, TIM15, TIM16, TIM17)

There are up to six synchronizable general-purpose timers embedded in the STM32F303xD/E (see *Table 5* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

Table 9. STM32F303xD/E SPI/I^2S implementation

SPI features(1)	SPI1	SPI2	SPI3	SPI4
Hardware CRC calculation	X	X	X	X
Rx/Tx FIFO	X	X	X	X
NSS pulse mode	X	X	X	X
I^2S mode	-	X	X	-
TI mode	X	X	X	X

1. X = supported.

3.24 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

3.25 Universal serial bus (USB)

The STM32F303xD/E embeds a full-speed USB device peripheral compliant with the USB specification version 2.0. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 Kbyte (256 bytes are used for CAN peripheral if enabled) and suspend/resume support.

The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

3.26 Infrared transmitter

The STM32F303xD/E devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

Figure 5. STM32F303xD/E LQFP100 pinout

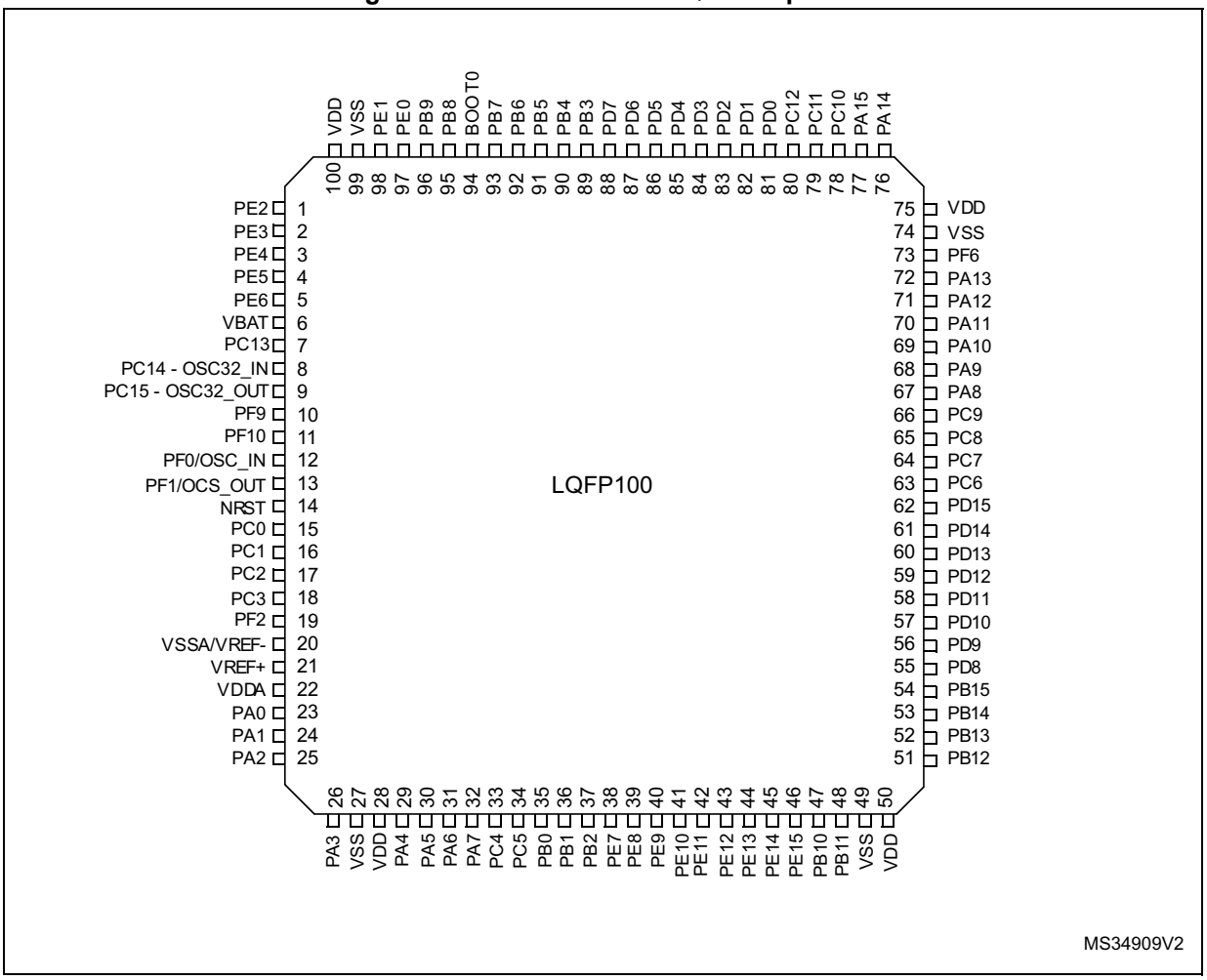


Table 13. STM32F303xD/E pin definitions (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	UFBGA100	WLCSP100	LQFP144						
61	95	A3	D5	139	PB8	I/O	FTf	-	TIM16_CH1, TIM4_CH3, TSC_SYNC, I2C1_SCL, USART3_RX, COMP1_OUT, CAN_RX, TIM8_CH2, TIM1_BKIN, EVENTOUT	-
62	96	B3	C6	140	PB9	I/O	FTf	-	TIM17_CH1, TIM4_CH4, I2C1_SDA, IR-OUT, USART3_TX, COMP2_OUT, CAN_TX, TIM8_CH3, EVENTOUT	-
-	97	C3	B7	141	PE0	I/O	FT	(1)	EVENTOUT, TIM4_ETR, TIM16_CH1, TIM20_ETR, USART1_TX, FMC_NBL0	-
-	98	A2	A8	142	PE1	I/O	FT	(1)	EVENTOUT, TIM17_CH1, TIM20_CH4, USART1_RX, FMC_NBL1	-
63	99	E3	C7	143	VSS	S	-	-	-	-
64	100	C4	A9, A10, B10, B8	144	VDD	S	-	-	-	-

1. Function availability depends on the chosen device.
2. PC13, PC14 and PC15 are supplied through the power switch. Since the switch sinks only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED)

   After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the RM0316 reference manual.
3. Fast ADC channel.
4. The VREF+ functionality is not available on the 64-pin package. In this package, the VREF+ is internally connected to VDDA.
5. These GPIOs offer a reduced touch sensing sensitivity. It is thus recommended to use them as sampling capacitor I/O.

Table 14. STM32F303xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM12/3/4/8/20/15/GPCOMP1	I2C3/TIM8/20/15/GPCOMP7/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/TIM8/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP3/5/6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port F	PF8	-	EVENT OUT	TIM20_BKIN2	-	-	-	-	-	-	-	-	-	FMC_NIOWR	-	-	-
	PF9	-	EVENT OUT	TIM20_BKIN	TIM15_CH1	-	SPI2_SCK	-	-	-	-	-	-	FMC_CD	-	-	-
	PF10	-	EVENT OUT	TIM20_BKIN2	TIM15_CH2	-	SPI2_SCK	-	-	-	-	-	-	FMC_INTR	-	-	-
	PF11	-	EVENT OUT	TIM20_ETR	-	-	-	-	-	-	-	-	-	-	-	-	-
	PF12	-	EVENT OUT	TIM20_CH1	-	-	-	-	-	-	-	-	-	FMC_A6	-	-	-
	PF13	-	EVENT OUT	TIM20_CH2	-	-	-	-	-	-	-	-	-	FMC_A7	-	-	-
	PF14	-	EVENT OUT	TIM20_CH3	-	-	-	-	-	-	-	-	-	FMC_A8	-	-	-
	PF15	-	EVENT OUT	TIM20_CH4	-	-	-	-	-	-	-	-	-	FMC_A9	-	-	-
Port G	PG0	-	EVENT OUT	TIM20_CH1N	-	-	-	-	-	-	-	-	-	FMC_A10	-	-	-
	PG1	-	EVENT OUT	TIM20_CH2N	-	-	-	-	-	-	-	-	-	FMC_A11	-	-	-
	PG2	-	EVENT OUT	TIM20_CH3N	-	-	-	-	-	-	-	-	-	FMC_A12	-	-	-
	PG3	-	EVENT OUT	TIM20_BKIN	-	-	-	-	-	-	-	-	-	FMC_A13	-	-	-
	PG4	-	EVENT OUT	TIM20_BKIN2	-	-	-	-	-	-	-	-	-	FMC_A14	-	-	-

Table 15. Memory map, peripheral register boundary addresses (continued)

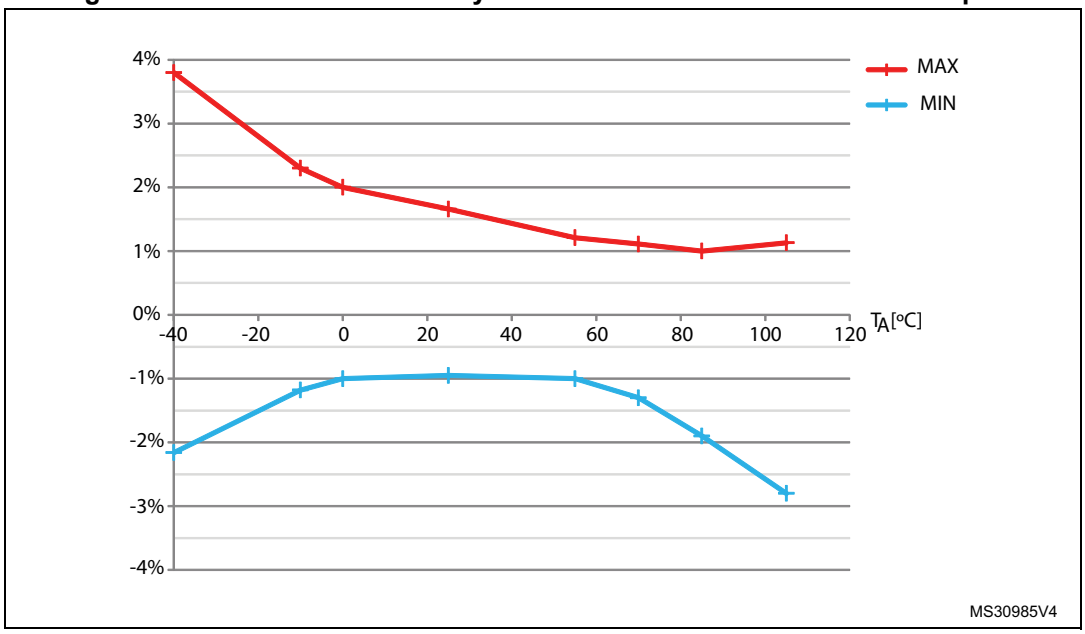
Bus	Boundary address	Size (bytes)	Peripheral
APB1	0x4000 7800 - 0x4000 7BFF	1 K	I2C3
	0x4000 7400 - 0x4000 77FF	1 K	DAC
	0x4000 7000 - 0x4000 73FF	1 K	PWR
	0x4000 6800 - 0x4000 6FFF	2 K	Reserved
	0x4000 6400 - 0x4000 67FF	1 K	bxCAN
	0x4000 6000 - 0x4000 63FF	1 K	USB/CAN SRAM
	0x4000 5C00 - 0x4000 5FFF	1 K	USB device FS
	0x4000 5800 - 0x4000 5BFF	1 K	I2C2
	0x4000 5400 - 0x4000 57FF	1 K	I2C1
	0x4000 5000 - 0x4000 53FF	1 K	UART5
	0x4000 4C00 - 0x4000 4FFF	1 K	UART4
	0x4000 4800 - 0x4000 4BFF	1 K	USART3
	0x4000 4400 - 0x4000 47FF	1 K	USART2
	0x4000 4000 - 0x4000 43FF	1 K	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	1 K	SPI3/I2S3
	0x4000 3800 - 0x4000 3BFF	1 K	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	1 K	I2S2ext
	0x4000 3000 - 0x4000 33FF	1 K	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 K	WWDG
	0x4000 2800 - 0x4000 2BFF	1 K	RTC
	0x4000 1800 - 0x4000 27FF	4 K	Reserved
	0x4000 1400 - 0x4000 17FF	1 K	TIM7
	0x4000 1000 - 0x4000 13FF	1 K	TIM6
	0x4000 0C00 - 0x4000 0FFF	1 K	Reserved
	0x4000 0800 - 0x4000 0BFF	1 K	TIM4
	0x4000 0400 - 0x4000 07FF	1 K	TIM3
	0x4000 0000 - 0x4000 03FF	1 K	TIM2

Table 33. Peripheral current consumption (continued)

Peripheral	Typical consumption(1)	Unit
	I_{DD}	
APB1-Bridge (3)	6.7	µA/MHz
TIM2	39.2	
TIM3	30.8	
TIM4	31.3	
TIM6	4.3	
TIM7	4.3	
WWDG	1.3	
SPI2	33.6	
SPI3	33.9	
USART2	39.3	
USART3	39.3	
UART4	29.8	
UART5	27.0	
I2C1	6.7	
I2C2	6.4	
USB	14.7	
CAN	25.6	
PWR	3.7	
DAC	22.1	
I2C3	6.8	

1. The power consumption of the analog part (I_{DDA}) of peripherals such as ADC, DAC, Comparators, OpAmp is not included. Refer to the tables of characteristics in the subsequent sections.
2. BusMatrix is automatically active when at least one master is ON (CPU, DMA1 or DMA2).
3. The APBx bridge is automatically active when at least one peripheral is ON on the same bus.

Figure 19. HSI oscillator accuracy characterization results for soldered parts



Low-speed internal (LSI) RC oscillator

Table 41. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption	-	0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

The parameters given in *Table 42* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 19*.

Table 42. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)	-	24(2)	MHz
	PLL input clock duty cycle	40(2)	-	60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)	-	72	MHz
t_{LOCK}	PLL lock time	-	-	200(2)	µs
Jitter	Cycle-to-cycle jitter	-	-	300(2)	ps

1. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design, not tested in production.

Table 73. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Pulse width of spikes that are suppressed by the analog filter	50	260	ns

1. Guaranteed by design, not tested in production.

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 74* for SPI or in *Table 75* for I²S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 19*.

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 74. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode 2.7 V<V_{DD}<3.6 V, SPI1/4	-	-	24	MHz
		Master mode 2 V<V_{DD}<3.6 V, SPI1/2/3/4			18	
		Slave mode 2 V<V_{DD}<3.6 V, SPI1/4			24	
		Slave mode 2 V<V_{DD}<3.6 V, SPI1/2/3/4			18	
		Slave mode transmitter/full duplex 2 V<V_{DD}<3.6 V, SPI1/2/3/4			16.5(2)	
		Slave mode transmitter/full duplex 2.7 V<V_{DD}<3.6 V, SPI1/4			22.5(2))	-
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	3	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	6.5	-	-	
$t_{h(SI)}$		Slave mode	4.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	10	-	30	
$t_{dis(SO)}$	Data output disable time	Slave mode	8	-	7	

Table 78. USB: full-speed electrical characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	-	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	-	2.0	V
Output driver Impedance(3)	Z_{DRV}	driving high and low	28	40	44	Ω

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed information, refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-), the matching impedance is already included in the embedded driver.

CAN (controller area network) interface

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

6.3.19 ADC characteristics

Unless otherwise specified, the parameters given in *Table 79* to *Table 82* are guaranteed by design, with conditions summarized in *Table 19*.

Table 79. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC	-	2.0	-	3.6	V
I_{DDA}	Current on VDDA pin (see *Figure 48*)	Single-ended mode, 5 MSPS	-	907	1033	µA
		Single-ended mode, 1 MSPS	-	194	285.5	
		Single-ended mode, 200 KSPS	-	51.5	70	
		Differential mode, 5 MSPS	-	887.5	1009	
		Differential mode, 1 MSPS	-	212	285	
		Differential mode, 200 KSPS	-	51	69.5	

Table 81. ADC accuracy - limited test conditions, 100-/144-pin packages (1)(2)

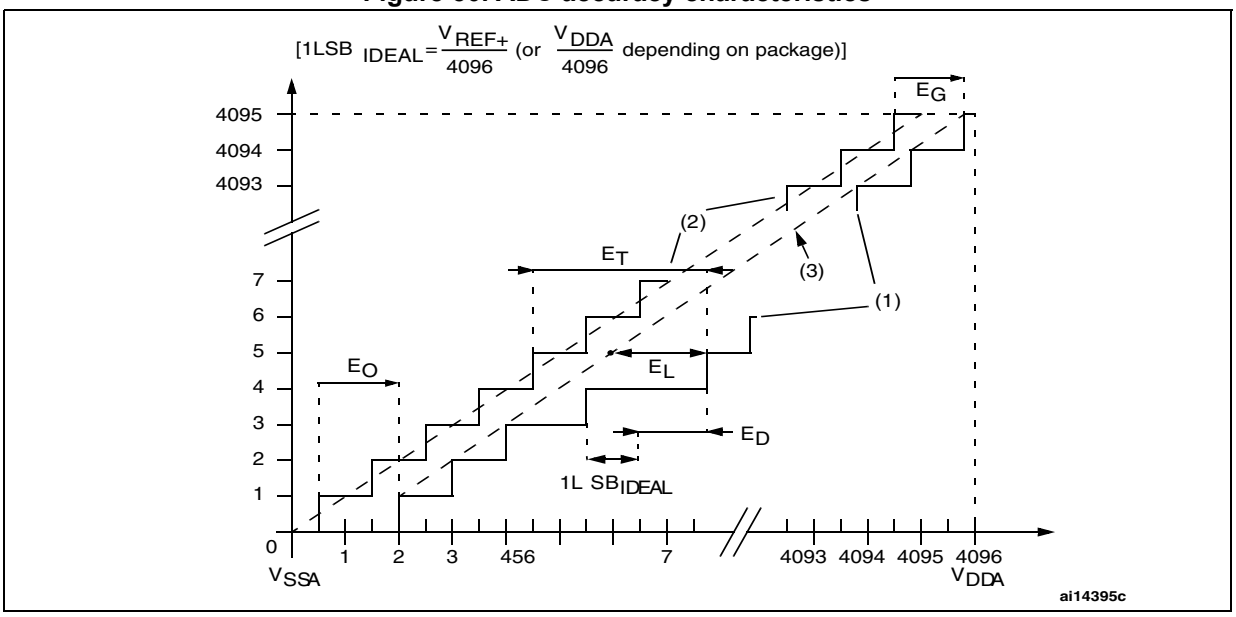
Symbol	Parameter	Conditions			Min (3)	Typ	Max (3)	Unit
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz Sampling freq. ≤ 5 Msps $V_{DDA} = V_{REF+} = 3.3$ V 25°C 100-pin/144-pin package	Single ended	Fast channel 5.1 Ms	-	±3.5	±4.5	LSB
				Slow channel 4.8 Ms	-	±4	±4.5	
			Differential	Fast channel 5.1 Ms	-	±3	±3	
				Slow channel 4.8 Ms	-	±3	±3	
EO	Offset error		Single ended	Fast channel 5.1 Ms	-	±1	±1.5	
				Slow channel 4.8 Ms	-	±1	±2.5	
			Differential	Fast channel 5.1 Ms	-	±1	±1.5	
				Slow channel 4.8 Ms	-	±1	±1.5	
EG	Gain error		Single ended	Fast channel 5.1 Ms	-	±3	±4	
				Slow channel 4.8 Ms	-	±3.5	±4	
			Differential	Fast channel 5.1 Ms	-	±1.5	±2.5	
				Slow channel 4.8 Ms	-	±2	±2.5	
ED	Differential linearity error		Single ended	Fast channel 5.1 Ms	-	±1	±1.5	
				Slow channel 4.8 Ms	-	±1	±1.5	
			Differential	Fast channel 5.1 Ms	-	±1	±1	
				Slow channel 4.8 Ms	-	±1	±1	
EL	Integral linearity error		Single ended	Fast channel 5.1 Ms	-	±1.5	±2	
				Slow channel 4.8 Ms	-	±1.5	±3	
			Differential	Fast channel 5.1 Ms	-	±1	±1.5	
				Slow channel 4.8 Ms	-	±1	±1.5	
ENOB(4)	Effective number of bits		Single ended	Fast channel 5.1 Ms	10.7	10.8	-	bits
				Slow channel 4.8 Ms	10.7	10.8	-	
			Differential	Fast channel 5.1 Ms	11.2	11.3	-	
				Slow channel 4.8 Ms	11.1	11.3	-	
SINAD(4)	Signal-to-noise and distortion ratio		Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	

Table 85. ADC accuracy at 1MSPS(1)(2)

Symbol	Parameter	Test conditions		Typ	Max(3)	Unit
ET	Total unadjusted error	ADC Freq ≤ 72 MHz Sampling Freq ≤ 1MSPS 2.4 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V Single-ended mode	Fast channel	±2.5	±5	LSB
			Slow channel	±3.5	±5	
EO	Offset error		Fast channel	±1	±2.5	
			Slow channel	±1.5	±2.5	
EG	Gain error		Fast channel	±2	±3	
			Slow channel	±3	±4	
ED	Differential linearity error		Fast channel	±0.7	±2	
			Slow channel	±0.7	±2	
EL	Integral linearity error		Fast channel	±1	±3	
			Slow channel	±1.2	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for IINJ(PIN) and ∑IINJ(PIN) in *Section 6.3.15: I/O port characteristics* does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.

Figure 50. ADC accuracy characteristics



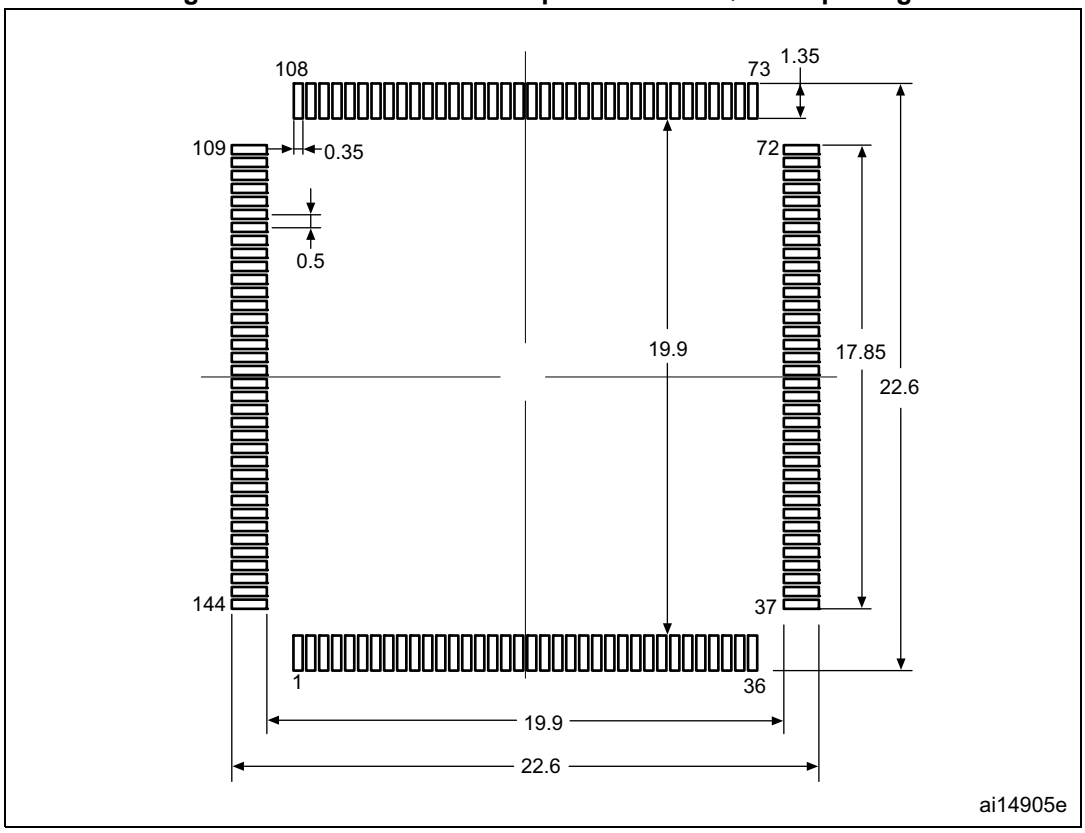
6.3.24 V_{BAT} monitoring characteristics

Table 91. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	2	-	-
Er(1)	Error on Q	-1	-	+1	%
T_{S_vbat}(1)(2)	ADC sampling time when reading the V_{BAT} 1mV accuracy	2.2	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

Figure 55. Recommended footprint for the LQFP144 package



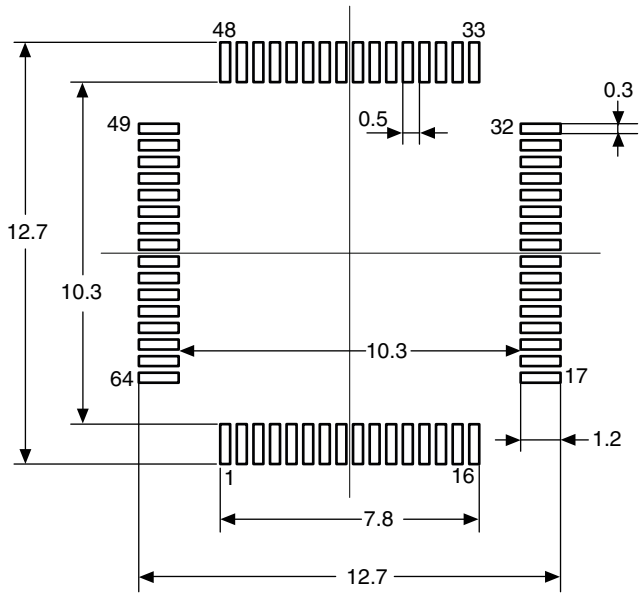
1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Table 98. LQFP64 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 67. Recommended footprint for the LQFP64 package



1. Dimensions are expressed in millimeters.