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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	86
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 39x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f303vet7

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F303xD/E microcontrollers.

This STM32F303xD/E datasheet should be read in conjunction with the reference manual of STM32F303xB/C/D/E, STM32F358xC and STM32F328x4/6/8 devices (RM0316) available on STMicroelectronics website at *www.st.com*.

For information on the ARM® Cortex®-M4 core with FPU, refer to the following documents:

- *Cortex® -M4 with FPU Technical Reference Manual*, available from the www.arm.com website
- *STM32F3 and STM32F4 Series Cortex® -M4 programming manual* (PM0214) available on STMicroelectronics website at *www.st.com*.

Table 4. STM32F303xD/E peripheral interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action
GPIO RTCCLK HSE/32 MC0	TIM16	Clock source used as input channel for HSI and LSI calibration
CSS CPU (hard fault) COMPx GPIO	TIM1, TIM8, TIM20 TIM15, 16, 17	Timer break
GPIO	TIMx	External trigger, timer break
	ADCx DAC1	Conversion external trigger
DAC1	COMPx	Comparator inverting input

Note: For more details about the interconnect actions, refer to the corresponding sections in the STM32F303xD/Ereference manual (RM0316).

3.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

Table 10. Capacitive sensing GPIOs available on STM32F303xD/E devices (continued)

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
3	TSC_G3_IO1	PC5	7	TSC_G7_IO1	PE2
	TSC_G3_IO2	PB0		TSC_G7_IO2	PE3
	TSC_G3_IO3	PB1		TSC_G7_IO3	PE4
	TSC_G3_IO4	PB2		TSC_G7_IO4	PE5
4	TSC_G4_IO1	PA9	8	TSC_G8_IO1	PD12
	TSC_G4_IO2	PA10		TSC_G8_IO2	PD13
	TSC_G4_IO3	PA13		TSC_G8_IO3	PD14
	TSC_G4_IO4	PA14		TSC_G8_IO4	PD15

Table 11. Number of capacitive sensing channels available on STM32F303xD/E devices

Analog I/O group	Number of capacitive sensing channels	
	STM32F303VE/ZE	STM32F303RE
G1	3	3
G2	3	3
G3	3	3
G4	3	3
G5	3	3
G6	3	3
G7	3	0
G8	3	0
Number of capacitive sensing channels	24	18

3.28 Development support

3.28.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.28.2 Embedded Trace Macrocell

The ARM embedded trace macrocell (ETM™) provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F303xD/E through a small number of ETM™ pins to an external hardware trace

Table 13. STM32F303xD/E pin definitions (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	UFBGA100	WLCSP100	LQFP144						
-	56	K8	G4	78	PD9	I/O	TTa	(1)	EVENTOUT, USART3_RX, FMC_D14	ADC4_IN13
-	57	J12	H3	79	PD10	I/O	TTa	(1)	EVENTOUT, USART3_CK, FMC_D15	ADC34_IN7, COMP6_INM
-	58	J11	H2	80	PD11	I/O	TTa	(1)	EVENTOUT, USART3_CTS, FMC_A16	ADC34_IN8, OPAMP4_VINP
-	59	J10	H1	81	PD12	I/O	TTa	(1)	EVENTOUT, TIM4_CH1, TSC_G8_IO1, USART3_RTS, FMC_A17	ADC34_IN9
-	60	H12	G3	82	PD13	I/O	TTa	(1)	EVENTOUT, TIM4_CH2, TSC_G8_IO2, FMC_A18	ADC34_IN10, COMP5_INM
-	-	-	-	83	VSS	S	-	(1)	-	-
-	-	-	-	84	VDD	S	-	(1)	-	-
-	61	H11	G2	85	PD14	I/O	TTa	(1)	EVENTOUT, TIM4_CH3, TSC_G8_IO3, FMC_D0	ADC34_IN11, OPAMP2_VINP
-	62	H10	G1	86	PD15	I/O	TTa	(1)	EVENTOUT, TIM4_CH4, TSC_G8_IO4, SPI2_NSS, FMC_D1	COMP3_INM
-	-	-	-	87	PG2	I/O	FT	(1)	EVENTOUT, TIM20_CH3N, FMC_A12	-
-	-	-	-	88	PG3	I/O	FT	(1)	EVENTOUT, TIM20_BKIN, FMC_A13	-
-	-	-	-	89	PG4	I/O	FT	(1)	EVENTOUT, TIM20_BKIN2, FMC_A14	-
-	-	-	-	90	PG5	I/O	FT	(1)	EVENTOUT, TIM20_ETR, FMC_A15	-
-	-	-	-	91	PG6	I/O	FT	(1)	EVENTOUT, FMC_INT2	-
-	-	-	-	92	PG7	I/O	FT	(1)	EVENTOUT, FMC_INT3	-
-	-	-	-	93	PG8	I/O	FT	(1)	EVENTOUT	-
-	-	-	-	94	VSS	S	-	(1)	-	-
-	-	-	-	95	VDD	S	-	(1)	-	-

Table 13. STM32F303xD/E pin definitions (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	UFBGA100	WLCSP100	LQFP144						
53	80	B10	A3	113	PC12	I/O	FT	-	EVENTOUT, TIM8_CH3N, UART5_TX, SPI3_MOSI/I2S3_SD, USART3_CK	-
-	81	C9	B3	114	PD0	I/O	FT	(1)	EVENTOUT, CAN_RX, FMC_D2	-
-	82	B9	C3	115	PD1	I/O	FT	(1)	EVENTOUT, TIM8_CH4, TIM8_BKIN2, CAN_TX, FMC_D3	-
54	83	C8	A4	116	PD2	I/O	FT	-	EVENTOUT, TIM3_ETR, TIM8_BKIN, UART5_RX	-
-	84	B8	B4	117	PD3	I/O	FT	(1)	EVENTOUT, TIM2_CH1/TIM2_ETR, USART2_CTS, FMC_CLK	-
-	85	B7	C4	118	PD4	I/O	FT	(1)	EVENTOUT, TIM2_CH2, USART2_RTS, FMC_NOE	-
-	86	A6	-	119	PD5	I/O	FT	(1)	EVENTOUT, USART2_TX, FMC_NWE	-
-	-	-	-	120	VSS	S	-	(1)	-	-
-	-	-	-	121	VDD	S	-	(1)	-	-
-	87	B6	-	122	PD6	I/O	FT	(1)	EVENTOUT, TIM2_CH4, USART2_RX, FMC_NWAIT	-
-	88	A5	D4	123	PD7	I/O	FT	(1)	EVENTOUT, TIM2_CH3, USART2_CK, FMC_NE1/FMC_NCE2	-
-	-	-	-	124	PG9	I/O	FT	(1)	EVENTOUT, FMC_NE2/FMC_NCE3	-
-	-	-	-	125	PG10	I/O	FT	(1)	EVENTOUT, FMC_NCE4_1/FMC_NE3	-
-	-	-	-	126	PG11	I/O	FT	(1)	EVENTOUT, FMC_NCE4_2	-
-	-	-	-	127	PG12	I/O	FT	(1)	EVENTOUT, FMC_NE4	-
-	-	-	-	128	PG13	I/O	FT	(1)	EVENTOUT, FMC_A24	-

Table 14. STM32F303xD/E alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3/TIM8/20/15/GPCOMP7/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/TIM8/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP3/5/6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port A	PA0	-	TIM2_CH1/TIM2_ETR	-	TSC_G1_IO1	-	-	-	USART2_CTS	COMP1_OUT	TIM8_BKIN	TIM8_ETR	-	-	-	-	EVENT OUT
	PA1	RTC_REFIN	TIM2_CH2	-	TSC_G1_IO2	-	-	-	USART2_RTS	-	TIM15_CH1N	-	-	-	-	-	EVENT OUT
	PA2	-	TIM2_CH3	-	TSC_G1_IO3	-	-	-	USART2_TX	COMP2_OUT	TIM15_CH1	-	-	-	-	-	EVENT OUT
	PA3	-	TIM2_CH4	-	TSC_G1_IO4	-	-	-	USART2_RX	-	TIM15_CH2	-	-	-	-	-	EVENT OUT
	PA4	-		TIM3_CH2	TSC_G2_IO1	-	SPI1_NSS	SPI3_NSS/I2S3_WS	USART2_CK	-	-	-	-	-	-	-	EVENT OUT
	PA5	-	TIM2_CH1/TIM2_ETR	-	TSC_G2_IO2	-	SPI1_SCK	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA6	-	TIM16_CH1	TIM3_CH1	TSC_G2_IO3	TIM8_BKIN	SPI1_MISO	TIM1_BKIN	-	COMP1_OUT	-	-	-	-	-	-	EVENT OUT
	PA7	-	TIM17_CH1	TIM3_CH2	TSC_G2_IO4	TIM8_CH1N	SPI1_MOSI	TIM1_CH1N	-	-	-	-	-	-	-	-	EVENT OUT
	PA8	MCO	-	-	I2C3_SCL	I2C2_SMBAL	I2S2_MCK	TIM1_CH1	USART1_CK	COMP3_OUT	-	TIM4_ETR	-	-	-	-	EVENT OUT
	PA9	-	-	I2C3_SMBAL	TSC_G4_IO1	I2C2_SCL	I2S3_MCK	TIM1_CH2	USART1_TX	COMP5_OUT	TIM15_BKIN	TIM2_CH3	-	-	-	-	EVENT OUT

5 Memory mapping

Figure 9. STM32F303xD/E memory map

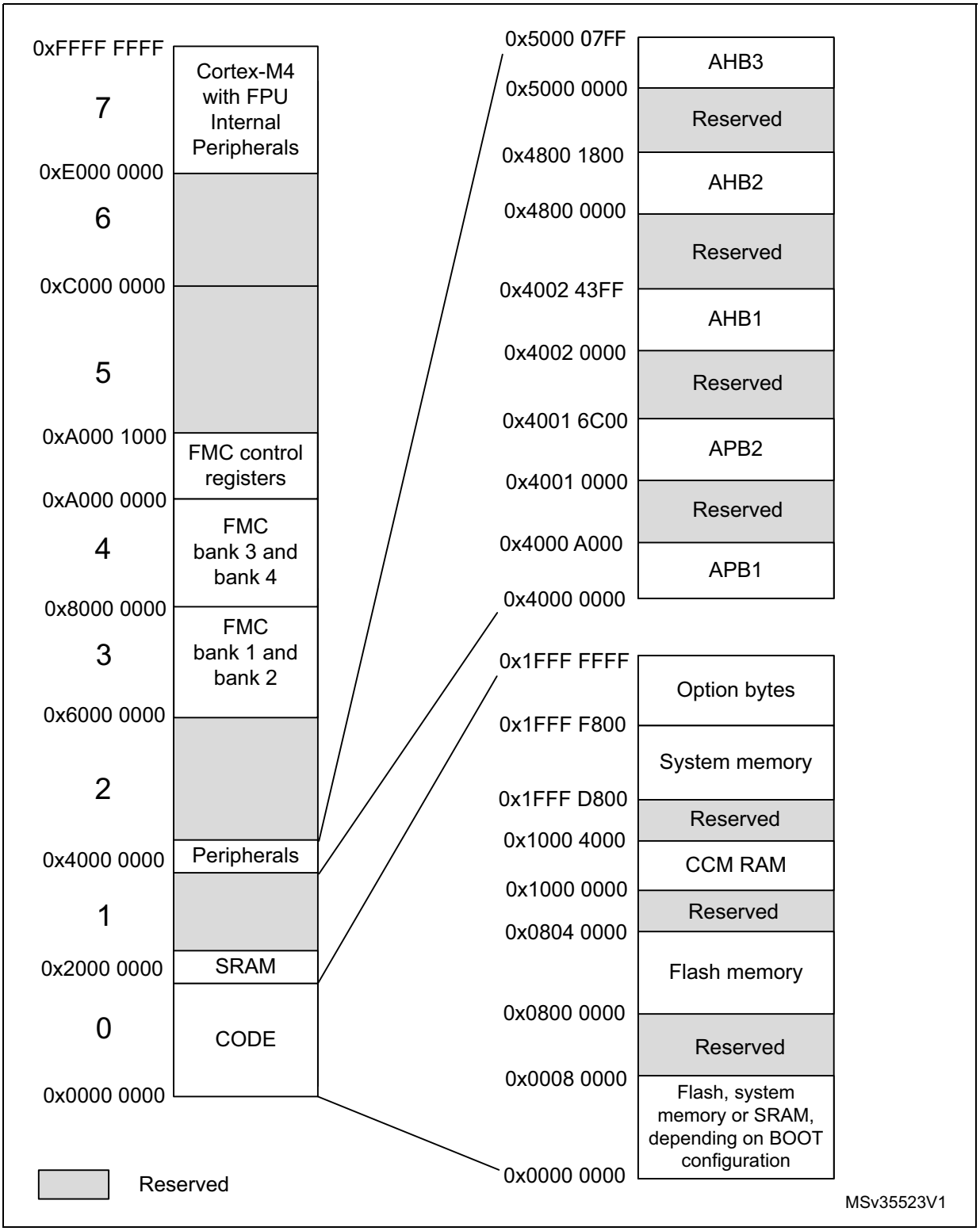


Table 15. Memory map, peripheral register boundary addresses (continued)

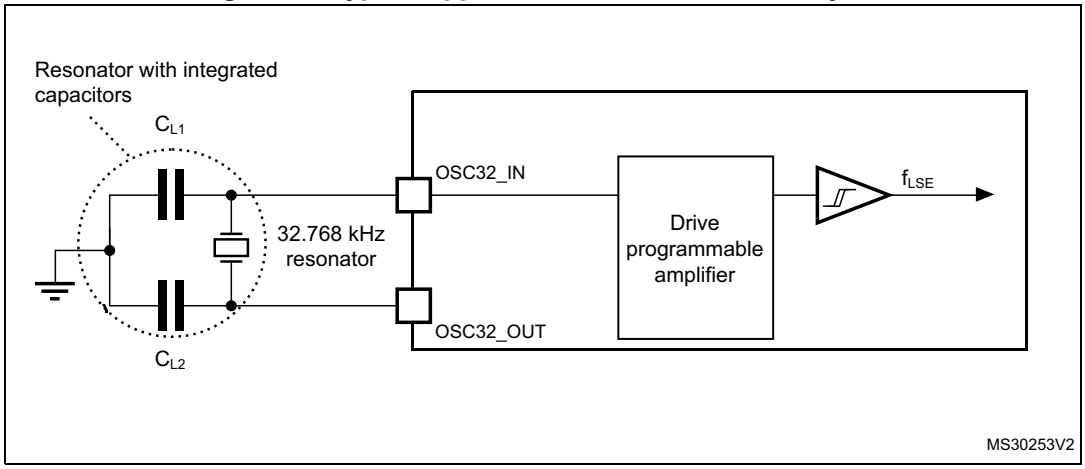
Bus	Boundary address	Size (bytes)	Peripheral
-	0x4001 8000 - 0x4001 FFFF	32 K	Reserved
	0x4001 5400 - 0x4001 7FFF	11 K	Reserved
	0x4001 5000 - 0x4001 53FF	1 K	TIM20
	0x4001 4C00 - 0x4001 4FFF	1 K	Reserved
	0x4001 4800 - 0x4001 4BFF	1 K	TIM17
	0x4001 4400 - 0x4001 47FF	1 K	TIM16
	0x4001 4000 - 0x4001 43FF	1 K	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 K	SPI4
	0x4001 3800 - 0x4001 3BFF	1 K	USART1
	0x4001 3400 - 0x4001 37FF	1 K	TIM8
	0x4001 3000 - 0x4001 33FF	1 K	SPI1
APB2	0x4001 2C00 - 0x4001 2FFF	1 K	TIM1
	0x4001 0800 - 0x4001 2BFF	9 K	Reserved
	0x4001 0400 - 0x4001 07FF	1 K	EXTI
	0x4001 0000 - 0x4001 03FF	1 K	SYSCFG + COMP + OPAMP
-	0x4000 7C00 - 0x4000 FFFF	32 K	Reserved

Table 33. Peripheral current consumption

Peripheral	Typical consumption(1)	Unit
	I_{DD}	
BusMatrix (2)	8.3	µA/MHz
DMA1	7.0	
DMA2	5.4	
FSMC	35.0	
CRC	1.5	
GPIOH	1.3	
GPIOA	5.4	
GPIOB	5.3	
GPIOC	5.4	
GPIOD	5.0	
GPIOE	5.4	
GPIOF	5.2	
GPIOG	5.0	
TSC	5.2	
ADC1&2	15.4	
ADC3&4	16.2	
APB2-Bridge (3)	3.1	
SYSCFG	4.0	
TIM1	26.0	
SPI1	6.2	
TIM8	26.4	
USART1	17.7	
SPI4	6.2	
TIM15	11.9	
TIM16	8.0	
TIM17	8.5	
TIM20	25.3	

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 18. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in *Table 40* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 19*.

High-speed internal (HSI) RC oscillator

Table 40. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1(2)	%
$DuCy_{(HSI)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -40 to 105°C	-2.8(3)	-	3.8(3)	%
		T_A = -10 to 85°C	-1.9(3)	-	2.3(3)	
		T_A = 0 to 85°C	-1.9(3)	-	2(3)	
		T_A = 0 to 70°C	-1.3(3)	-	2(3)	
		T_A = 0 to 55°C	-1(3)	-	2(3)	
		T_A = 25°C(4)	-1	-	1	
$t_{SU(HSI)}$	HSI oscillator startup time	-	1(2)	-	2(2)	µs
$I_{DDA(HSI)}$	HSI oscillator power consumption	-	-	80	100(2)	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.
4. Factory calibrated, parts not soldered.

Table 56. Synchronous non-multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	2THCLK-1	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	6	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	THCLK+1.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	7.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	6.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	0	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	0	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	THCLK+2	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	7.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	7	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	THCLK+0.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. Based on characterization, not tested in production.

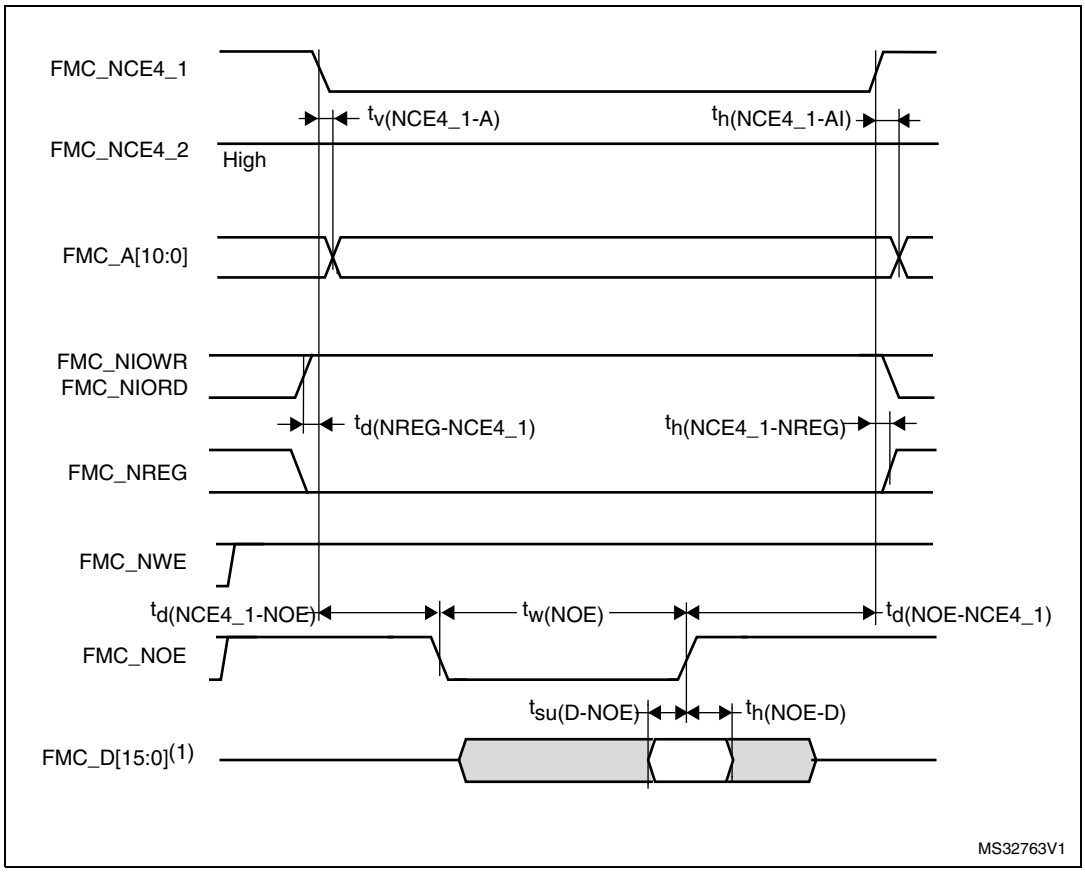
PC Card/CompactFlash controller waveforms and timings

Figure 28 to *Figure 33* present the PC Card/Compact Flash controller waveforms, and *Table 57* to *Table 58* provide the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FMC_SetupTime = 0x04;
- COM.FMC_WaitSetupTime = 0x07;
- COM.FMC_HoldSetupTime = 0x04;
- COM.FMC_HiZSetupTime = 0x05;
- ATT.FMC_SetupTime = 0x04;
- ATT.FMC_WaitSetupTime = 0x07;
- ATT.FMC_HoldSetupTime = 0x04;
- ATT.FMC_HiZSetupTime = 0x05;
- IO.FMC_SetupTime = 0x04;
- IO.FMC_WaitSetupTime = 0x07;
- IO.FMC_HoldSetupTime = 0x04;
- IO.FMC_HiZSetupTime = 0x05;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the THCLK is the HCLK clock period.

Figure 30. PC Card/CompactFlash controller waveforms for attribute memory read access



1. Only data bits 0...7 are read (bits 8...15 are disregarded).

6.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling two LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 61*. They are based on the EMS levels and classes defined in application note AN1709.

Table 61. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

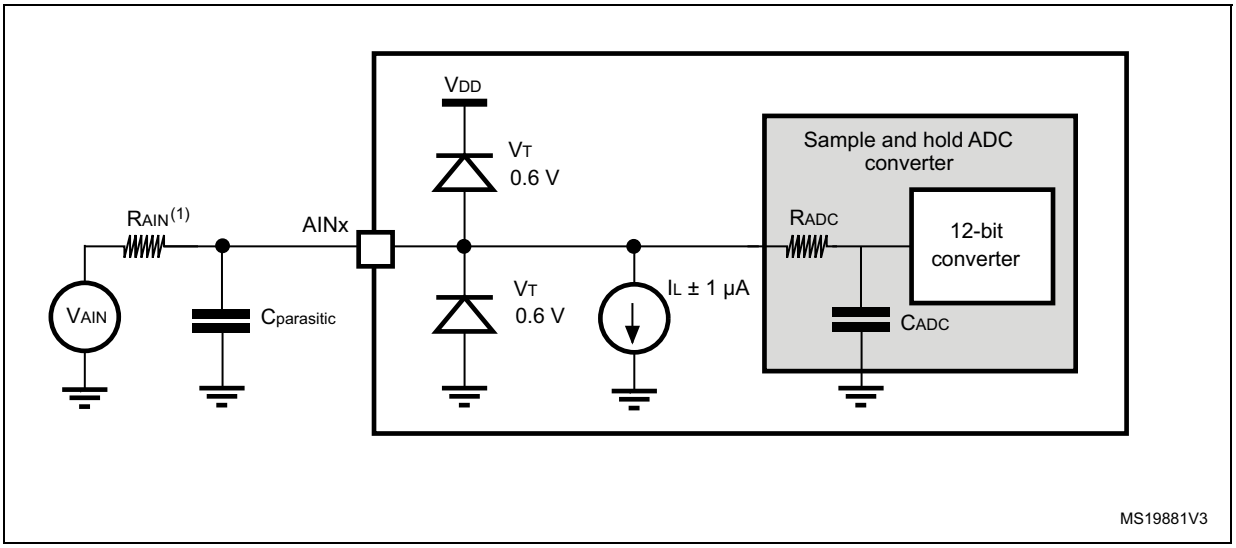
- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Table 82. ADC accuracy, 100-pin/144-pin packages(1)(2)(3) (continued)

Symbol	Parameter	Conditions			Min (4)	Max(4)	Unit
EL	Integral linearity error	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps, 2.0 V≤ V_{DDA}, V_{REF+} ≤ 3.6 V 100-pin/144-pin package	Single Ended	Fast channel 5.1 Ms	-	±2	LSB
				Slow channel 4.8 Ms	-	±3	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2	
ENOB (5)	Effective number of bits		Single Ended	Fast channel 5.1 Ms	10.4	-	bits
				Slow channel 4.8 Ms	10.2	-	
			Differential	Fast channel 5.1 Ms	10.8	-	
				Slow channel 4.8 Ms	10.8	-	
SINAD (5)	Signal-to-noise and distortion ratio		Single Ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	63	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
SNR(5)	Signal-to-noise ratio		Single Ended	Fast channel 5.1 Ms	64	-	
				Slow channel 4.8 Ms	64	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
THD(5)	Total harmonic distortion		Single Ended	Fast channel 5.1 Ms	-	74	
				Slow channel 4.8 Ms	-	-74	
			Differential	Fast channel 5.1 Ms	-	-78	
				Slow channel 4.8 Ms	-	-76	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.15* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.
5. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Figure 51. Typical connection diagram using the ADC



1. Refer to *Table 79* for the values of R_{AIN}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 12*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.20 DAC electrical specifications

Table 86. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2.4	-	3.6	V
R_{LOAD}(1)	Resistive load	DAC output buffer ON	5	-	-	kΩ
R_L	Resistive load	Dac output buffer ON: connected to V_{SSA}	5	-	-	kΩ
		Dac output buffer ON: connected to V_{DDA}	25	-	-	kΩ
R_O(1)	Output impedance	DAC output buffer OFF	-	-	15	kΩ
C_{LOAD}(1)	Capacitive load	DAC output buffer ON	-	-	50	pF
V_{DAC_OUT} (1)	Voltage on DAC_OUT output	Corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{DDA} = 3.6 V and (0x155) and (0xEAB) at V_{DDA} = 2.4 V DAC output buffer ON.	0.2	-	V_{DDA} – 0.2	V
		DAC output buffer OFF	-	0.5	V_{DDA} - 1LSB	mV

Table 86. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{REF}	DAC DC current consumption in quiescent mode (Standby mode)	With no load, worst code (0xF1C) on the input	-	-	220	µA
I_{DDA}(3)	DAC DC current consumption in quiescent mode (Standby mode)(2)	With no load, middle code (0x800) on the input.	-	-	380	µA
		With no load, worst code (0xF1C) on the input.	-	-	480	µA
DNL(3)	Differential non linearity Difference between two consecutive code-1LSB)	Given for a 10-bit input code	-	-	±0.5	LSB
		Given for a 12-bit input code	-	-	±2	LSB
INL(3)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095)	Given for a 10-bit input code	-	-	±1	LSB
		Given for a 12-bit input code	-	-	±4	LSB
Offset(3)	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{DDA}/2$)	-	-	-	±10	mV
		Given for a 10-bit input code at V_{DDA} = 3.6 V	-	-	±3	LSB
		Given for a 12-bit input code at V_{DDA} = 3.6 V	-	-	±12	LSB
Gain error(3)	Gain error	Given for a 12-bit input code	-	-	±0.5	%
$t_{SETTLING}$(3)	Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	$C_{LOAD} \leq$50 pF, $R_{LOAD} \geq$ 5 kΩ	-	3	4	µs
t_{STAB}	Power-up time	-	1			conversion cycle
Update rate(3)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	$C_{LOAD} \leq$50 pF, $R_{LOAD} \geq$ 5 kΩ	-	-	1	MS/s
t_{WAKEUP}(3)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	$C_{LOAD} \leq$50 pF, $R_{LOAD} \geq$ 5 kΩ	-	6.5	10	µs
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	C_{LOAD} = 50 pF, No $R_{LOAD} \geq$ 5 kΩ,	-	–67	–40	dB
I_{skink}(1)	Output sink current	DAC buffer ON Output level higher than 0.2 V	100	-	-	µA

1. Guaranteed by design, not tested in production.

Table 87. Comparator characteristics(1) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
TV_{OFFSET}	Total offset variation	Full temperature range	-	-	3	mV
I_{DDA}	COMP current consumption	-	-	400	600	µA

1. Guaranteed by design, not tested in production.

6.3.22 Operational amplifier characteristics

Table 88. Operational amplifier characteristics(1)

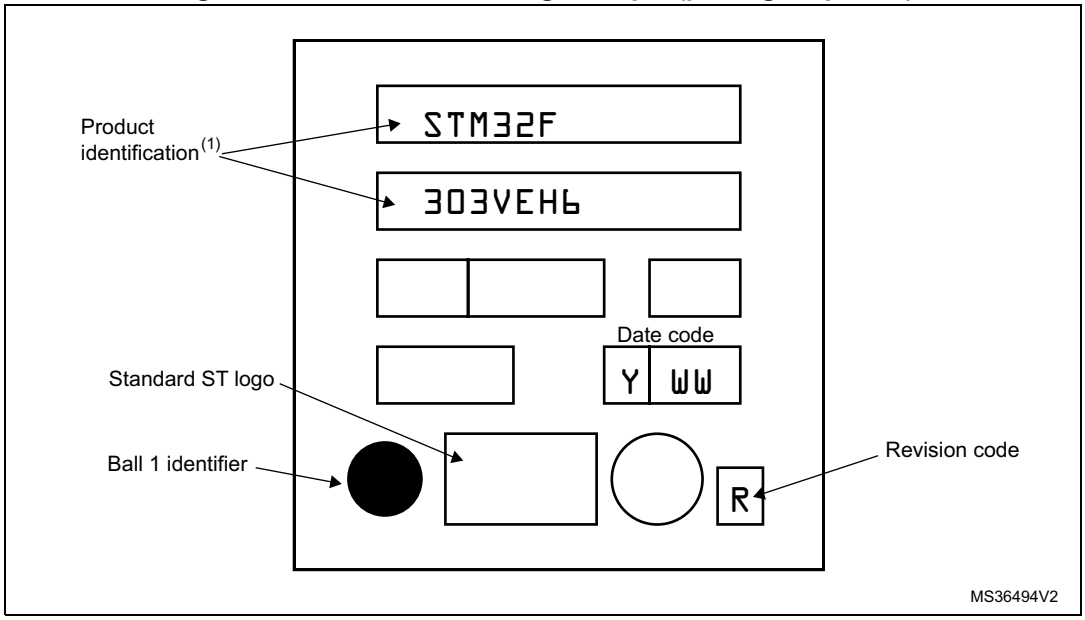
Symbol	Parameter		Condition	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage		-	2.4	-	3.6	V
CMIR	Common mode input range		-	0	-	V_{DDA}	V
VI_{OFFSET}	Input offset voltage	Maximum calibration range	25°C, No Load on output.	-	-	4	mV
			All voltage/Temp.	-	-	6	
		After offset calibration	25°C, No Load on output.	-	-	1.6	
			All voltage/Temp.	-	-	3	
ΔVI_{OFFSET}	Input offset voltage drift		-	-	5	-	µV/°C
I_{LOAD}	Drive current		-	-	-	500	µA
I_{DDA}	OPAMP consumption		No load, quiescent mode	-	690	1450	µA
TS_OPAMP_VOUT	ADC sampling time when reading the OPAMP output.		-	400	-	-	ns
CMRR	Common mode rejection ratio		-	-	90	-	dB
PSRR	Power supply rejection ratio		DC	73	117	-	dB
GBW	Bandwidth		-	-	8.2	-	MHz
SR	Slew rate		-	-	4.7	-	V/µs
R_{LOAD}	Resistive load		-	4	-	-	kΩ
C_{LOAD}	Capacitive load		-	-	-	50	pF
VOH_{SAT}	High saturation voltage(2)		R_{load} = min, Input at V_{DDA}.	$V_{DDA-100}$	-	-	mV
			R_{load} = 20K, Input at V_{DDA}.	V_{DDA-20}	-	-	
VOL_{SAT}	Low saturation voltage(2)		Rload = min, input at 0V	-	-	100	
			Rload = 20K, input at 0V.	-	-	20	
φm	Phase margin		-	-	62	-	°
$t_{OFFTRIM}$	Offset trim time: during calibration, minimum time needed between two steps to have 1 mV accuracy		-	-	-	2	ms
t_{WAKEUP}	Wake up time from OFF state.		C_{LOAD} ≤50 pf, R_{LOAD} ≥ 4 kΩ, Follower configuration	-	2.8	5	µs

Device marking for UFBGA100

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 59. UFBGA100 marking example (package top view)



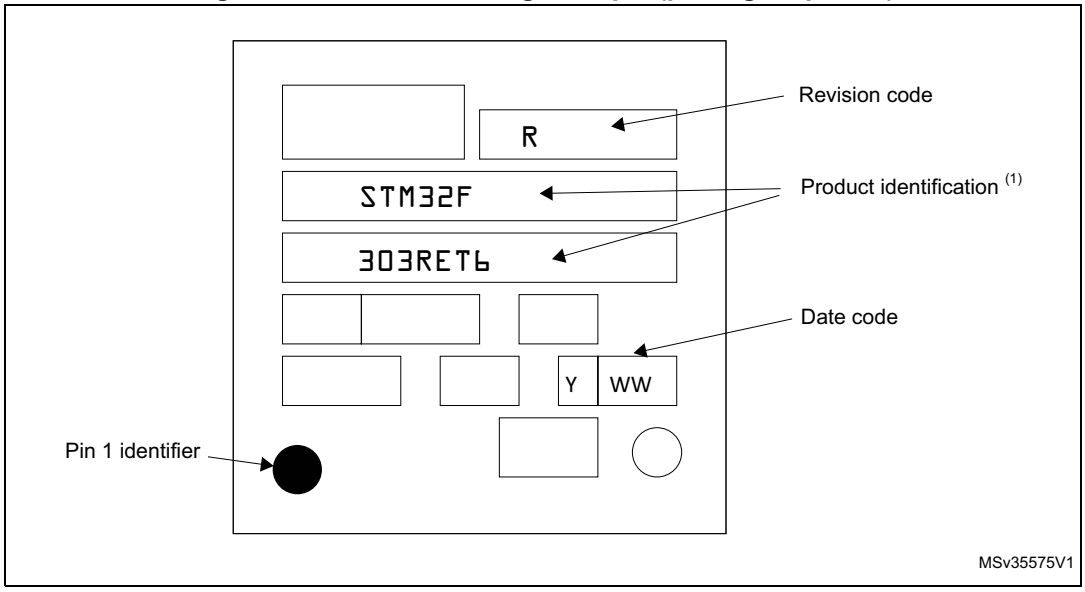
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Device marking for LQFP64

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 68. LQFP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.