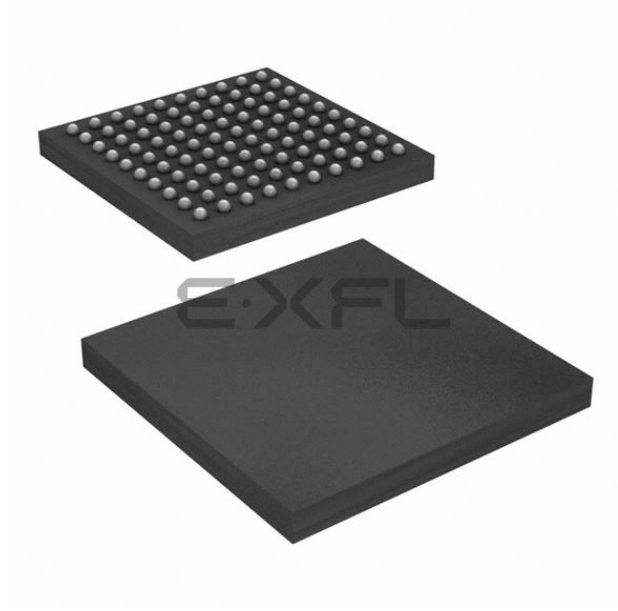

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## What is "Embedded - Microcontrollers"?

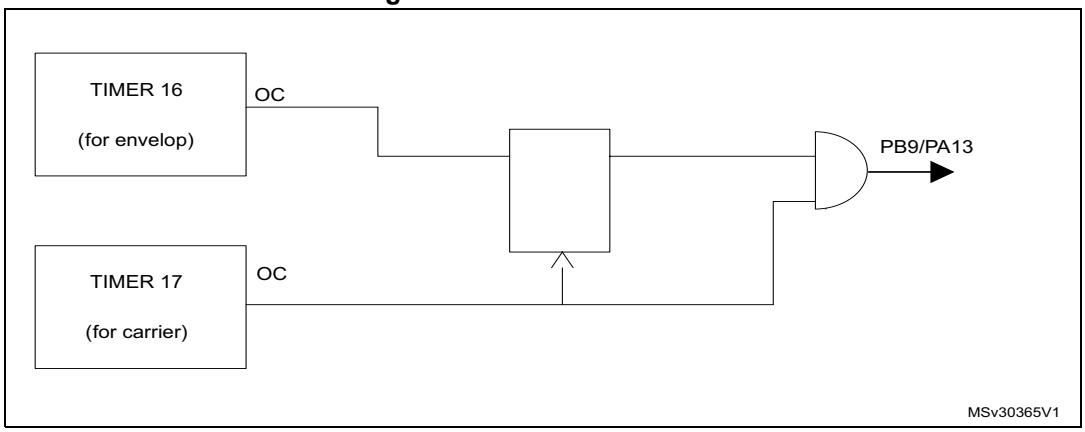
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | DMA, I²S, POR, PWM, WDT |
| Number of I/O | 77 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 80K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 39x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-UFBGA, WLCSP |
| Supplier Device Package | 100-WLCSP (4.2x4.7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f303vey6tr |

# List of figures

Figure 3. Infrared transmitter




## 3.27 Touch sensing controller (TSC)

The STM32F303xD/E devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 24 capacitive sensing channels distributed over 8 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic, etc.). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 10. Capacitive sensing GPIOs available on STM32F303xD/E devices

| Group | Capacitive sensing signal name | Pin name | Group | Capacitive sensing signal name | Pin name |
|---|---|---|---|---|---|
| 1 | TSC_G1_IO1 | PA0 | 5 | TSC_G5_IO1 | PB3 |
| | TSC_G1_IO2 | PA1 | | TSC_G5_IO2 | PB4 |
| | TSC_G1_IO3 | PA2 | | TSC_G5_IO3 | PB6 |
| | TSC_G1_IO4 | PA3 | | TSC_G5_IO4 | PB7 |
| 2 | TSC_G2_IO1 | PA4 | 6 | TSC_G6_IO1 | PB11 |
| | TSC_G2_IO2 | PA5 | | TSC_G6_IO2 | PB12 |
| | TSC_G2_IO3 | PA6 | | TSC_G6_IO3 | PB13 |
| | TSC_G2_IO4 | PA7 | | TSC_G6_IO4 | PB14 |

**Table 12. Legend/abbreviations used in the pinout table**

| Name | | Abbreviation | Definition |
|---|---|---|---|
| Pin name | | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name | |
| I/O structure | | FT | 5 V tolerant I/O |
| | | FTf | 5 V tolerant I/O, $I^2C$ FM+ option |
| | | TTa | 3.3 V tolerant I/O |
| | | TC | Standard 3.3V I/O |
| | | B | Dedicated to BOOT0 pin |
| | | RST | Bi-directional reset pin with embedded weak pull-up resistor |
| Notes | | Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset | |
| Pin functions | Alternate functions | Functions selected through GPIOx_AFR registers | |
| | Additional functions | Functions directly selected/enabled through peripheral registers | |

**Table 13. STM32F303xD/E pin definitions (continued)**

| Pin number | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | UFBGA100 | WLCSP100 | LQFP144 | | | | | | |
| - | - | - | - | 49 | PF11 | I/O | FT | (1) | EVENTOUT, TIM20_ETR | - |
| - | - | - | - | 50 | PF12 | I/O | FT | (1) | EVENTOUT, TIM20_CH1, FMC_A6 | - |
| - | - | - | - | 51 | VSS | S | - | - | - | - |
| - | - | - | - | 52 | VDD | S | - | (1) | - | - |
| - | - | - | - | 53 | PF13 | I/O | FT | (1) | EVENTOUT, TIM20_CH2, FMC_A7 | - |
| - | - | - | - | 54 | PF14 | I/O | FT | (1) | EVENTOUT, TIM20_CH3, FMC_A8 | - |
| - | - | - | - | 55 | PF15 | I/O | FT | (1) | EVENTOUT, TIM20_CH4, FMC_A9 | - |
| - | - | - | - | 56 | PG0 | I/O | FT | (1) | EVENTOUT, TIM20_CH1N, FMC_A10 | - |
| - | - | - | - | 57 | PG1 | I/O | FT | (1) | EVENTOUT, TIM20_CH2N, FMC_A11 | - |
| - | 38 | M7 | F8 | 58 | PE7 | I/O | TTa | (1) | EVENTOUT, TIM1_ETR, FMC_D4 | ADC3_IN13 |
| - | 39 | L7 | E6 | 59 | PE8 | I/O | TTa | (1) | EVENTOUT, TIM1_CH1N, FMC_D5 | ADC34_IN6, COMP4_INM |
| - | 40 | M8 | - | 60 | PE9 | I/O | TTa | (1) | EVENTOUT, TIM1_CH1, FMC_D6 | ADC3_IN2(3) |
| - | - | - | - | 61 | VSS | S | - | (1) | - | - |
| - | - | - | - | 62 | VDD | S | - | (1) | - | - |
| - | 41 | L8 | - | 63 | PE10 | I/O | TTa | (1) | EVENTOUT, TIM1_CH2N, FMC_D7 | ADC3_IN14 |
| - | 42 | M9 | H5 | 64 | PE11 | I/O | TTa | (1) | EVENTOUT, TIM1_CH2, SPI4_NSS, FMC_D8 | ADC3_IN15 |
| - | 43 | L9 | G5 | 65 | PE12 | I/O | TTa | (1) | EVENTOUT, TIM1_CH3N, SPI4_SCK, FMC_D9 | ADC3_IN16 |
| - | 44 | M10 | - | 66 | PE13 | I/O | TTa | (1) | EVENTOUT, TIM1_CH3, SPI4_MISO, FMC_D10 | ADC3_IN3(3) |

**Table 13. STM32F303xD/E pin definitions (continued)**

| Pin number | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | UFBGA100 | WLCSP100 | LQFP144 | | | | | | |
| - | 45 | M11 | - | 67 | PE14 | I/O | TTa | (1) | EVENTOUT, TIM1_CH4, SPI4_MOSI, TIM1_BKIN2, FMC_D11 | ADC4_IN1(3) |
| - | 46 | M12 | - | 68 | PE15 | I/O | TTa | (1) | EVENTOUT, TIM1_BKIN, USART3_RX, FMC_D12 | ADC4_IN2(3) |
| 29 | 47 | L10 | K4 | 69 | PB10 | I/O | TTa | - | TIM2_CH3, TSC_SYNC, USART3_TX, EVENTOUT | COMP5_INM, OPAMP3_VINM, OPAMP4_VINM |
| 30 | 48 | L11 | K3 | 70 | PB11 | I/O | TTa | - | TIM2_CH4, TSC_G6_IO1, USART3_RX, EVENTOUT | ADC12_IN14, COMP6_INP, OPAMP4_VINP |
| 31 | 49 | F12 | K1, J1, K2 | 71 | VSS | S | - | - | - | - |
| 32 | 50 | G12 | J5 | 72 | VDD | S | - | - | - | - |
| 33 | 51 | L12 | J4 | 73 | PB12 | I/O | TTa | (5) | TSC_G6_IO2, I2C2_SMBAL, SPI2_NSS/I2S2_WS, TIM1_BKIN, USART3_CK, EVENTOUT | ADC4_IN3(3), COMP3_INM, OPAMP4_VOUT |
| 34 | 52 | K12 | J3 | 74 | PB13 | I/O | TTa | - | TSC_G6_IO3, SPI2_SCK/I2S2_CK, TIM1_CH1N, USART3_CTS, EVENTOUT | ADC3_IN5(3), COMP5_INP, OPAMP3_VINP, OPAMP4_VINP |
| 35 | 53 | K11 | J2 | 75 | PB14 | I/O | TTa | - | TIM15_CH1, TSC_G6_IO4, SPI2_MISO/I2S2ext_SD, TIM1_CH2N, USART3_RTS, EVENTOUT | ADC4_IN4(3), COMP3_INP, OPAMP2_VINP |
| 36 | 54 | K10 | H4 | 76 | PB15 | I/O | TTa | - | RTC_REFIN, TIM15_CH2, TIM15_CH1N, TIM1_CH3N, SPI2_MOSI/I2S2_SD, EVENTOUT | ADC4_IN5(3), COMP6_INM |
| - | 55 | K9 | - | 77 | PD8 | I/O | TTa | (1) | EVENTOUT, USART3_TX, FMC_D13 | ADC4_IN12, OPAMP4_VINM |

**Table 13. STM32F303xD/E pin definitions (continued)**

| Pin number | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | UFBGA100 | WLCSP100 | LQFP144 | | | | | | |
| 61 | 95 | A3 | D5 | 139 | PB8 | I/O | FTf | - | TIM16_CH1, TIM4_CH3, TSC_SYNC, I2C1_SCL, USART3_RX, COMP1_OUT, CAN_RX, TIM8_CH2, TIM1_BKIN, EVENTOUT | - |
| 62 | 96 | B3 | C6 | 140 | PB9 | I/O | FTf | - | TIM17_CH1, TIM4_CH4, I2C1_SDA, IR-OUT, USART3_TX, COMP2_OUT, CAN_TX, TIM8_CH3, EVENTOUT | - |
| - | 97 | C3 | B7 | 141 | PE0 | I/O | FT | (1) | EVENTOUT, TIM4_ETR, TIM16_CH1, TIM20_ETR, USART1_TX, FMC_NBL0 | - |
| - | 98 | A2 | A8 | 142 | PE1 | I/O | FT | (1) | EVENTOUT, TIM17_CH1, TIM20_CH4, USART1_RX, FMC_NBL1 | - |
| 63 | 99 | E3 | C7 | 143 | VSS | S | - | - | - | - |
| 64 | 100 | C4 | A9, A10, B10, B8 | 144 | VDD | S | - | - | - | - |

1. Function availability depends on the chosen device.
2. PC13, PC14 and PC15 are supplied through the power switch. Since the switch sinks only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED)

   After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the RM0316 reference manual.
3. Fast ADC channel.
4. The VREF+ functionality is not available on the 64-pin package. In this package, the VREF+ is internally connected to VDDA.
5. These GPIOs offer a reduced touch sensing sensitivity. It is thus recommended to use them as sampling capacitor I/O.

**Table 15. Memory map, peripheral register boundary addresses (continued)**

| Bus | Boundary address | Size (bytes) | Peripheral |
|---|---|---|---|
| - | 0x4001 8000 - 0x4001 FFFF | 32 K | Reserved |
| | 0x4001 5400 - 0x4001 7FFF | 11 K | Reserved |
| | 0x4001 5000 - 0x4001 53FF | 1 K | TIM20 |
| | 0x4001 4C00 - 0x4001 4FFF | 1 K | Reserved |
| | 0x4001 4800 - 0x4001 4BFF | 1 K | TIM17 |
| | 0x4001 4400 - 0x4001 47FF | 1 K | TIM16 |
| | 0x4001 4000 - 0x4001 43FF | 1 K | TIM15 |
| | 0x4001 3C00 - 0x4001 3FFF | 1 K | SPI4 |
| | 0x4001 3800 - 0x4001 3BFF | 1 K | USART1 |
| | 0x4001 3400 - 0x4001 37FF | 1 K | TIM8 |
| | 0x4001 3000 - 0x4001 33FF | 1 K | SPI1 |
| APB2 | 0x4001 2C00 - 0x4001 2FFF | 1 K | TIM1 |
| | 0x4001 0800 - 0x4001 2BFF | 9 K | Reserved |
| | 0x4001 0400 - 0x4001 07FF | 1 K | EXTI |
| | 0x4001 0000 - 0x4001 03FF | 1 K | SYSCFG + COMP + OPAMP |
| - | 0x4000 7C00 - 0x4000 FFFF | 32 K | Reserved |

**Table 28. Typical and maximum $V_{DDA}$ consumption in Stop and Standby modes**

| Symbol | Parameter | Conditions | | Typ @$V_{DD}$ ($V_{DD}$ = $V_{DDA}$) | | | | | | Max(1) | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 2.0 V | 2.4 V | 2.7 V | 3.0 V | 3.3 V | 3.6 V | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DDA}$ | Supply current in Stop mode | $V_{DDA}$ supervisor ON | Regulator in run/low-power mode, all oscillators OFF | 1.72 | 1.85 | 1.97 | 2.10 | 2.25 | 2.41 | 10.7 | 11 | 12 | µA |
| | Supply current in Standby mode | | LSI ON and IWDG ON | 2.08 | 2.26 | 2.43 | 2.61 | 2.82 | 3.05 | - | - | - | |
| | | | LSI OFF and IWDG OFF | 1.60 | 1.73 | 1.85 | 1.98 | 2.13 | 2.29 | 3.6 | 4 | 6 | |
| | Supply current in Stop mode | $V_{DDA}$ supervisor OFF | Regulator in run/low-power mode, all oscillators OFF | 1.00 | 1.02 | 1.05 | 1.10 | 1.16 | 1.24 | - | - | - | |
| | Supply current in Standby mode | | LSI ON and IWDG ON | 1.36 | 1.43 | 1.51 | 1.61 | 1.74 | 1.88 | - | - | - | |
| | | | LSI OFF and IWDG OFF | 0.88 | 0.90 | 0.93 | 0.98 | 1.05 | 1.12 | - | - | - | |

1. Data based on characterization results, not tested in production.

**Table 29. Typical and maximum current consumption from $V_{BAT}$ supply**

| Symbol | Para meter | Conditions (1) | Typ @$V_{BAT}$ | | | | | | | | Max @$V_{BAT}$ = 3.6 V(2) | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.65V | 1.8V | 2V | 2.4V | 2.7V | 3V | 3.3V | 3.6V | $T_A$ = 25°C | $T_A$ = 85°C | $T_A$ = 105°C | |
| $I_{DD\_VBAT}$ | Backup domain supply current | LSE & RTC ON; “Xtal mode” lower driving capability; LSEDRV[1:0] = '00' | 0.48 | 0.50 | 0.52 | 0.58 | 0.65 | 0.72 | 0.80 | 0.90 | 1.1 | 1.5 | 2.0 | µA |
| | | LSE & RTC ON; “Xtal mode” higher driving capability; LSEDRV[1:0] = '11' | 0.83 | 0.86 | 0.90 | 0.98 | 1.03 | 1.10 | 1.20 | 1.30 | 1.5 | 2.2 | 2.9 | |

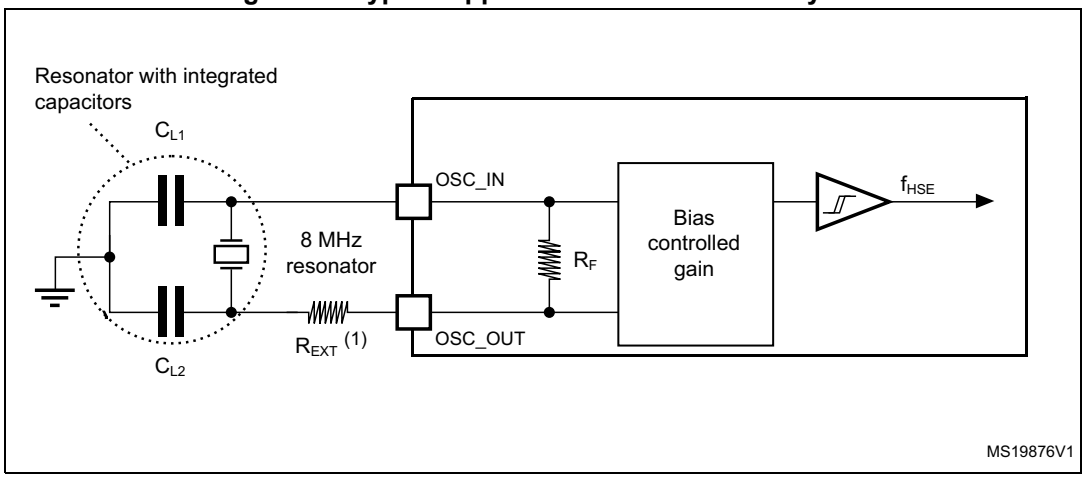
1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values.
2. Data based on characterization results, not tested in production.

**Table 33. Peripheral current consumption (continued)**

| Peripheral | Typical consumption(1) | Unit |
|---|---|---|
| | $I_{DD}$ | |
| APB1-Bridge (3) | 6.7 | µA/MHz |
| TIM2 | 39.2 | |
| TIM3 | 30.8 | |
| TIM4 | 31.3 | |
| TIM6 | 4.3 | |
| TIM7 | 4.3 | |
| WWDG | 1.3 | |
| SPI2 | 33.6 | |
| SPI3 | 33.9 | |
| USART2 | 39.3 | |
| USART3 | 39.3 | |
| UART4 | 29.8 | |
| UART5 | 27.0 | |
| I2C1 | 6.7 | |
| I2C2 | 6.4 | |
| USB | 14.7 | |
| CAN | 25.6 | |
| PWR | 3.7 | |
| DAC | 22.1 | |
| I2C3 | 6.8 | |

1. The power consumption of the analog part ($I_{DDA}$) of peripherals such as ADC, DAC, Comparators, OpAmp is not included. Refer to the tables of characteristics in the subsequent sections.
2. BusMatrix is automatically active when at least one master is ON (CPU, DMA1 or DMA2).
3. The APBx bridge is automatically active when at least one peripheral is ON on the same bus.

**Figure 17. Typical application with an 8 MHz crystal**




1. $R_{EXT}$ value depends on the crystal characteristics.

### Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 39*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 39. LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz)**

| Symbol | Parameter | Conditions(1) | Min(2) | Typ | Max(2) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | LSE current consumption | LSEDRV[1:0]=00 lower driving capability | - | 0.5 | 0.9 | µA |
| | | LSEDRV[1:0]=01 medium low driving capability | - | - | 1 | |
| | | LSEDRV[1:0]=10 medium high driving capability | - | - | 1.3 | |
| | | LSEDRV[1:0]=11 higher driving capability | - | - | 1.6 | |
| $g_m$ | Oscillator transconductance | LSEDRV[1:0]=00 lower driving capability | 5 | - | - | µA/V |
| | | LSEDRV[1:0]=01 medium low driving capability | 8 | - | - | |
| | | LSEDRV[1:0]=10 medium high driving capability | 15 | - | - | |
| | | LSEDRV[1:0]=11 higher driving capability | 25 | - | - | |
| $t_{SU(LSE)}$(3) | Startup time | $V_{DD}$ is stabilized | - | 2 | - | s |

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

**Table 53. Synchronous multiplexed NOR/PSRAM read timings(1) (continued)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{d(CLKL-ADIV)}$ | FMC_CLK low to FMC_AD[15:0] invalid | 0 | - | ns |
| $t_{su(ADV-CLKH)}$ | FMC_A/D[15:0] valid data before FMC_CLK high | 4 | - | |
| $t_{h(CLKH-ADV)}$ | FMC_A/D[15:0] valid data after FMC_CLK high | 6 | - | |
| $t_{su(NWAIT-CLKH)}$ | FMC_NWAIT valid before FMC_CLK high | 3 | - | |
| $t_{h(CLKH-NWAIT)}$ | FMC_NWAIT valid after FMC_CLK high | 4 | - | |

1. Based on characterization, not tested in production.

**Figure 25. Synchronous multiplexed PSRAM write timings**

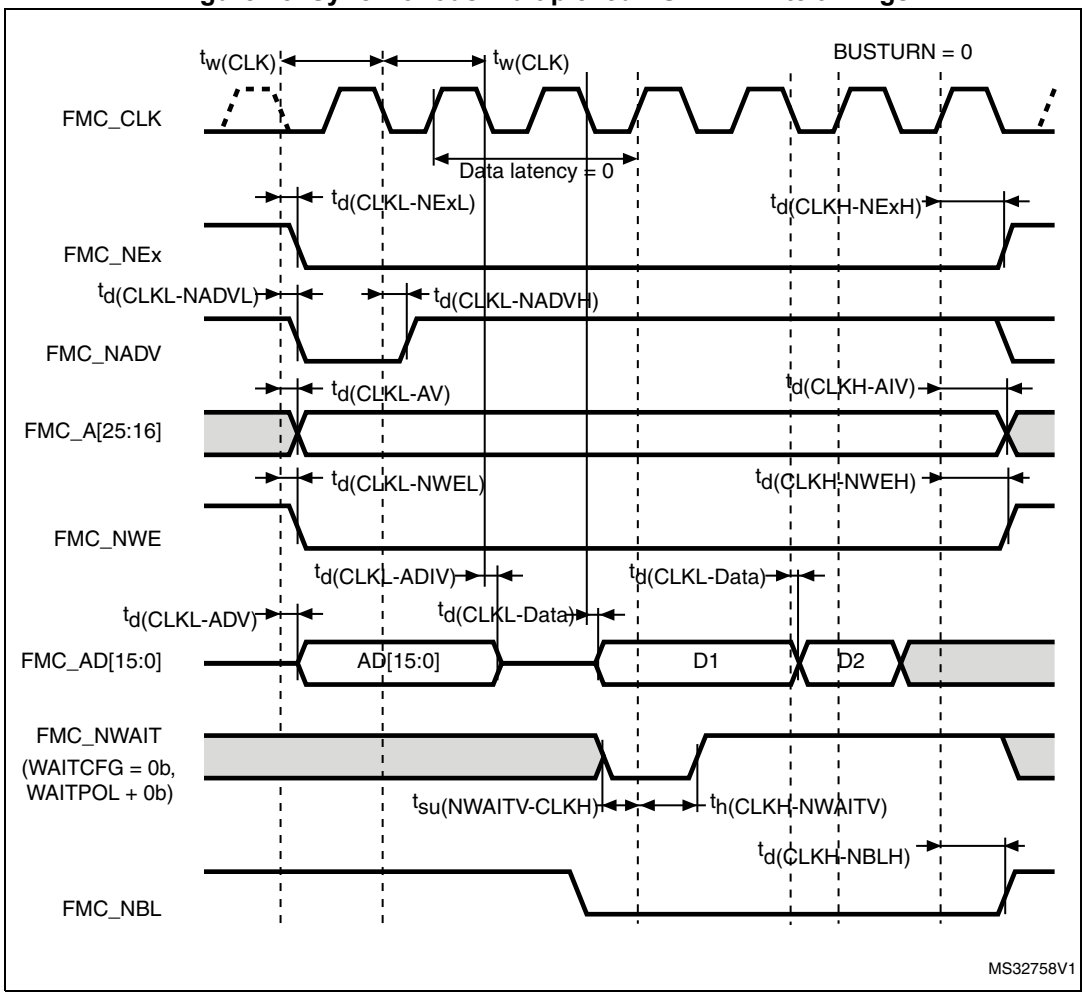


**Table 55. Synchronous non-multiplexed NOR/PSRAM read timings(1) (continued)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{h(CLKH-DV)}$ | FMC_D[15:0] valid data after FMC_CLK high | 5 | - | ns |
| $t_{su(NWAIT-CLKH)}$ | FMC_NWAIT valid before FMC_CLK high | 2 | - | |
| $t_{h(CLKH-NWAIT)}$ | FMC_NWAIT valid after FMC_CLK high | 4 | - | |

1. Based on characterization, not tested in production.

**Figure 27. Synchronous non-multiplexed PSRAM write timings**

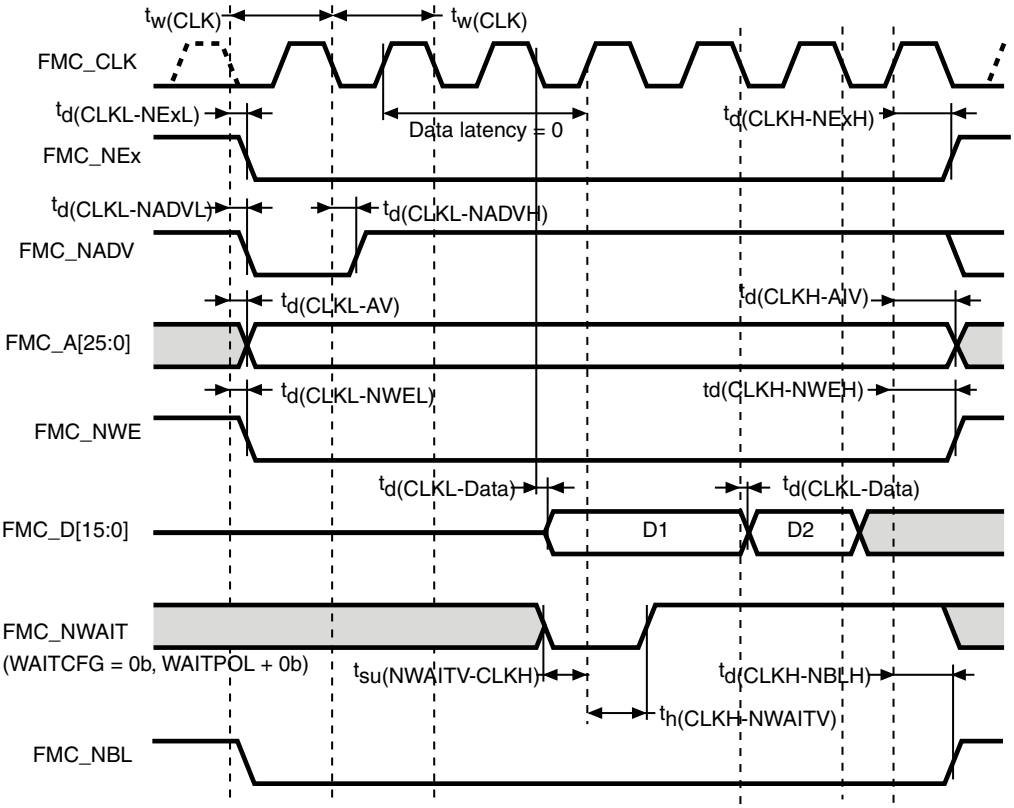
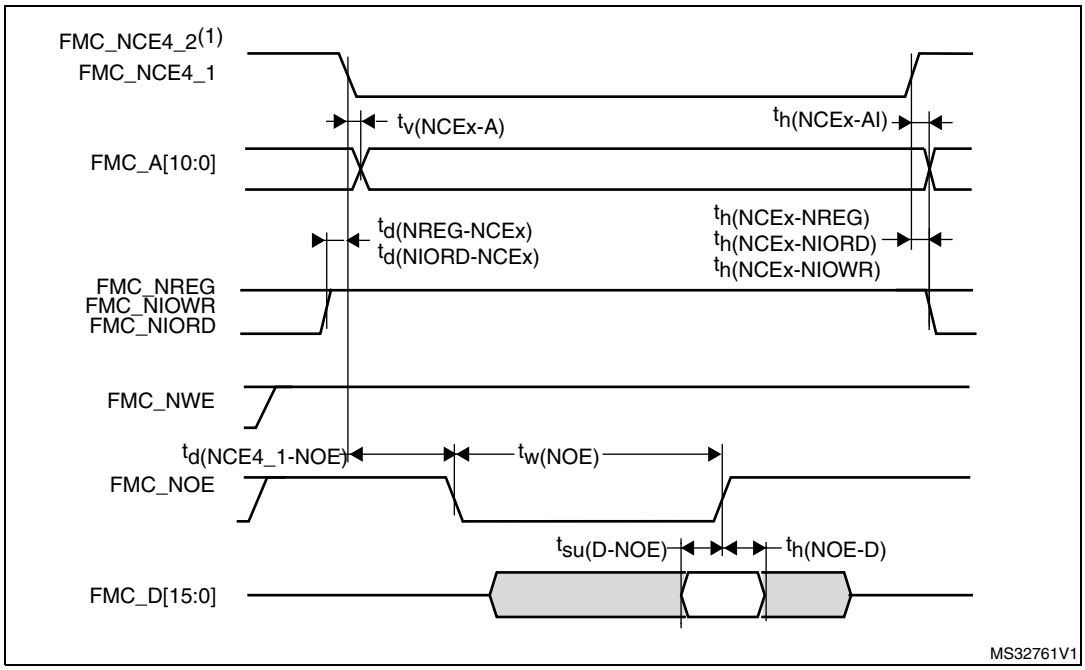


**Figure 28. PC Card/CompactFlash controller waveforms for common memory read access**




1. FMC_NCE4_2 remains high (inactive during 8-bit access.

**Figure 29. PC Card/CompactFlash controller waveforms for common memory write access**

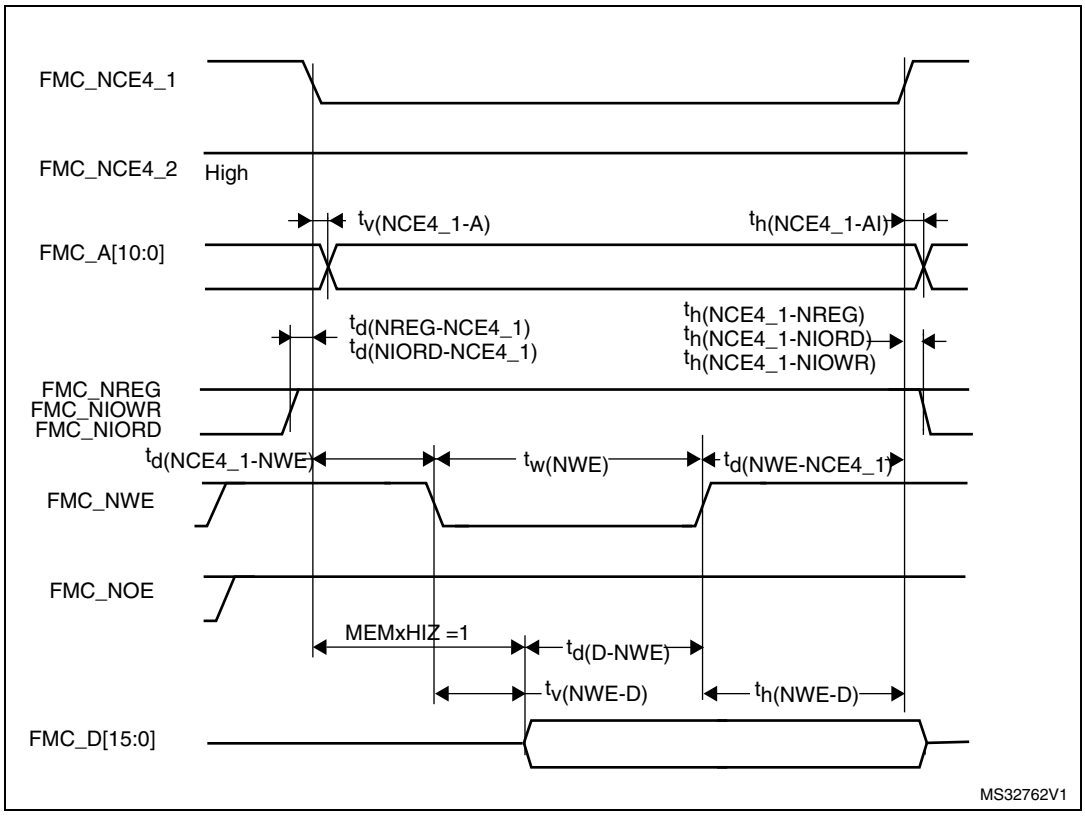


**Figure 32. PC Card/CompactFlash controller waveforms for I/O space read access**

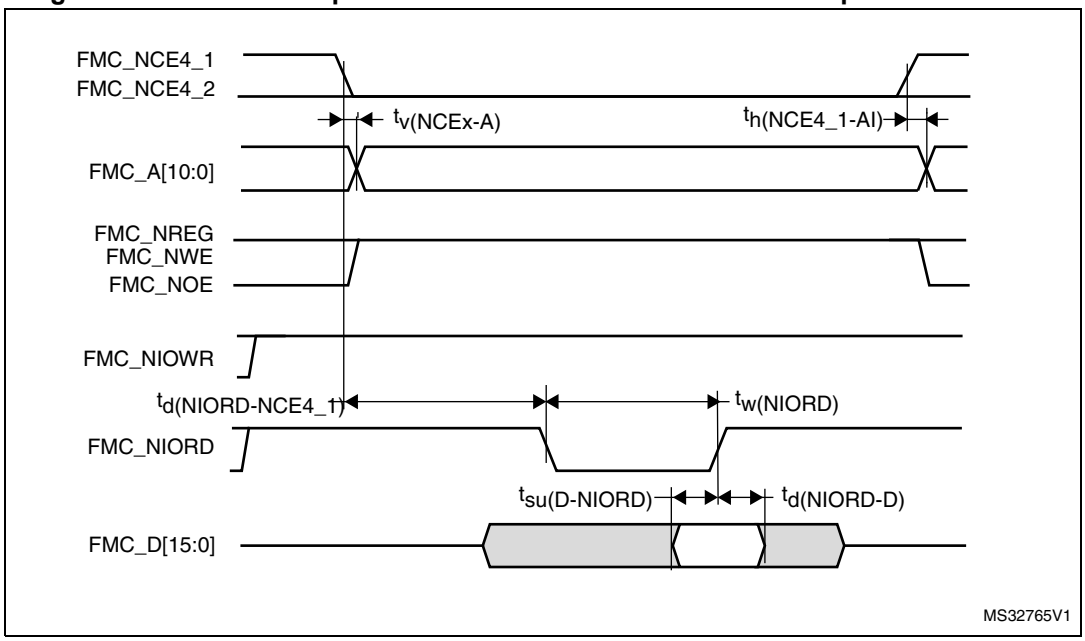
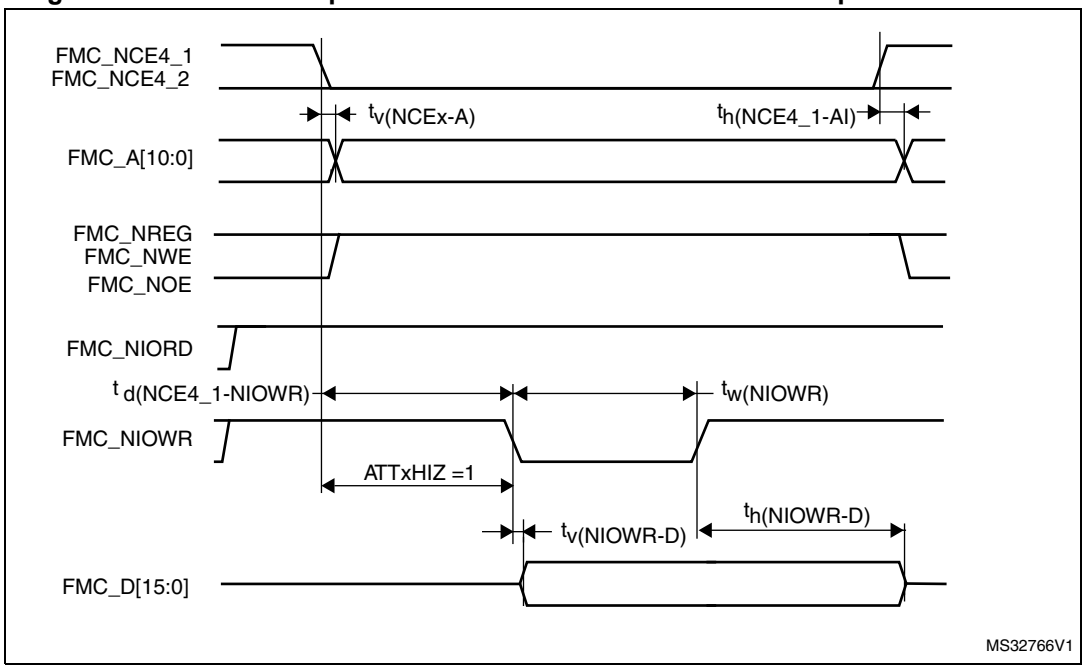



**Figure 33. PC Card/CompactFlash controller waveforms for I/O space write access**



### Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 40* and *Table 68*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 19*.

**Table 68. I/O AC characteristics(1)**

| OSPEEDRy [1:0] value(1) | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| x0 | $f_{max(IO)out}$ | Maximum frequency(2) | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | - | 2(3) | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | - | 125(3) | ns |
| | $t_{r(IO)out}$ | Output low to high level rise time | | - | 125(3) | |
| 01 | $f_{max(IO)out}$ | Maximum frequency(2) | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | - | 10(3) | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | - | 25(3) | ns |
| | $t_{r(IO)out}$ | Output low to high level rise time | | - | 25(3) | |
| 11 | $f_{max(IO)out}$ | Maximum frequency(2) | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 50(3) | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 30(3) | |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 2.7 V | - | 20(3) | |
| | $t_{f(IO)out}$ | Output high to low level fall time | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 5(3) | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 8(3) | |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 2.7 V | - | 12(3) | |
| | $t_{r(IO)out}$ | Output low to high level rise time | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 5(3) | |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 8(3) | |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 2.7 V | - | 12(3) | |
| FM+ configuration(4) | $f_{max(IO)out}$ | Maximum frequency(2) | $C_L$ = 50 pF, $V_{DD}$ = 2 to 3.6 V | - | 2(4) | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | | - | 12(4) | ns |
| | $t_{r(IO)out}$ | Output low to high level rise time | | - | 34(4) | |
| - | $t_{EXTIpw}$ | Pulse width of external signals detected by the EXTI controller | - | 10(3) | - | ns |

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0316 reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 40*.
3. Guaranteed by design, not tested in production.
4. The I/O speed configuration is bypassed in FM+ I/O mode. Refer to the reference manual RM0316 for a description of FM+ I/O mode configuration.

## USB characteristics

**Table 76. USB startup time**

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| $t_{STARTUP}$(1) | USB transceiver startup time | 1 | µs |

1. Guaranteed by design, not tested in production.

**Table 77. USB DC electrical characteristics**

| Symbol | Parameter | Conditions | Min.(1) | Max.(1) | Unit |
|---|---|---|---|---|---|
| **Input levels** | | | | | |
| $V_{DD}$ | USB operating voltage(2) | - | 3.0(3) | 3.6 | V |
| $V_{DI}$(4) | Differential input sensitivity | I(USB_DP, USB_DM) | 0.2 | - | V |
| $V_{CM}$(4) | Differential common mode range | Includes $V_{DI}$ range | 0.8 | 2.5 | |
| $V_{SE}$(4) | Single ended receiver threshold | - | 1.3 | 2.0 | |
| **Output levels** | | | | | |
| $V_{OL}$ | Static output level low | $R_L$ of 1.5 kΩ to 3.6 V(5) | - | 0.3 | V |
| $V_{OH}$ | Static output level high | $R_L$ of 15 kΩ to $V_{SS}$(5) | 2.8 | 3.6 | |

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F303xD/E USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V $V_{DD}$ voltage range.
4. Guaranteed by design, not tested in production.
5. $R_L$ is the load connected on the USB drivers.

**Figure 47. USB timings: definition of data signal rise and fall time**

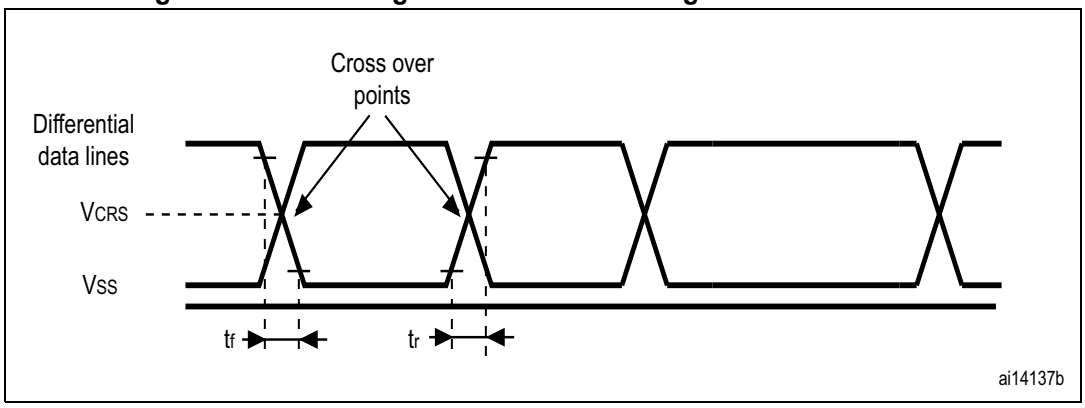



**Table 78. USB: full-speed electrical characteristics(1)**

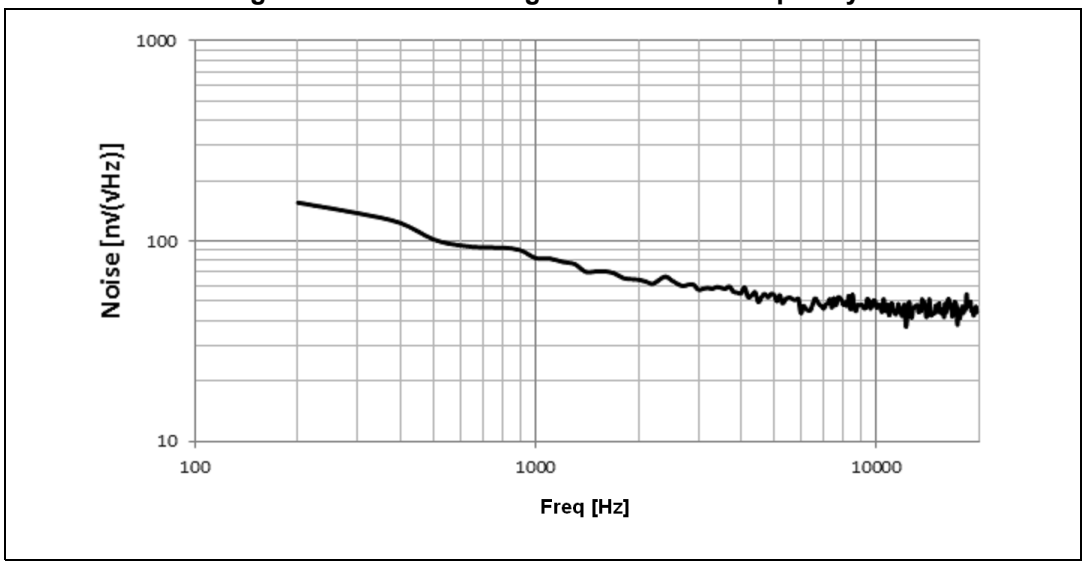
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Driver characteristics** | | | | | | |
| $t_r$ | Rise time(2) | $C_L$ = 50 pF | 4 | - | 20 | ns |
| $t_f$ | Fall time(2) | $C_L$ = 50 pF | 4 | - | 20 | ns |

**Table 82. ADC accuracy, 100-pin/144-pin packages(1)(2)(3) (continued)**

| Symbol | Parameter | Conditions | | | Min (4) | Max(4) | Unit |
|---|---|---|---|---|---|---|---|
| EL | Integral linearity error | ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps, 2.0 V≤ $V_{DDA}$, $V_{REF+}$ ≤ 3.6 V 100-pin/144-pin package | Single Ended | Fast channel 5.1 Ms | - | ±2 | LSB |
| | | | | Slow channel 4.8 Ms | - | ±3 | |
| | | | Differential | Fast channel 5.1 Ms | - | ±2 | |
| | | | | Slow channel 4.8 Ms | - | ±2 | |
| ENOB (5) | Effective number of bits | | Single Ended | Fast channel 5.1 Ms | 10.4 | - | bits |
| | | | | Slow channel 4.8 Ms | 10.2 | - | |
| | | | Differential | Fast channel 5.1 Ms | 10.8 | - | |
| | | | | Slow channel 4.8 Ms | 10.8 | - | |
| SINAD (5) | Signal-to-noise and distortion ratio | | Single Ended | Fast channel 5.1 Ms | 64 | - | dB |
| | | | | Slow channel 4.8 Ms | 63 | - | |
| | | | Differential | Fast channel 5.1 Ms | 67 | - | |
| | | | | Slow channel 4.8 Ms | 67 | - | |
| SNR(5) | Signal-to-noise ratio | | Single Ended | Fast channel 5.1 Ms | 64 | - | |
| | | | | Slow channel 4.8 Ms | 64 | - | |
| | | | Differential | Fast channel 5.1 Ms | 67 | - | |
| | | | | Slow channel 4.8 Ms | 67 | - | |
| THD(5) | Total harmonic distortion | | Single Ended | Fast channel 5.1 Ms | - | 74 | |
| | | | | Slow channel 4.8 Ms | - | -74 | |
| | | | Differential | Fast channel 5.1 Ms | - | -78 | |
| | | | | Slow channel 4.8 Ms | - | -76 | |

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.15* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted $V_{DDA}$, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.
5. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Figure 53. OPAMP voltage noise versus frequency




### 6.3.23 Temperature sensor characteristics

Table 89. TS characteristics

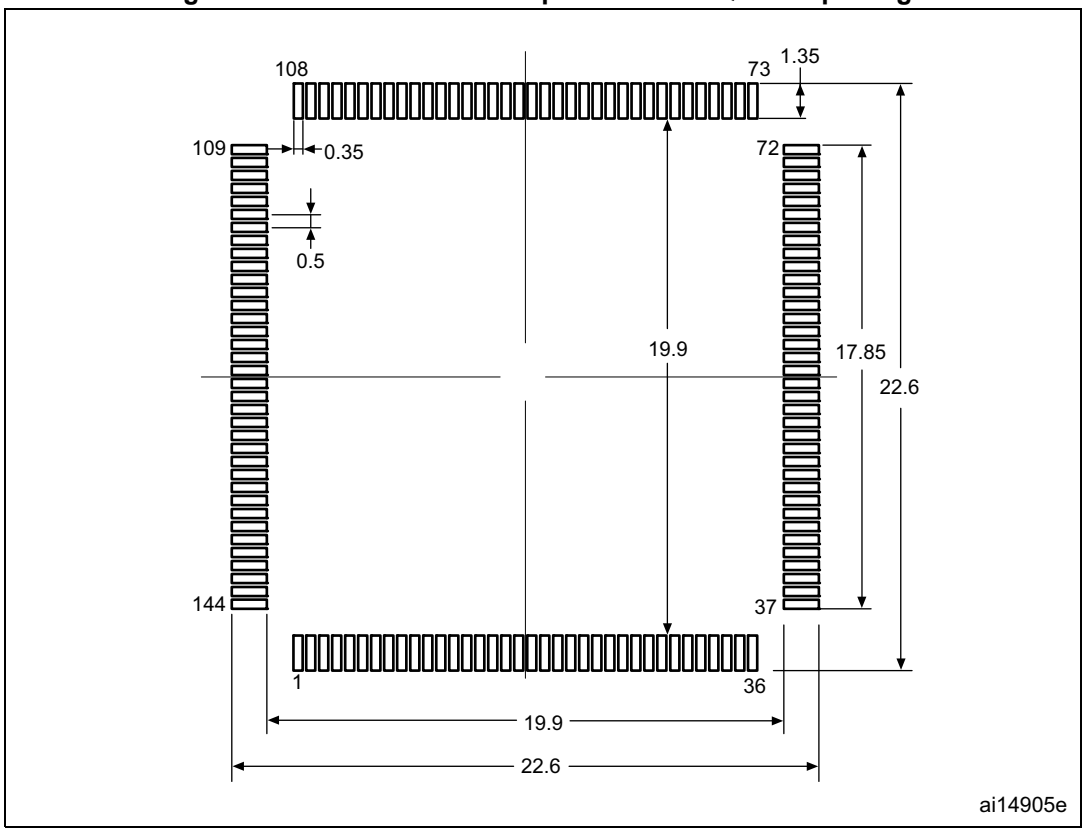
| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_L$(1) | $V_{SENSE}$ linearity with temperature | - | ±1 | ±2 | °C |
| Avg_Slope(1) | Average slope | 4.0 | 4.3 | 4.6 | mV/°C |
| $V_{25}$ | Voltage at 25 °C | 1.34 | 1.43 | 1.52 | V |
| $t_{START}$(1) | Startup time | 4 | - | 10 | µs |
| $T_{S\_temp}$(1)(2) | ADC sampling time when reading the temperature | 2.2 | - | - | µs |

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

Table 90. Temperature sensor calibration values

| Calibration value name | Description | Memory address |
|---|---|---|
| TS_CAL1 | TS ADC raw data acquired at temperature of 30 °C, $V_{DDA}$= 3.3 V | 0x1FFF F7B8 - 0x1FFF F7B9 |
| TS_CAL2 | TS ADC raw data acquired at temperature of 110 °C $V_{DDA}$= 3.3 V | 0x1FFF F7C2 - 0x1FFF F7C3 |

**Figure 55. Recommended footprint for the LQFP144 package**




1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

## 7.7 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 19: General operating conditions*.

The maximum chip-junction temperature, $T_J$ max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A$ max is the maximum temperature in °C,
- $\Theta_{JA}$ is the package junction-to- thermal resistance, in °C/W,
- $P_D$ max is the sum of $P_{INT}$ max and $P_{I/O}$ max ($P_D$ max = $P_{INT}$ max + $P_{I/O}$max),
- $P_{INT}$ max is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual $V_{OL}$ / $I_{OL}$ and $V_{OH}$ / $I_{OH}$ of the I/Os at low and high level in the application.

**Table 99. Package thermal characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | **Thermal resistance junction-** LQFP144 - 20 × 20 mm | 33 | °C/W |
| | **Thermal resistance junction-** UFBGA100 - 7 × 7 mm | 59 | |
| | **Thermal resistance junction-** LQFP100 - 14 × 14 mm | 42 | |
| | **Thermal resistance junction-** WLCSP100 - 0.4 mm pitch | 44 | |
| | **Thermal resistance junction-** LQFP64 - 10 × 10 mm / 0.5 mm pitch | 46 | |

### 7.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

### 7.7.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Part numbering*.

Each temperature range suffix corresponds to a specific guaranteed temperature at maximum dissipation and to a specific maximum junction temperature.

As applications do not commonly use the STM32F303xD/E at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range is best suited to the application.