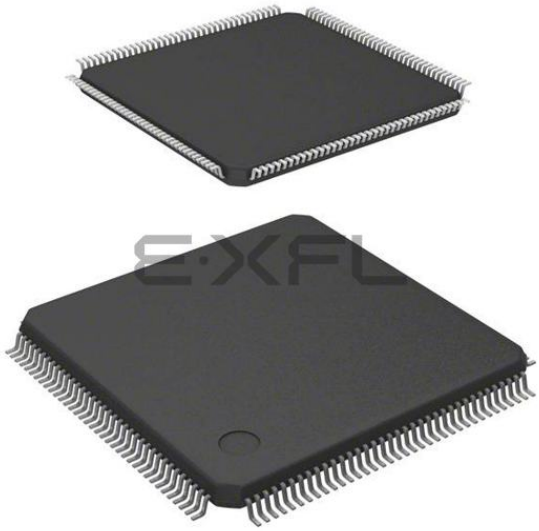

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	115
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 40x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f303zet7

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F303xD/E microcontrollers.

This STM32F303xD/E datasheet should be read in conjunction with the reference manual of STM32F303xB/C/D/E, STM32F358xC and STM32F328x4/6/8 devices (RM0316) available on STMicroelectronics website at *www.st.com*.

For information on the ARM® Cortex®-M4 core with FPU, refer to the following documents:

- *Cortex® -M4 with FPU Technical Reference Manual*, available from the www.arm.com website
- *STM32F3 and STM32F4 Series Cortex® -M4 programming manual* (PM0214) available on STMicroelectronics website at *www.st.com*.

effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

3.13 Interrupts and events

3.13.1 Nested vectored interrupt controller (NVIC)

The STM32F303xD/E devices embed a nested vectored interrupt controller (NVIC) able to handle up to 73 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.14 Fast analog-to-digital converter (ADC)

Four fast analog-to-digital converters 5 MSPS, with selectable resolution between 12 and 6 bit, are embedded in the STM32F303xD/E family devices. The ADCs have up to 40 external channels. Some of the external channels are shared between ADC1&2 and between ADC3&4. The ADCs can perform conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADCs have also internal channels: Temperature sensor connected to ADC1 channel 16, VBAT/2 connected to ADC1 channel 17, Voltage reference VREFINT connected to the 4 ADCs channel 18, VREFOPAMP1 connected to ADC1 channel 15, VREFOPAMP2 connected to ADC2 channel 17, VREFOPAMP3 connected to ADC3 channel 17 and VREFOPAMP4 connected to ADC4 channel 17.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single-shunt phase current reading techniques.

The ADC can be served by the DMA controller.

Three analog watchdogs are available per ADC.

The analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

Table 10. Capacitive sensing GPIOs available on STM32F303xD/E devices (continued)

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
3	TSC_G3_IO1	PC5	7	TSC_G7_IO1	PE2
	TSC_G3_IO2	PB0		TSC_G7_IO2	PE3
	TSC_G3_IO3	PB1		TSC_G7_IO3	PE4
	TSC_G3_IO4	PB2		TSC_G7_IO4	PE5
4	TSC_G4_IO1	PA9	8	TSC_G8_IO1	PD12
	TSC_G4_IO2	PA10		TSC_G8_IO2	PD13
	TSC_G4_IO3	PA13		TSC_G8_IO3	PD14
	TSC_G4_IO4	PA14		TSC_G8_IO4	PD15

Table 11. Number of capacitive sensing channels available on STM32F303xD/E devices

Analog I/O group	Number of capacitive sensing channels	
	STM32F303VE/ZE	STM32F303RE
G1	3	3
G2	3	3
G3	3	3
G4	3	3
G5	3	3
G6	3	3
G7	3	0
G8	3	0
Number of capacitive sensing channels	24	18

3.28 Development support

3.28.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.28.2 Embedded Trace Macrocell

The ARM embedded trace macrocell (ETM™) provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F303xD/E through a small number of ETM™ pins to an external hardware trace

Figure 5. STM32F303xD/E LQFP100 pinout

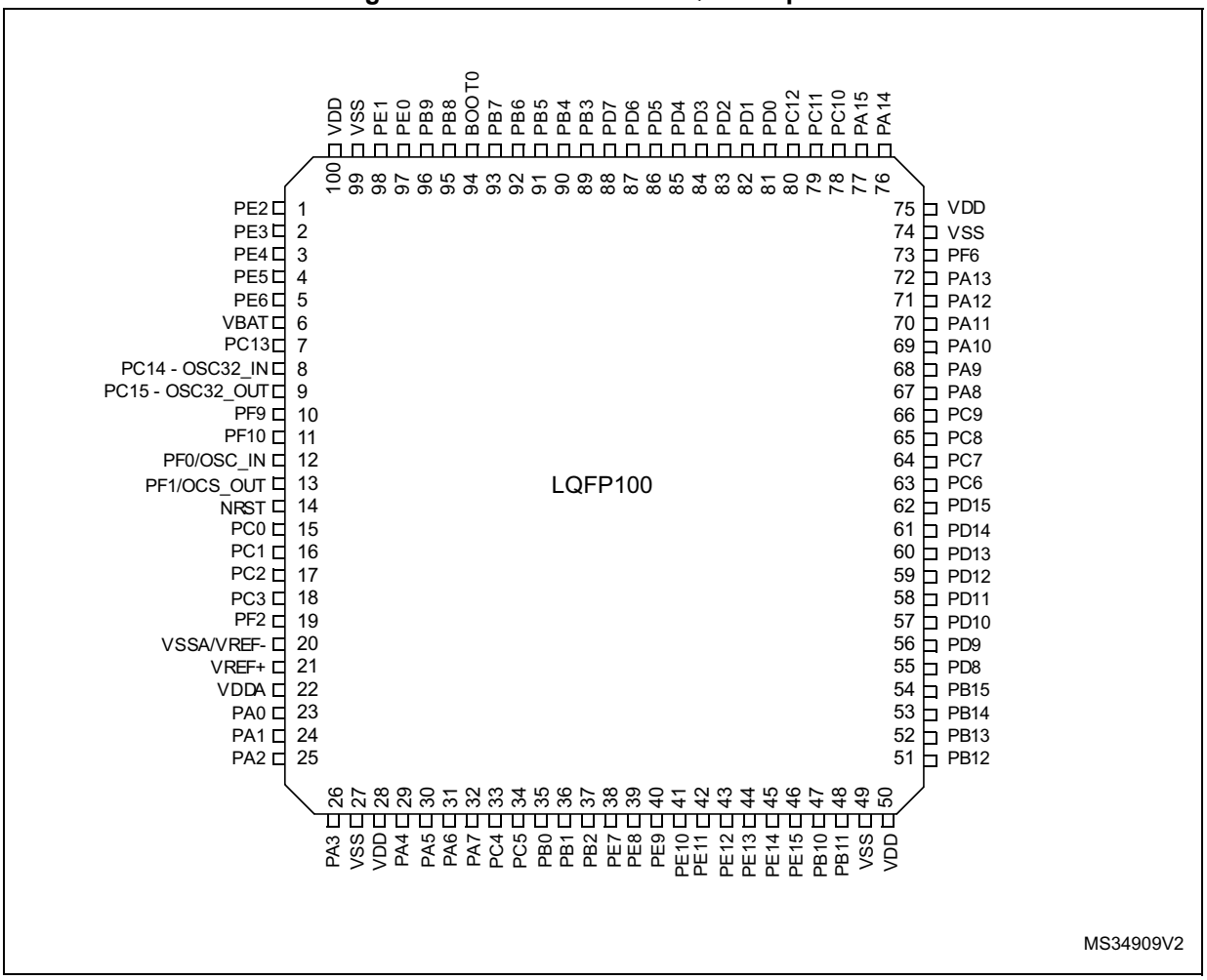


Table 13. STM32F303xD/E pin definitions

Pin number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	UFBGA100	WLCSP100	LQFP144						
-	1	B2	D6	1	PE2	I/O	FT	(1)	TRACECK, EVENTOUT, TIM3_CH1, TSC_G7_IO1, SPI4_SCK, TIM20_CH1, FMC_A23	-
-	2	A1	D7	2	PE3	I/O	FT	(1)	TRACED0, EVENTOUT, TIM3_CH2, TSC_G7_IO2, SPI4_NSS, TIM20_CH2, FMC_A19	-
-	3	B1	C8	3	PE4	I/O	FT	(1)	TRACED1, EVENTOUT, TIM3_CH3, TSC_G7_IO3, SPI4_NSS, TIM20_CH1N, FMC_A20	-
-	4	C2	B9	4	PE5	I/O	FT	(1)	TRACED2, EVENTOUT, TIM3_CH4, TSC_G7_IO4, SPI4_MISO, TIM20_CH2N, FMC_A21	-
-	5	D2	E7	5	PE6	I/O	FT	(1)	TRACED3, EVENTOUT, SPI4_MOSI, TIM20_CH3N, FMC_A22	WKUP3, RTC_TAMP3
1	6	E2	D8	6	VBAT	S	-	-	-	-
2	7	C1	C9	7	PC13(2)	I/O	TC	-	EVENTOUT, TIM1_CH1N	WKUP2,RTC_TAMP1, RTC_TS, RTC_OUT
3	8	D1	C10	8	PC14 - OSC32_IN (2)	I/O	TC	-	EVENTOUT	OSC32_IN
4	9	E1	D9	9	PC15 - OSC32_OUT(2)	I/O	TC	-	EVENTOUT	OSC32_OUT
-	-	-	-	10	PH0	I/O	FT	(1)	EVENTOUT, TIM20_CH1, FMC_A0	-
-	-	-	-	11	PH1	I/O	FT	(1)	EVENTOUT, TIM20_CH2, FMC_A1	-
-	19	J1	E8	12	PF2	I/O	TTa	(1)	EVENTOUT, TIM20_CH3, FMC_A2	ADC12_IN10
-	-	-	-	13	PF3	I/O	FT	(1)	EVENTOUT, TIM20_CH4, FMC_A3	-

Table 14. STM32F303xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM12/3/4/8/20/15/GPCOMP1	I2C3/TIM8/20/15/GPCOMP7/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/TIM8/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP3/5/6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port B	PB14	-	TIM15_CH1	-	TSC_G6_IO4	-	SPI2_MISO/I2S2ext_SD	TIM1_CH2N	USART3_RTS	-	-	-	-	-	-	-	EVENTOUT
	PB15	RTC_REFIN	TIM15_CH2	TIM15_CH1N	-	TIM1_CH3N	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-	-	-	-	EVENTOUT
Port C	PC0	-	EVENTOUT	TIM1_CH1	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC1	-	EVENTOUT	TIM1_CH2	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC2	-	EVENTOUT	TIM1_CH3	COMP7_OUT	-	-	-	-	-	-	-	-	-	-	-	-
	PC3	-	EVENTOUT	TIM1_CH4	-	-	-	TIM1_BKIN2	-	-	-	-	-	-	-	-	-
	PC4	-	EVENTOUT	TIM1_ETR	-	-	-	-	USART1_TX	-	-	-	-	-	-	-	-
	PC5	-	EVENTOUT	TIM15_BKIN	TSC_G3_IO1	-	-	-	USART1_RX	-	-	-	-	-	-	-	-
	PC6	-	EVENTOUT	TIM3_CH1	-	TIM8_CH1	-	I2S2_MCK	COMP6_OUT	-	-	-	-	-	-	-	-
	PC7	-	EVENTOUT	TIM3_CH2	-	TIM8_CH2	-	I2S3_MCK	COMP5_OUT	-	-	-	-	-	-	-	-
	PC8	-	EVENTOUT	TIM3_CH3	-	TIM8_CH3	-	-	COMP3_OUT	-	-	-	-	-	-	-	-
	PC9	-	EVENTOUT	TIM3_CH4	I2C3_SDA	TIM8_CH4	I2SCKIN	TIM8_BKIN2	-	-	-	-	-	-	-	-	-

Table 14. STM32F303xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3/TIM8/20/15/GPCOMP7/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/TIM8/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP3/5/6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port E	PE12	-	EVENT OUT	TIM1_CH3N	-	-	SPI4_SCK	-	-	-	-	-	-	FMC_D9	-	-	-
	PE13	-	EVENT OUT	TIM1_CH3	-	-	SPI4_MISO	-	-	-	-	-	-	FMC_D10	-	-	-
	PE14	-	EVENT OUT	TIM1_CH4	-	-	SPI4_MOSI	TIM1_BKIN2	-	-	-	-	-	FMC_D11	-	-	-
	PE15	-	EVENT OUT	TIM1_BKIN	-	-	-	-	USART3_RX	-	-	-	-	FMC_D12	-	-	-
Port F	PF0	-	EVENT OUT	-	-	I2C2_SDA	SPI2_NSS/I2S2_WS	TIM1_CH3N	-	-	-	-	-	-	-	-	-
	PF1	-	EVENT OUT	-	-	I2C2_SCL	SPI2_SCK/I2S2_CK	-	-	-	-	-	-	-	-	-	-
	PF2	-	EVENT OUT	TIM20_CH3	-	-	-	-	-	-	-	-	-	FMC_A2	-	-	-
	PF3	-	EVENT OUT	TIM20_CH4	-	-	-	-	-	-	-	-	-	FMC_A3	-	-	-
	PF4	-	EVENT OUT	COMP1_OUT	TIM20_CH1N	-	-	-	-	-	-	-	-	FMC_A4	-	-	-
	PF5	-	EVENT OUT	TIM20_CH2N	-	-	-	-	-	-	-	-	-	FMC_A5	-	-	-
	PF6	-	EVENT OUT	TIM4_CH4	-	I2C2_SCL	-	-	USART3_RTS	-	-	-	-	FMC_NIORD	-	-	-
	PF7	-	EVENT OUT	TIM20_BKIN	-	-	-	-	-	-	-	-	-	FMC_NREG	-	-	-

Table 14. STM32F303xD/E alternate function mapping (continued)

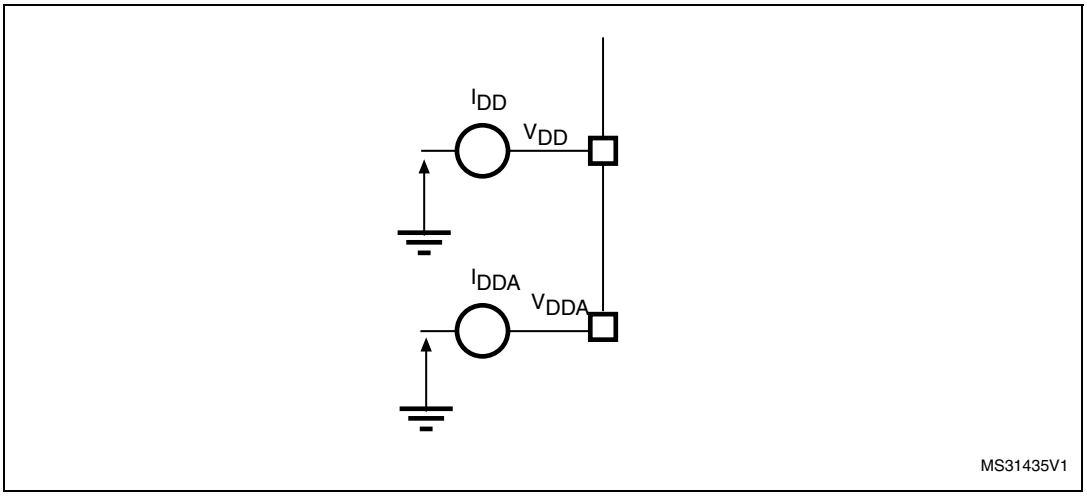
Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM12/3/4/8/20/15/GPCOMP1	I2C3/TIM8/20/15/GPCOMP7/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/TIM8/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP3/5/6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port G	PG5	-	EVENT OUT	TIM20_ETR	-	-	-	-	-	-	-	-	-	FMC_A15	-	-	-
	PG6	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_INT2	-	-	-
	PG7	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_INT3	-	-	-
	PG8	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PG9	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_NE2/FMC_NCE3	-	-	-
	PG10	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_NCE4_1/FMC_NE3	-	-	-
	PG11	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_NCE4_2	-	-	-
	PG12	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_NE4	-	-	-
	PG13	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A24	-	-	-
	PG14	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A25	-	-	-
	PG15	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Table 15. Memory map, peripheral register boundary addresses (continued)

Bus	Boundary address	Size (bytes)	Peripheral
-	0x4001 8000 - 0x4001 FFFF	32 K	Reserved
	0x4001 5400 - 0x4001 7FFF	11 K	Reserved
	0x4001 5000 - 0x4001 53FF	1 K	TIM20
	0x4001 4C00 - 0x4001 4FFF	1 K	Reserved
	0x4001 4800 - 0x4001 4BFF	1 K	TIM17
	0x4001 4400 - 0x4001 47FF	1 K	TIM16
	0x4001 4000 - 0x4001 43FF	1 K	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 K	SPI4
	0x4001 3800 - 0x4001 3BFF	1 K	USART1
	0x4001 3400 - 0x4001 37FF	1 K	TIM8
	0x4001 3000 - 0x4001 33FF	1 K	SPI1
APB2	0x4001 2C00 - 0x4001 2FFF	1 K	TIM1
	0x4001 0800 - 0x4001 2BFF	9 K	Reserved
	0x4001 0400 - 0x4001 07FF	1 K	EXTI
	0x4001 0000 - 0x4001 03FF	1 K	SYSCFG + COMP + OPAMP
-	0x4000 7C00 - 0x4000 FFFF	32 K	Reserved

6.1.7 Current consumption measurement

Figure 13. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 16: Voltage characteristics*, *Table 17: Current characteristics*, and *Table 18: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 16. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{BAT} and V_{DD})	-0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	
V_{REF+}–V_{DDA}(2)	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	
V_{IN}(3)	Input voltage on FT and FTf pins	V_{SS} –0.3	V_{DD} + 4.0	V
	Input voltage on TTa pins	V_{SS} –0.3	4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
	Input voltage on Boot0 pin	0	9	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.13: Electrical sensitivity characteristics*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range. The following relationship must be respected between V_{DDA} and V_{DD}:
V_{DDA} must power on before or at the same time as V_{DD} in the power up sequence.
V_{DDA} must be greater than or equal to V_{DD}.
2. V_{REF+} must be always lower or equal than V_{DDA} ($V_{REF+} \leq V_{DDA}$). If unused then it must be connected to V_{DDA}.
3. V_{IN} maximum must always be respected. Refer to *Table 17: Current characteristics* for the maximum allowed injected current values.

Table 32. Switching output I/O current consumption

Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ	Unit
I_{SW}	I/O current consumption	V_{DD} = 3.3 V C_{ext} = 0 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.90	mA
			4 MHz	0.93	
			8 MHz	1.16	
			18 MHz	1.60	
			36 MHz	2.51	
			48 MHz	2.97	
		V_{DD} = 3.3 V C_{ext} = 10 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.93	
			4 MHz	1.06	
			8 MHz	1.47	
			18 MHz	2.26	
			36 MHz	3.39	
			48 MHz	5.99	
		V_{DD} = 3.3 V C_{ext} = 22 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.03	
			4 MHz	1.30	
			8 MHz	1.79	
			18 MHz	3.01	
			36 MHz	5.99	
		V_{DD} = 3.3 V C_{ext} = 33 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.10	
			4 MHz	1.31	
			8 MHz	2.06	
			18 MHz	3.47	
			36 MHz	8.35	
		V_{DD} = 3.3 V C_{ext} = 47 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.20	
			4 MHz	1.54	
			8 MHz	2.46	
			18 MHz	4.51	
			36 MHz	9.98	

1. CS = 5 pF (estimated value).

Figure 26. Synchronous non-multiplexed NOR/PSRAM read timings

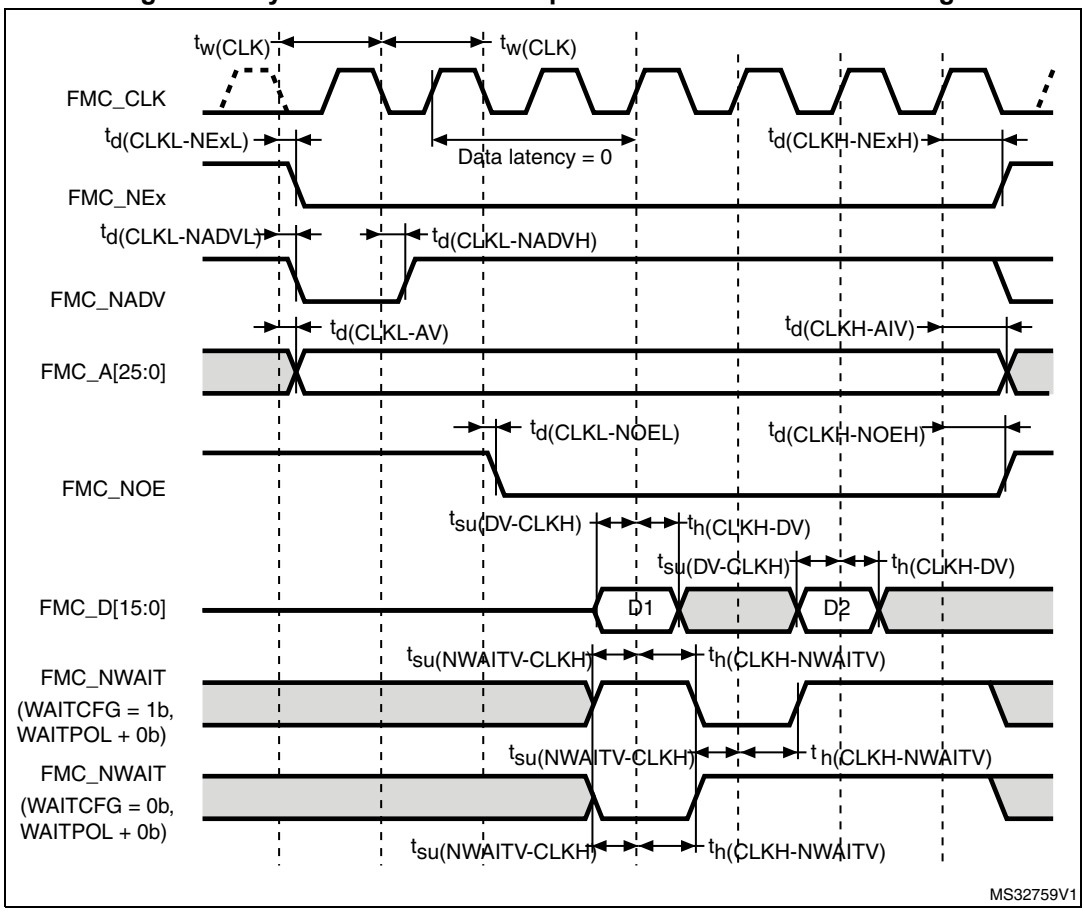


Table 55. Synchronous non-multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	2THCLK-1	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	THCLK+1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	7	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	2.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	7	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	THCLK	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	6	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	THCLK+1	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	3.5	-	

Table 73. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Pulse width of spikes that are suppressed by the analog filter	50	260	ns

1. Guaranteed by design, not tested in production.

SPI/I²S characteristics

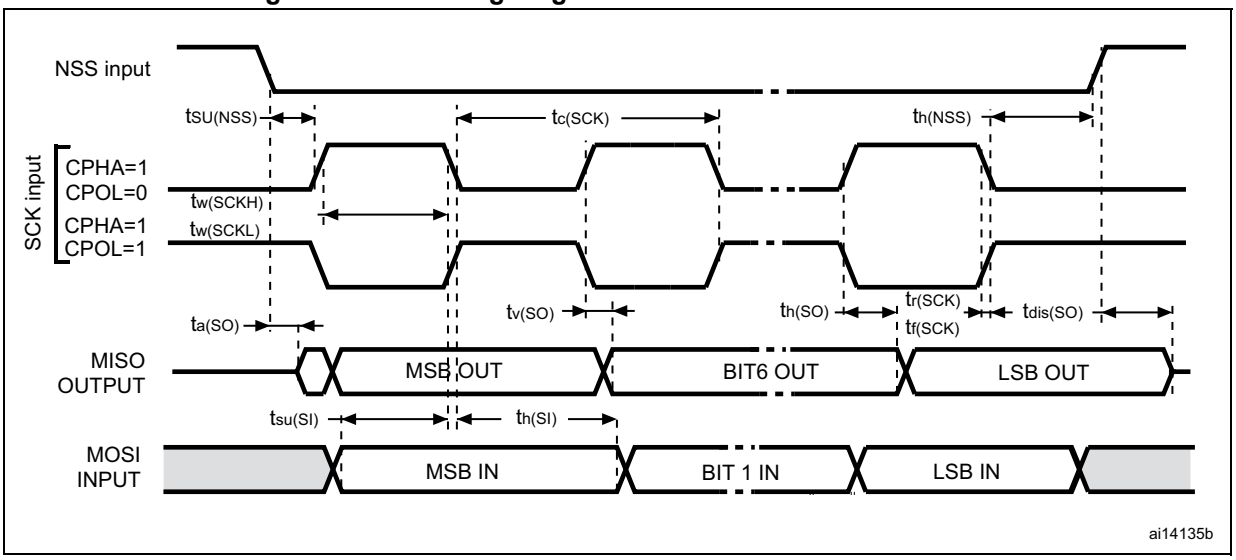
Unless otherwise specified, the parameters given in *Table 74* for SPI or in *Table 75* for I²S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 19*.

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 74. SPI characteristics(1)

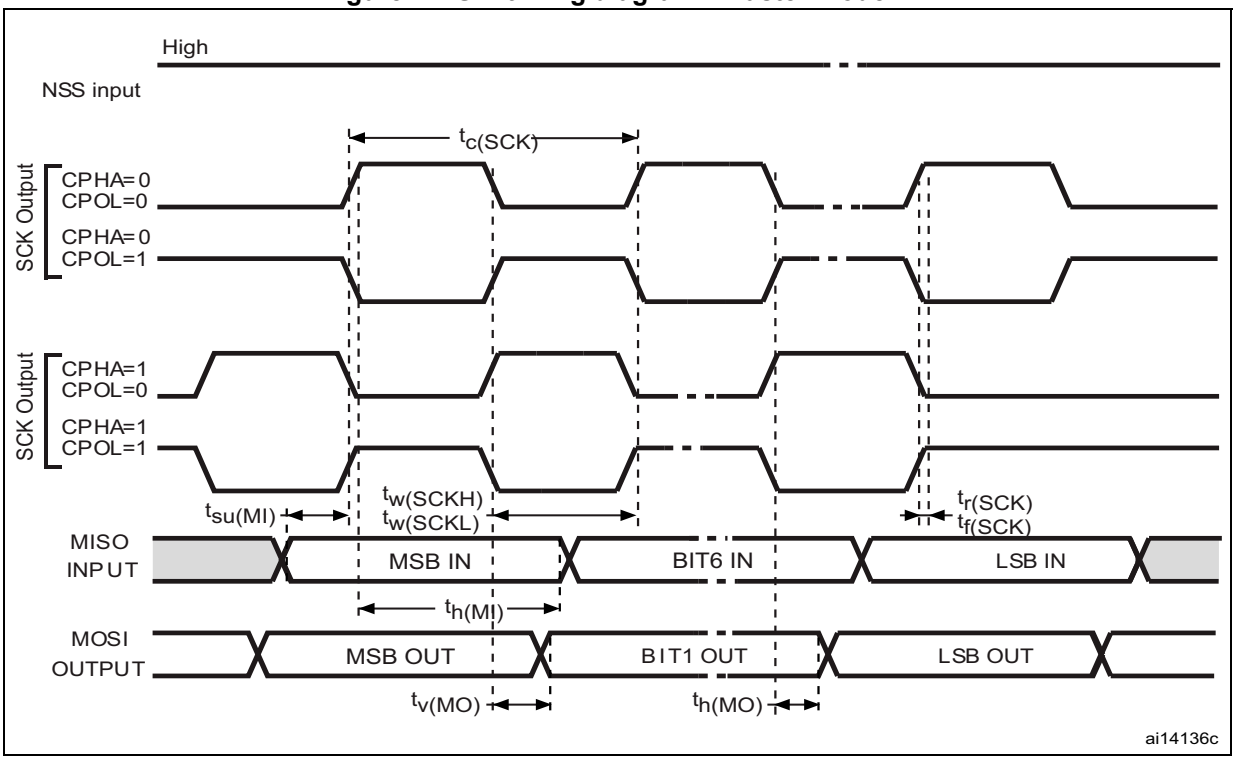
Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode 2.7 V<V_{DD}<3.6 V, SPI1/4	-	-	24	MHz
		Master mode 2 V<V_{DD}<3.6 V, SPI1/2/3/4			18	
		Slave mode 2 V<V_{DD}<3.6 V, SPI1/4			24	
		Slave mode 2 V<V_{DD}<3.6 V, SPI1/2/3/4			18	
		Slave mode transmitter/full duplex 2 V<V_{DD}<3.6 V, SPI1/2/3/4			16.5(2)	
		Slave mode transmitter/full duplex 2.7 V<V_{DD}<3.6 V, SPI1/4			22.5(2))	-
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	3	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	6.5	-	-	
$t_{h(SI)}$		Slave mode	4.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	10	-	30	
$t_{dis(SO)}$	Data output disable time	Slave mode	8	-	7	

Figure 43. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Figure 44. SPI timing diagram - master mode(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Table 82. ADC accuracy, 100-pin/144-pin packages(1)(2)(3) (continued)

Symbol	Parameter	Conditions			Min (4)	Max(4)	Unit
EL	Integral linearity error	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps, 2.0 V≤ V_{DDA}, V_{REF+} ≤ 3.6 V 100-pin/144-pin package	Single Ended	Fast channel 5.1 Ms	-	±2	LSB
				Slow channel 4.8 Ms	-	±3	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2	
ENOB (5)	Effective number of bits		Single Ended	Fast channel 5.1 Ms	10.4	-	bits
				Slow channel 4.8 Ms	10.2	-	
			Differential	Fast channel 5.1 Ms	10.8	-	
				Slow channel 4.8 Ms	10.8	-	
SINAD (5)	Signal-to-noise and distortion ratio		Single Ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	63	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
SNR(5)	Signal-to-noise ratio		Single Ended	Fast channel 5.1 Ms	64	-	
				Slow channel 4.8 Ms	64	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
THD(5)	Total harmonic distortion		Single Ended	Fast channel 5.1 Ms	-	74	
				Slow channel 4.8 Ms	-	-74	
			Differential	Fast channel 5.1 Ms	-	-78	
				Slow channel 4.8 Ms	-	-76	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.15* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.
5. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Table 83. ADC accuracy - limited test conditions, 64-pin packages(1)(2) (continued)

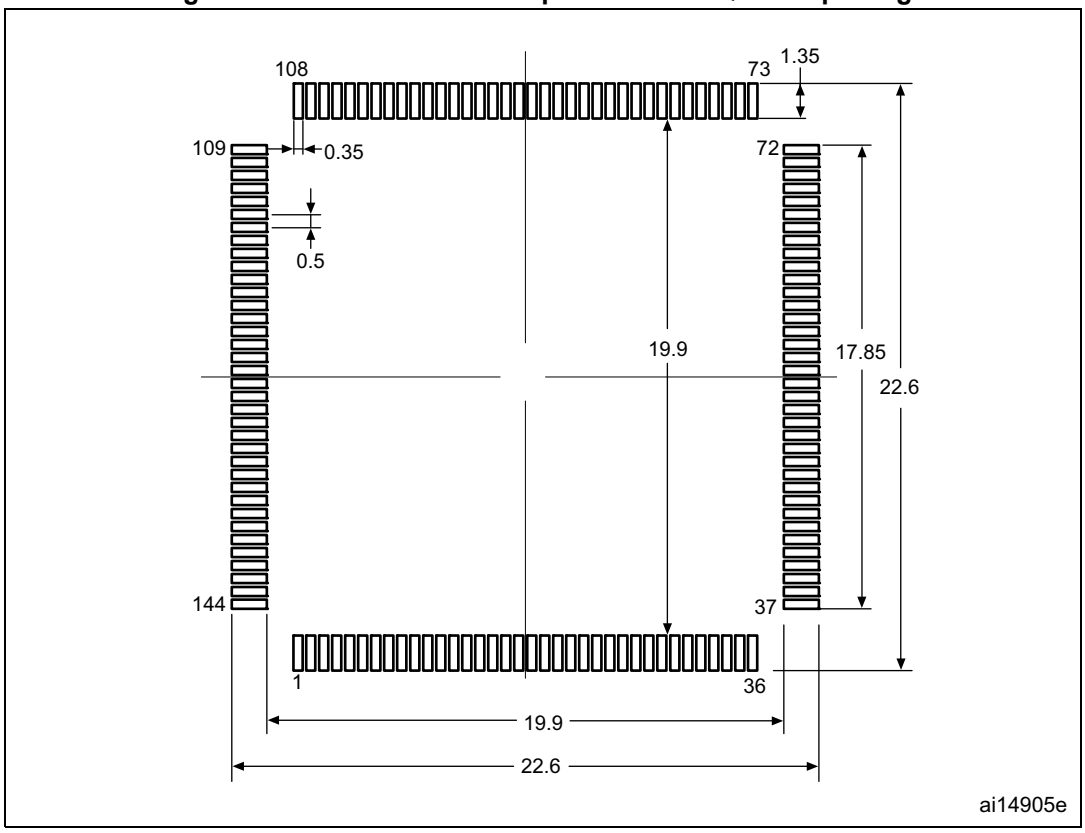
Symbol	Parameter	Conditions			Min (3)	Typ	Max (3)	Unit
SNR(4)	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz Sampling freq ≤ 5 Msps V_{DDA} = 3.3 V 25°C 64-pin package	Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	
THD(4)	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-80	-80	
				Slow channel 4.8 Ms	-	-78	-77	
			Differential	Fast channel 5.1 Ms	-	-83	-82	
				Slow channel 4.8 Ms	-	-81	-80	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.15* does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.
4. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Table 84. ADC accuracy, 64-pin packages(1)(2)(3)

Symbol	Parameter	Conditions			Min(4)	Max (4)	Unit
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps 2.0 V ≤ V_{DDA} ≤ 3.6 V 64-pin package	Single ended	Fast channel 5.1 Ms	-	±6.5	LSB
				Slow channel 4.8 Ms	-	±6.5	
			Differential	Fast channel 5.1 Ms	-	±4	
				Slow channel 4.8 Ms	-	±4.5	
EO	Offset error		Single ended	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3	
			Differential	Fast channel 5.1 Ms	-	±2.5	
				Slow channel 4.8 Ms	-	±2.5	
EG	Gain error		Single ended	Fast channel 5.1 Ms	-	±6	
				Slow channel 4.8 Ms	-	±6	
			Differential	Fast channel 5.1 Ms	-	±3.5	
				Slow channel 4.8 Ms	-	±4	
ED	Differential linearity error		Single ended	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
			Differential	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	

Figure 55. Recommended footprint for the LQFP144 package



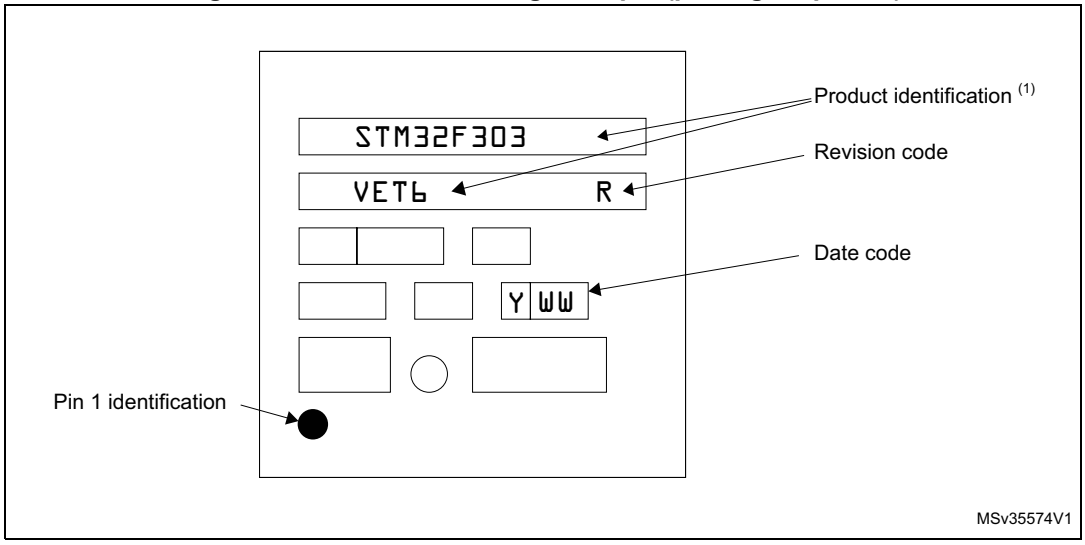
1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Device marking for LQFP100

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 62. LQFP100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

9 Revision history

Table 101. Document revision history

Date	Revision	Changes
20-Jan-2015	1	Initial release.
30-Jan-2015	2	Updated: – *Table 13: STM32F303xD/E pin definitions* – *Table 14: STM32F303xD/E alternate function mapping* – *Table 38: HSE oscillator characteristics* – *Figure 56: LQFP144 marking example (package top view)* – *Figure 62: LQFP100 marking example (package top view)*
03-Mar-2015	3	Added USB_DM and USB_DP as additional function to PA11 and PA12 description, respectively in *Table 13: STM32F303xD/E pin definitions*. Updated: – *Figure 56: LQFP144 marking example (package top view)*, – *Figure 59: UFBGA100 marking example (package top view)*, – *Figure 62: LQFP100 marking example (package top view)*.
08-Dec-2015	4	Renamed: – FMC as FSMC, – CCM RAM as CCM SRAM. Removed: – *table: I2C timings specification* and *Figure: I2C bus AC waveforms and measurement circuit* in *Section : I2C interface characteristics*. – Added package information for WLCSP100 in *Section 7: Package information*.
21-Oct-2016	5	Updated: *Table 2: STM32F303xD/E family device features and peripheral counts*, *Section 3.17: Ultra-fast comparators (COMP)*, *Table 66: DAC characteristics*, *Table 61: ADC characteristics*, *Table 13: STM32F303xD/E pin definitions*, *Table 14: STM32F303xD/E alternate function mapping*, *Figure 41: Recommended NRST pin protection* Added: *Table 37: Wakeup time using USART*.