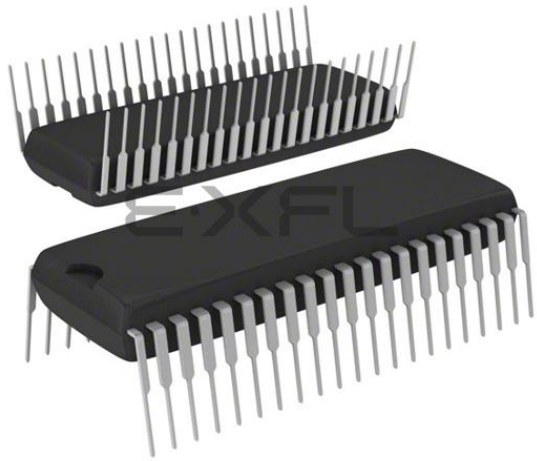

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Details	
Product Status	Obsolete
Applications	TV Controller
Core Processor	Z8
Program Memory Type	OTP (32kB)
Controller Series	Digital Television Controller (DTC)
RAM Size	300 x 8
Interface	I²C, 2-Wire Serial
Number of I/O	27
Voltage - Supply	4.5V ~ 5.5V
Operating Temperature	0°C ~ 70°C
Mounting Type	Through Hole
Package / Case	42-DIP (0.600", 15.24mm)
Supplier Device Package	42-SDIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z9025106psc

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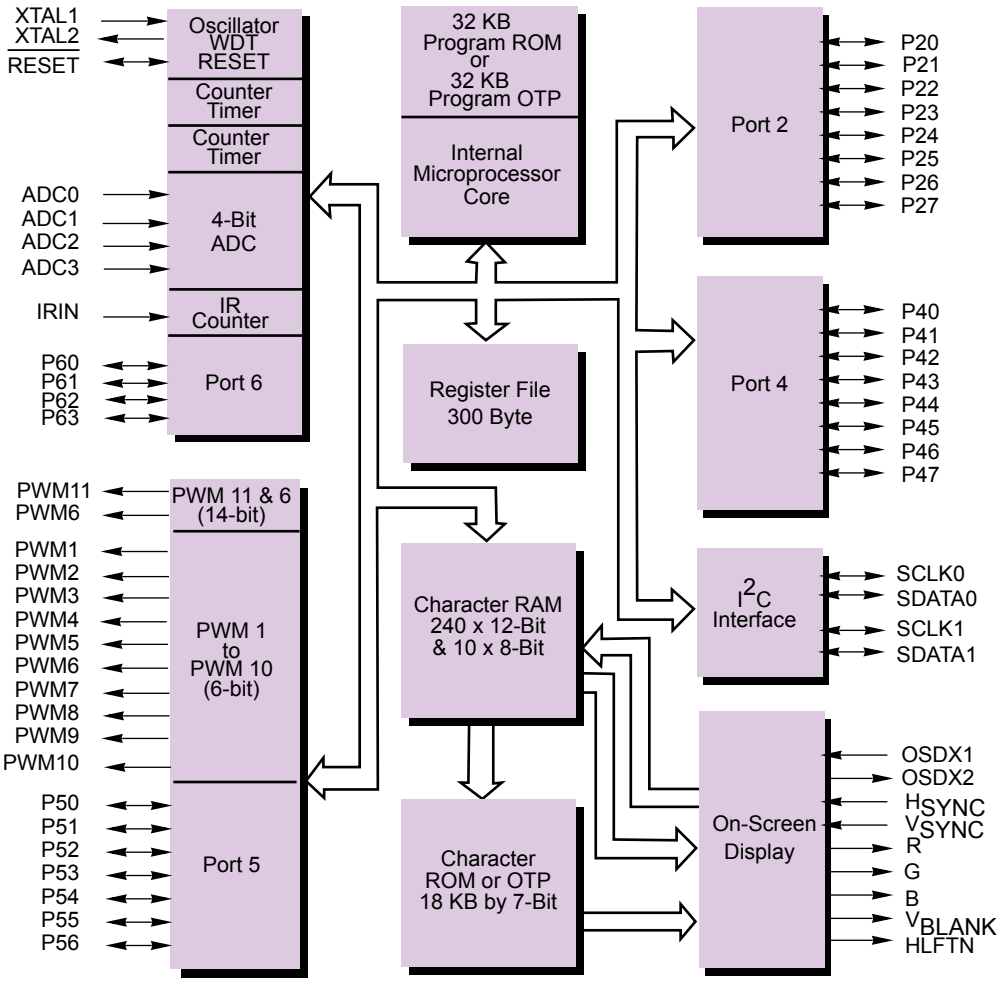

Figure 2 Z90255 Block Diagram

Note: PWM 6 can be either a 6-bit or 14-bit output.

The Z90255 takes full advantage of Zilog's Z8 expanded register file space to offer greater flexibility in creating a user-friendly On-Screen Display (OSD).

Three basic addressing spaces are available: Program memory, Video RAM (VRAM) and the Register file. The register file is composed of 300 bytes of general-purpose registers, 16 control and status registers, one I/O port register and three reserved registers.

Table 3 Multiplexed Pin Descriptions (Continued)

Acronym	Pin Name(s)	Description
P61/ADC2	Port 6 bit 1 or Analog-to-Digital Converter Channel 2	Port 6 bit 1 can be programmed as an input or output line.
P41/ADC1	Port 4 bit 1 or Analog-to-Digital Converter Channel 1	Port 4 bit1 can be programmed as an input or output line.
P44/PWM7	Port 4 bit 4 or Pulse Width Modulator 7	These port pins can be programmed as input or output ports. Each PWM channel has 6-bit resolution.
P45/PWM8	Port 4 bit 5 or Pulse Width Modulator 8	
P46/PWM9	Port 4 bit 6 or Pulse Width Modulator 9	
P47/PWM10	Port 4 bit 7 or Pulse Width Modulator 10	
PWM11/P56	Pulse Width Modulator 11 or Port 5 bit 6	The PWM signal-generator channel has 14-bit resolution. Port 5 bit 6 and port 5 bit 5 can be programmed as inputs or outputs.
PWM6/P55	Pulse Width Modulator 6 or Port 5 bit 5	
PWM6/P55	Pulse Width Modulator 6 or Port 5 bit 5	These port pins can be programmed as input or output ports. Each PWM signal-generator channel has 6-bit resolution.
PWM5/P54	Pulse Width Modulator 5 or Port 5 bit 4	
PWM4/P53	Pulse Width Modulator 4 or Port 5 bit 3	
PWM3/P52	Pulse Width Modulator 3 or Port 5 bit 2	
PWM2/P51	Pulse Width Modulator 2 or Port 5 bit 1	The PWM signal-generator channel has 6-bit resolution. Port 5 bit 1 and Port 5 bit 0 can be programmed as an input or output port.
PWM1/P50	Pulse Width Modulator 1 or Port 5 bit 0	The PWM signal-generator channel has 6-bit resolution. Port 5 bit 0 can be programmed as an input or output port.

Note: PWM6 can be either 6-bit or 14-bit output.

2.2 Expanded Register File

The register file has been expanded to provide additional system control registers, additional general purpose registers, and expanded mapping of peripheral devices and I/O ports in the register address area.

The lower nibble of the Register Pointer (FDh) addresses the Expanded Register File (ERF) Bank. The 0h value in the lower nibble identifies the Standard Register File to be addressed. Any other value from 1h to Fh selects an ERF Bank. When an ERF Bank is selected, register addresses from 00h to 0Fh access the sixteen ERF Bank registers, which in effect replace the first sixteen locations of the Z90255 Standard Register File. Only ERF Bank 4, ERF Bank 5, ERF Bank 6, ERF Bank 7, ERF Bank A, ERF Bank B, ERF Bank C and ERF Bank F are implemented in the Z90255 controller (Table 4).

2.3 Program Memory

The Z90255 has 32KB of program memory. Refer to Figure 6. The first 12 bytes of the program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to interrupt and program control routine addresses which are passed to the specified vector address. The IRQ0 vector is permanently assigned to the IR interrupt request. The IRQ1 vector is permanently assigned to the V_{SYNC} and H_{SYNC} interrupt request. Program memory starts at address 000Ch after being reset.

Table 6 Stop Mode Recovery (SMR) Register 0Bh: Bank F (SMR)

Bit	7	6	5	4	3	2	1	0
R/W	R	W	W	W	W	W	W	W
Reset	0	0	1	0	0	0	0	0
Note: R = Read W = Write X = Indeterminate								

Bit/ Field	Bit Position	R/W	Value	Description
Stop flag	7	R	0 1	POR Stop Recovery
Stop Recovery level	6	W	0 1	Low POR High
Stop Delay	5	W	0 1	Off On POR
Stop Mode Recover Source	4-2	W	000 001 010 011 100 101 110 111	POR and /or External Reset P63 P62 Must NOT be used Must NOT be used P27 P2 NOR 0-3 P2 NOR 0-7
External Clock Divide by 2	1	W	0 1	SCLK/TCLK = XTAL/2 POR SCLK/TCLK = XTAL
SCLK/TCLK Divide by 16	0	W	0 1	Off POR On

SCLK/TCLK Divide-by-16 Select (bit O)

This bit controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to reduce device power consumption selectively during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources counter/timers and interrupt logic).

The Second Color feature can be used to implement an analog bar for volume control, tuning, etc. The change step for color is half the character size. Refer to Tables 8 and 9.

Second Color Control Register

The Second Color Position is the place where the foreground color changes to the color defined in the Second Color Control Register.

Table 11 Second Color Control Register 07h:Bank A (SNDCLR_CNTRL)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate

Bit/ Field	Bit Position	R/W	Value	Description
Second Color Enable	7	R/W	0 1	Disables the second color feature Enables the second color feature
Second Color	6, 5, 4	R/W		R, G, B respectively. Defines the second color after the second color position defined in SNDCLR register.
Row Address	3, 2, 1, 0	R/W		Defines one of the 10 rows (from 0, the first row, to 9, the 10th row).

Second Color Register

Table 12 Second Color Register 08h:Bank A (SNDCLR)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate

Bit/ Field	Bit Position	R/W	Value	Description
Halftone Effect Output Delay on P20	7	R/W	xx/x 00/0 00/1 01/0 01/1 10/0 10/1 11/0 11/1	Bits 5, 4 in ROW_SPACE/ bit 7 No Delay Delay by 0.5 Dot-Clock Period Delay by 1.0 Dot-Clock Period Delay by 1.5 Dot-Clock Period Delay by 2.0 Dot-Clock Period Delay by 2.5 Dot-Clock Period Delay by 3.0 Dot-Clock Period Delay by 3.5 Dot-Clock Period
Mesh Color	6, 5, 4	R/W		Defines the mesh color. B,G,R respectively.
P20 for Halftoning	3	R/W	0 1	Normal Mesh effect Use P20 Output for Halftoning
Software Field Number/ Polarity of Halftone Effect Output	2	R/W	0 1	Even Field/Positive Halftone Effect Output Odd Field/Negative Halftone Effect Output
Software Mesh	1	R/W	0 1	Hardware Defines Field Number Software Defined Field Number
Mesh Enable	0	R/W	0 1	Mesh is Disabled Mesh is Enabled

When working with Progressive mode, mesh does not work the same way as in Interlace mode.

Bit 7, Halftone Output Delay on P20, is the amount of time that output of the halftone signal is delayed to compensate for the amount of delay of OSD RGB from external circuitries.

Bits 6, 5, and 4, Mesh Color, define the color of the mesh window. The colors are specified in Blue, Green, Red order, as shown in Table 17.

5.5 Inter-Row Spacing

Inter-Row Spacing can be from 0 to 15 horizontal scan line (HL). A setting of 0 HL is called Continuous Row Display. A horizontal interrupt is generated at the start of each row. Software must program the spacing between the current row and the next row during the current horizontal interrrupt.

The time required to process a row must not exceed the display time of the row. Refer to Table 20.

Table 20 Row Space Register 04h: BankA (ROW_SPACE)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate

Bit/ Field	Bit Position	R/W	Value	Description
Fade On/Off	7	R/W	0 1	Fade feature disabled Fade feature enabled
Fade Direction	6	R/W	0 1	Fade area below the defined fade position Fade area above the defined fade position
Halftone Effect Output Delay On P20	5, 4	R/W		Works with bit 7 in MC_Reg
Inter-Row Space	3, 2, 1, 0	R/W		Inter row spacing

Bit 7, Fade ON/OFF, disables or enables the fade effect.

Bit 6, Fade Direction, controls the direction of the fade effect. When Fade Direction is set to 0, the bottom of the TV screen is faded out. Fading occurs beginning with the row number set in FADE_POS1 (3,2,1,0) and the scan line number set in FADE_POS2 (4,3,2,1,0). When the Fade Direction is set to 1, the top of the screen is faded out.

Bits 5 and 4, Halftone Effect Delay on P20, work with MC_REG (7).
Bits 3, 2, 1, and 0, Inter-Row Space, specify the number of HL to add between displayed rows.

5.7 Character Size and Smoothing Effect

The Z90255 supports four character sizes: 1X, 2X, double width, and double height. The 2X size duplicates each pixel horizontally and vertically to reach double size. Figure 14 shows a character at 1X, 2X without smoothing, and 2X with smoothing.

Smoothing means enhancing a character to improve its appearance. This effect can be applied to 2X and double width characters, and is enabled and disabled in DISP_ATTR: 03h: Bank A (4).

Check the effect of smoothing on 2X and double width characters before finalizing OSD programming.

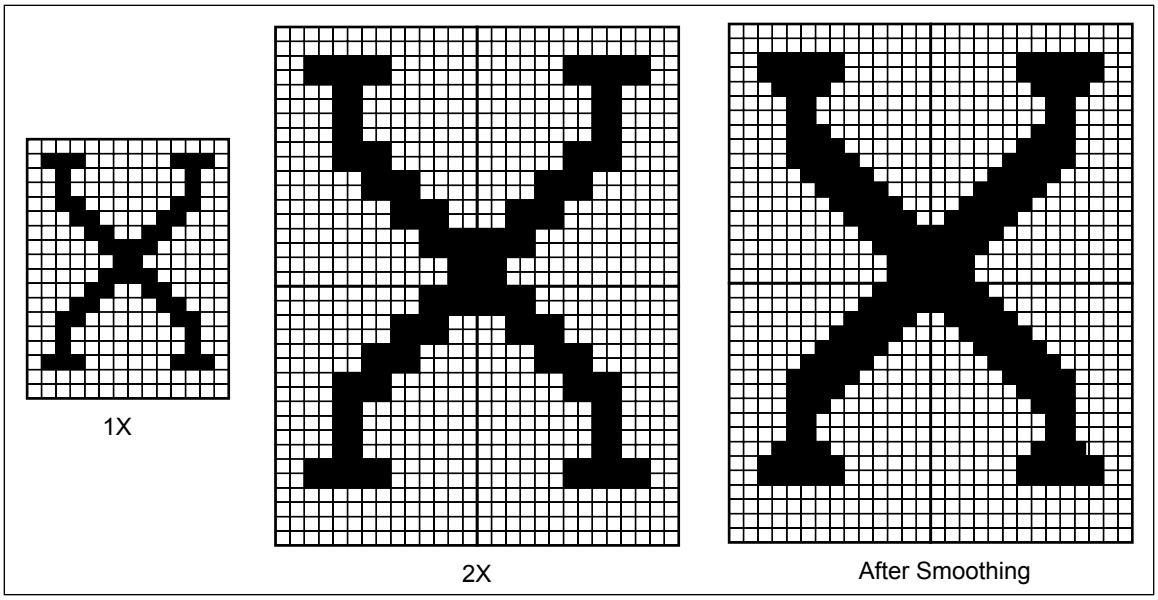

Figure 14 Smoothing Effect on 2X Character Size

Table 23 VRAM Structure and Memory Map

Character Code Data Bit[11] , Character Color C[2:0]		Character Code Data Bit[7:0]	
		Row 0 Attribute(ROW0_ATTR)	FC00h
Row0/Column 0 D[11:8]	FE01h	Row 0/Column 0 D[7:0]	FC01h
Row0/Column 1 through 22 D[11:8]	FE02h FE17h	Row 0/Column 1 through 22 D[7:0]	FC02h FC17h
Row 0/Column 23 D[11:8]	FE18h	Row 0/Column 23 D[7:0]	FC18h
		Row 1 Attribute(ROW1_ATTR)	FC20h
Row1/Column 0 D[11:8]	FE21h	Row 1/Column 0 D[7:0]	FC21h
Row1/Column 1 through 22 D[11:8]	FE22h FE37h	Row 1/Column 1 through 22 D[7:0]	FC22h FC37h
Row 1/Column 23 D[11:8]	FE38h	Row 1/Column 23 D[7:0]	FC38h
Row 2 D[11:8]	FE41h FE58h	Row 2 Video RAM buffer	FC40h FC41h FC58h
Row 3 D[11:8]	FE61h FE78h	Row 3 Video RAM buffer	FC60h FC61h FC78h
Row 4 D[11:8]	FE81h FE98h	Row 4 Video RAM buffer	FC80h FC81h FC98h
Row 5 D[11:8]	FEA1h FEB8h	Row 5 Video RAM buffer	FCA0h FCA1h FCB8h

Table 35 Master I²C Control Register 0Ch: Bank C (I²C_CNTL)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	0	0	x	x	x	x

Note: R = Read W = Write X = Indeterminate

Bit/ Field	Bit Position	R/W	Value	Description
Clock Selection	7	R/W	0 1	1X SCLK for I²C and ADC 0.5X SCLK for I²C and ADC
Reserved	6	R W		Return 1 No Effect
I²C Selection 1	5	R/W	0 1	P26 selection - POR P27 selection - POR SCLK1 selection on P26 SDATA1 selection on P27
I²C Selection 0	4	R/W	0 1	P24 selection - POR P25 selection - POR SCLK 0 selection on P24 SDATA0 selection on P25
Reserved	3	R/W		Must be 0
I²C Enable	2	R/W	0 1	Disable I²C Interface Enable I²C Interface
I²C Speed (for 6-MHz XTAL)	1, 0	R/W	00 01 10 11	10 KHz 50 KHz 100 KHz 330 KHz

If bits 4 and 5 both equal 1, then the I²C Selection 0 prevails.

Controlling the I²C Interface

Software controls the I²C module by writing appropriate commands into the I²C Command Register (I²C_CMD:0Bh:0Ch). See Table 36.

Table 40 Port 2 Mode Register F6h: P2M

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W
Reset	1	1	1	1	1	1	1	1

Note: R = Read W = Write X = Indeterminate

Bit/ Field	Bit Position	R/W	Value	Description
P27 I/O Definition	7	W	0 1	Defines P27 as Output Defines P27 as Input
P26 I/O Definition	6	W	0 1	Defines P26 as Output Defines P26 as Input
P25 I/O Definition	5	W	0 1	Defines P25 as Output Defines P25 as Input
P24 I/O Definition	4	W	0 1	Defines P24 as Output Defines P24 as Input
P23 I/O Definition	3	W	0 1	Defines P23 as Output Defines P23 as Input
P22 I/O Definition	2	W	0 1	Defines P22 as Output Defines P22 as Input
P21 I/O Definition	1	W	0 1	Defines P21 as Output Defines P21 as Input
P20 I/O Definition	0	W	0 1	Defines P20 as Output Defines P20 as Input

When P27/P26 or P25/P24 are used as I^2C pins, then these pins are automatically set to open-drain mode.

Table 41 Port 2 Data Register 02h: P2

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Note: R = Read W = Write X = Indeterminate

Bit/ Field	Bit Position	R/W	Value	Description
P27	7	R W		Data input on P27 Data Output on P27
P26	6	R W		Data input on P26 Data Output on P26
P25	5	R W		Data input on P25 Data Output on P25
P24	4	R W		Data input on P24 Data Output on P24
P23	3	R W		Data input on P23 Data Output on P23
P22	2	R W		Data input on P22 Data Output on P22
P21	1	R W		Data input on P21 Data Output on P21
P20	0	R W		Data input on P20 Data Output on P20

7.1 Port 4 Pin-Out Selection Register

Bits 5, 4, 3, and 2 control the configuration of multiplexed pins 20, 19, 18, and 17. If a bit is set to 0, the pin functions as a PWM output port. If a bit is set to 1, the pin functions as a programmable regular input/output port. See Table 42. This value is the default following a Power-On Reset.

Table 42 Port 4 Pin-Out Selection Register 08h: Bank C (PIN_SLT)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	1	1	1	1	x	x

Note: R = Read W = Write X = Indeterminate

Bit/ Field	Bit Position	R/W	Value	Description
P62 I/O definition	2	R/W	0 1	Data Output Data Input - POR
P61 I/O definition	1	R/W	0 1	Data Output Data Input - POR
P60 I/O definition	0	R/W	0 1	Data Output Data Input - POR

8 Infrared Interface

The Z90255 supports the Infrared (IR) Remote Control interface with a minimum of software overhead.

Two bytes of data are received through the Infrared (IR) Interface. The lower byte, bits 7-0, is stored in IR Capture Register 0. The upper byte, bits 15-8, is stored in IR Capture Register 1.

When an IR interrupt occurs, the IR capture registers contain the amount of time passed from the previous IR interrupt if bit 0 in the TCR0 is set to 0. If bit 0 is set to 1, the IR capture registers contain the amount of time passed from the last overflow of the IR capture counter. The IR interrupt flags are reset by the IR interrupt service routine software. Refer to Table 50 through Table 53.

Timer Control Register 0

Rising edge (falling edge) interrupt is preserved even when a falling edge (rising edge) interrupt occurs. But it is overridden by a second rising edge (falling edge) if the second one occurs before the first rising edge (falling edge) is serviced. Preservation of the interrupt means that it generates the hardware interrupt after the first interrupt is serviced when two different (rising edge/falling edge) interrupts are already ON.

Table 50 Timer Control Register 0 01h: Bank C (TCR0)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Note: R = Read W = Write X = Indeterminate

Bit/ Field	Bit Position	R/W	Value	Description
Reserved	7, 6, 5, 4, 3	R		Return 0
		W		No Effect
CAPint_r	2	R	0	No Rising Edge is Captured
			1	Rising Edge is Captured
		W	0	No Effect
			1	Reset Flag
CAPint_f	1	R	0	No Falling Edge is Captured
			1	Falling Edge is Captured
		W	0	No Effect
			1	Reset Flag
Tout_CAP	0	R	0	No Time-out of the Capture Timer
			1	Time-out of the Capture Timer
		W	0	No Effect
			1	Reset Flag

During the interrupt service routine, software must read the contents of Timer Control Register 0. Then it checks which bit is set to 1, indicating the type of edge which generated the interrupt.

Table 51 Timer Control Register 1 02h: Bank C (TCR1)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	1	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate

Bit/ Field	Bit Position	R/W	Value	Description
Reserved	7	R		Return 0
		W		No Effect
CAP Halt	6	R/W	0	Capture Timer Running
			1	Capture Timer Halted
CAP Edge	5, 4	R/W	00	No capture
			01	Capture on Rising Edge Only
			10	Capture on Falling Edge Only
			11	Capture on Both Edges

Bit/ Field	Bit Position	R/W	Value	Description
6-bit/14-bit PWM6	7	R/W	0 1	Select 6-bit (POR) Select 14-bit
PWM 11 / P56	6	R/W	0 1	Select PWM 11 Select P56 - POR
PWM 6* / P55	5	R/W	0 1	Select PWM 6 Select P55 - POR
PWM 5 / P54	4	R/W	0 1	Select PWM 5 Select P54 - POR
PWM 4 / P53	3	R/W	0 1	Select PWM 4 Select P53 - POR
PWM 3 / P52	2	R/W	0 1	Select PWM 3 Select P52 - POR
PWM 2 / P51	1	R/W	0 1	Select PWM 2 Select P51 - POR
PWM 1 / P50	0	R/W	0 1	Select PWM 1 Select P50 - POR

Note: PWM6 can be either 6- or 14-bit depending on the bit status in bit7.

Port 4 Pin-Out Selection Register

Bits 5, 4, 3, and 2 of the Port 4 Pin-Out Selection Register (Table 55) control the configuration of multiplexed pins 20, 19, 18, and 17. If a bit is reset to 0, the pin functions as a PWM output port. This value is the default following a Power-On Reset. If a bit is set to 1, the pin functions as a programmable regular input/output port.

Table 55 Port 4 Pin-Out Selection Register 08h: Bank C (PIN_SLT)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	1	1	1	1	x	x

Note: R = Read W = Write X = Indeterminate

Table 70 3-Bit ADC Data Register 00h: Bank C (3ADC_DTA)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	0	0	0	0	x	x	x

Note: R = Read W = Write X = Indeterminate

Bit/Field	Bit Position	R/W	Value	Description
Reserved	7	R W		Return 1 No effect
ADC Speed	6, 5	R/W	00 01 10 11	No ADC - POR SCLK/2 SCLK/3 SCLK/4
ADC Input Selection	4, 3	R/W	00 01 10 11	Select ADC0 - POR Select ADC 1 Select ADC 2 Select ADC 3
ADC Data	2, 1, 0	R/W		Digitized data from selected ADC input

Table 71 4-Bit ADC Data Register 01h: Bank F (4ADC_DTA)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	x	x	x	x

Note: R = Read W = Write X = Indeterminate

Bit/Field	Bit Position	R/W	Value	Description
ADC Speed	7, 6	R/W	00 01 10 11	No ADC - POR SCLK/2 SCLK/3 SCLK/4
ADC Input Selection	5, 4	R/W	00 01 10 11	Select ADC0 - POR Select ADC 1 Select ADC 2 Select ADC 3
ADC Data	3, 2, 1, 0	R/W		Digitized data from selected ADC input

P41 must be set to input mode to select ADC1.

11.3 AC Characteristics

The numbers in Table 74 correspond to the numbered signal segments in Figure 22.

Table 74 AC Characteristics

No.	Symbol	Parameter	Min	Max	Unit
1	TpC	Input Clock Period	166	1000	ns
2	T_RC, T_FC	Clock Input Rise And Fall Time		25	ns
3	T_WC	Input Clock Width	35		ns
4	$T_WHsync_{IN}L$	Hsync Input Low Width	70		ns
5	$T_WHsync_{IN}H$	Hsync Input High Width	3TpC		
6	$TpHsync_{IN}$	Hsync Input Period	8TpC		
7	T_RHsync_{IN}, T_FHsync_{IN}	Hsync Input Rise Fall Time		100	ns
8	T_WIL	Interrupt Request Input Low	70		ns
9	T_WIH	Interrupt Request Input High	3TpC		
10	T_DPOR	Power-On Reset Delay	25	100	ms
11	$T_DLVIRES$	Low Voltage Detect To Internal Reset Condition	200		ns
12	T_WRES	Reset Minimum Width	5TpC		
13	T_DH_SOI	H_{sync} Start To OSDX2 Stop	2TpV	3TpV	
14	T_DH_SOH	H_{sync} Start To OSDX2 Start		1TpV	