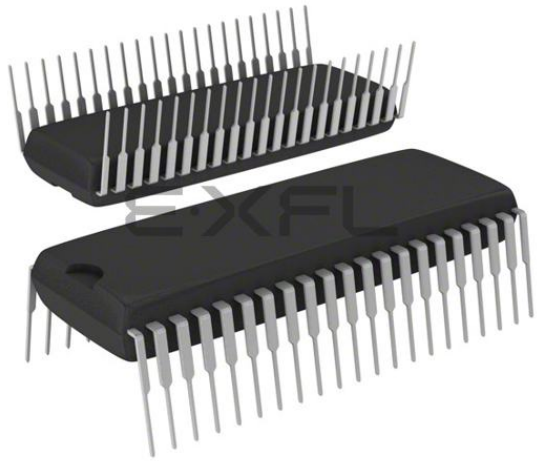

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Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	TV Controller
Core Processor	Z8
Program Memory Type	OTP (32kB)
Controller Series	Digital Television Controller (DTC)
RAM Size	300 x 8
Interface	I²C, 2-Wire Serial
Number of I/O	27
Voltage - Supply	4.5V ~ 5.5V
Operating Temperature	0°C ~ 70°C
Mounting Type	Through Hole
Package / Case	42-DIP (0.600", 15.24mm)
Supplier Device Package	42-SDIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z9025106psg

Table 4 Register File Map

BANK 4		BANK 5		BANK 6		BANK 7	
Address	**Description**	**Address**	**Description**	**Address**	**Description**	**Address**	**Description**
00h-0Fh	Gen. Pur. Reg.	00h-0Fh	Gen. Pur. Reg.	00h-0Fh	Gen. Pur. Reg.	00h-0Fh	Gen. Pur. Reg.

BANK A		BANK B	
Address	**Description**	**Address**	**Description**
00h	OSD Control Register(OSD_CNTL)	00h	PWM11-High Data Register(PWM11H)
01h	Vertical Position Register(VERT_POS)	01h	PWM11-Low Data Register(PWM11L)
02h	Horizontal Position Register(HOR_POS)	02h	PWM1 Data Register(PWM1)
03h	Display Attribute Register(DISP_ATTR)	03h	PWM2 Data Register(PWM2)
04h	Row Space Register (ROW_SPACE)	04h	PWM3 Data Register(PWM3)
05h	Fade Position1 Register(FADE_POS1)	05h	PWM4 Data Register(PWM4)
06h	Fade Position2 Regisiter(FADE_POS2)	06h	PWM5 Data Register(PWM5)
07h	Second Color Control Register(SNDCLR_CNTRL)	07h	PWM6(6-bit) Data Register(PWM6_6)
08h	Second Color Position Register(SNDCLR_POS)	08h	PWM7 Data Register(PWM7)
09h	Color Palette0 Register(CLR_P0)	09h	PWM8 Data Register(PWM8)
0Ah	Color Palette1 Register(CLR_P1)	0Ah	PWM9 Data Register(PWM9)
0Bh	Color Palette2 Register(CLR_P2)	0Bh	PWM10 Data Register(PWM10)
0Ch	Color Palette3 Register(CLR_P3)	0Ch	Port 5 Data Register(PRT5_DTA)
0Dh	Color Palette4 Register(CLR_P4)	0Dh	PWM Mode Register(P_MODE)
0Eh	Color Palette5 Register(CLR_P5)	0Eh	Port 5 Direction Register(PRT5_DRT)
0Fh	Color Palette6 Register(CLR_P6)	0Fh	

BANK C		BANK F	
Address	**Description**	**Address**	**Description**
00h	3-bit ADC Data Register(3ADC_DTA)	00h	Port Configuration Register(PCON)
01h	Timer Control Register0(TCR0)	01h	4-bit ADC Data Register (4ADC_DTA)
02h	Timer Control Register1(TCR1)	02h	Port6 Direction Register(PRT6_DRT)
03h	IR Capture Register0(IR_CP0)	03h	Port6 Data Register (PRT6_DTA)
04h	IR Capture Register1(IR_CP1)	04h	Mesh Column Start Register(MC_ST)
05h	Port4 Data Register(PRT4_DTA)	05h	Mesh Column End Register(MC_END)
06h	Port4 Direction Register(PRT4_DRT)	06h	Mesh Row Enable Register(MR_EN)
07h	Interrupt Status Register(INT_ST)	07h	Mesh Control Register(MC_REG)
08h	Port4 Pin_out Selection Register(PIN_SLT)	08h	PWM6 High Data Register(PWM6H_14)
09h	Color Index Register(CLR_IDX)	09h	PWM6 Low Data Register (PWM6L_14)
0Ah	I2C Data Register(I^2C_DATA)	0Ah	
0Bh	I2C Command Register(I^2C_CMD)	0Bh	Stop Mode Register(SMR)
0Ch	I2C Control Register(I^2C_CNTL)	0Ch	
0Dh		0Dh	
0Eh		0Eh	
0Fh		0Fh	WDT Mode Register(WDTMR)

3 Watch-Dog Timer (WDT)

The Watch-Dog Timer (WDT) is driven by an internal RC oscillator. Therefore accuracy is dependent on the tolerance of the RC components. Table 5 describes the Watch-Dog Timer Mode register bits.

Table 5 Watch-Dog Timer Mode Register 0Fh: Bank F

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	1	0	1

Note: R = Read W = Write X = Indeterminate

Bit/ Field	Bit Position	R/W	Value	Description
reserved	7-4	W	0	Must be 0
WDT During Stop	3	W	0 1	Off On POR
WDT During Halt	2	W	0 1	Off On POR
WDT TAP	1, 0	W	00 01 10 11	6 msec 12 msec POR 24 msec 96 msec

WDT During Halt Mode (T2)

Bit 2 determines if the WDT is active during Halt Mode. A 1 value indicates active during Halt. The default is 1. A WDT timeout during Halt Mode resets control registers and ports to their default reset conditions.

Bit 3 determines if the WDT is active during Stop mode. A 1 value indicates active during Stop mode. A WDT timeout during Stop mode resets control registers and ports to their default reset conditions.

Bits 4, 5, 6 and 7 are reserved and must be cleared to 0.

The WDTMR register is accessible only during the first 60 processor cycles from the execution of the first instruction after Power-On Reset, Watch-Dog Reset, or a

Note: Stop-Mode Recovery (SMR) by the WDT increases the Stop Mode standby current (ICC2). This is because the internal RC oscillator is running to support this recovery mode.

The Z90255 and Z90251 have Stop-Mode Recovery (SMR) circuitry. Two SMR methods are implemented, a single-fixed input pin or a flexible, programmable set of inputs. The Z8-base product specification should be reviewed to determine the SMR options available.

In simple cases, a Low level applied to input pin P27 triggers an SMR. To use this mode, pin P27 (I/O Port 2, bit 7) must be configured as an input before entering Stop Mode. The Low level on P27 must meet a minimum pulse width TWSM. Some microcontrollers provide multiple SMR input sources. The SMR source is selected via the SMR Register.

Note: Using specialized SMR modes (P27 input or SMR register based) or the WDT timeout (only when in the Stop Mode) provides a unique reset operation. Some control registers are initialized differently for a SMR/WDT triggered POR than a standard reset operation.

Note: The Stop Mode current (ICC2) is minimized when

- V_{CC} is at the low end of the device operating range
- WDT is Off in Stop Mode
- Output current sourcing is minimized
- All inputs (digital and analog) are at the low or high rail voltages

4.3 STOP Mode Recovery Register

The STOP Mode Recovery Register register selects the clock divide value and determines the mode of Stop Mode Recovery. All bits are Write-Only, except bit 7 which is Read-Only. Bit 7 is a flag bit that is hardware set in a Stop Mode Recovery condition, and reset by a power-on cycle. Bit 6 controls whether a Low level or a High level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4, of the SMR register, specify the source of the Stop-Mode Recovery signal. Bits 0 and 1 control internal clock divider circuitry. The SMR is located in bank F of the expanded register file at address 0Bh.

Table 6 contains Stop Mode Recovery (SMR) Register bit descriptions.

5 On-Screen Display

The On-Screen Display (OSD) module generates and displays a 10 row by 24 columns of 512 characters at 14 x 18-dots resolution. The color of each character can be specified independently.

The televison OSD controller uses H_{SYNC} and V_{SYNC} signals to synchronize its internal circuitry to the video signal, then outputs RGB and Video Blank (VBLANK) signals. The VBLANK signal is used to multiplex the OSD signal and video signal onto the screen. The result is that the On-Screen Display is superimposed over the TV picture.

The display results from the successful timing of several components:

- OSD Positioning
- Second Color Feature
- Mesh and Halftone Effect
- OSD Fade
- Inter-Row Spacing
- Character Generation

5.1 OSD Position

OSD Positioning is controlled by programming the following registers:

- OSD Control Register (Table 8)
- Vertical Position Register (Table 9)
- Horizontal Position Register (Table 10)

OSD Control Register

Table 8 OSD Control Register 00h:Bank A (OSD_CNTL)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	x	x	x	x	x	x	x

Note: R = Read W = Write X = Indeterminate

Vertical Position Register

The Vertical Position Register (Table 6) sets the vertical placement of the OSD on the screen. The unit of measure for placement is the number of scan lines from the top of the TV field.

Table 9 Vertical Position Register 01h:Bank A (VERT_POS)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate

Bit/ Field	Bit Position	R/W	Value	Description
reserved	7	R W	0 1	Return 0 No effect
Character double height	6	R/W	0 1	Normal when bit 3 of OSD_CNTL is 0. 2X when bit 3 of OSD_CNTL is 1. Double height when bit 3 of OSD_CNTL is 0. Double width when bit 3 of OSD_CNTL is 1.
Vertical Position	5,4,3,2,1,0	R/W		Vertical position control

The value required for this register can be computed using the following equation:

$$VERT\_POS = (V_{POS} - 6) / 4$$

VERT_POS represents the contents of bits 5,4,3,2,1,0 of the Vertical Position Register (VERT_POS). The default value is 0. When the value is 0, the OSD is at the top-most OSD position on the screen, with an offset of 06h scan lines above the OSD area.

VERT_POS is the number of scan lines from the V_{SYNC} to the OSD start position. V_{POS} must be a positive integer with a minimum value of Ah incrementing by 4.

Bit/ Field	Bit Position	R/W	Value	Description
Reserved	7	R W	0 1	Return 1 No effect
HV_{SYNC} Interrupt Option	6	R/W	0 1	Interrupt Pending Disabled Interrupt Pending Enabled
Second Color Position	5,4,3,2,1,0	R/W		Specifies start position of the color change to the second color.

Note: Column increment is 0.5. Offset is 03h. System software requires that the offset be added to the increment for the second color in the bar display. The bar position must be defined before the second color is enabled.

Bit 6, HV_{SYNC} Interrupt Option, defines the procedure for processing when a second interrupt is issued before the first interrupt has completed processing. If bit 6 is set to 0, bit 6 is not pending the other interrupt (H_{SYNC} or V_{SYNC}) while one is in service. If bit 6 is set to 1, bit 6 is pending the other interrupt (H_{SYNC} or V_{SYNC}) while one is in service.

Figures 9 is an example of second color display in the eighth row of the OSD. Each of the small grid squares represents one pixel. Each column has two areas for second color display. In this example, the second color is at Position 6. The second color position for the first column has a value of 3 because the OSD is offset from the left of the TV screen at a distance equal to 03h. Each column is the size of one display character. Each Second color column is a half character column. The screen position offset is added to Second color position. Because the offset is 03h, the Second color postions begin with 3 = (3+0), 4 = (3+1), 5 = (4+1), and so forth.

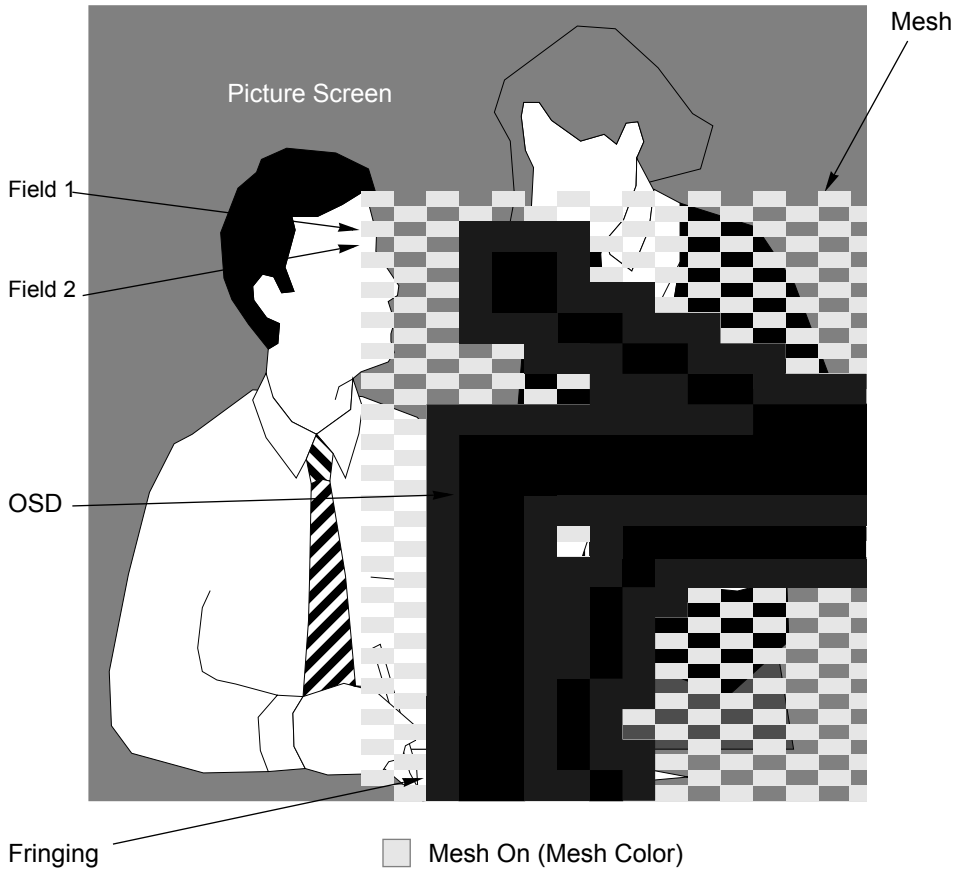


Figure 10 Mesh On

General descriptions of the registers used to control the mesh are contained in Tables 13 through 16.

Table 13 Mesh Column Start Register 04h: Bank F (MC_St)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate

Bit/ Field	Bit Position	R/W	Value	Description
V_{BLANK} Delay	7, 6, 5, 4	R/W	0000	No Delay
			0001	Delay by 0.5 Dot-Clock Period
			0010	Delay by 1.0 Dot-Clock Period
			0011	Delay by 1.5 Dot-Clock Period
			0100	Delay by 2.0 Dot-Clock Period
			0101	Delay by 2.5 Dot-Clock Period
			0110	Delay by 3.0 Dot-Clock Period
			0111	Delay by 3.5 Dot-Clock Period
			1000	Delay by 4.0 Dot-Clock Period
			1001	Delay by 4.5 Dot-Clock Period
			1010	Delay by 5.0 Dot-Clock Period
			1011	Delay by 5.5 Dot-Clock Period
			1100	Delay by 6.0 Dot-Clock Period
			1101	Delay by 6.5 Dot-Clock Period
			1110	Delay by 7.0 Dot-Clock Period
			1111	Delay by 7.5 Dot-Clock Period
Foreground Character for Halftone Effect	3	R/W	0	Not included
			1	Included
Reserved	2, 1	R/W		Must be 0
Mesh Window Row	0	R/W	0	No mesh OSD for Next Row
			1	Mesh OSD for Next Row

Bits 7, 6, 5, and 4, VBLANK Delay, set the amount of time that the VBLANK signal is properly aligned with the OSD RGB output with delay from external circuitries.

Bit 3, Character Foreground for Halftone Effect, defines whether displaying a foreground color for character display is included. If bit 3 is set to 0, halftone is disabled for pixels with foreground color. If bit 3 is set to 1, halftone is active for pixels with both foreground and background colors.

Bit 0, Mesh Window Row, sets the mesh effect to On or Off for the next row of the OSD.

Table 16 Mesh Control Register 07h: Bank F (MC_Reg)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate

Bit/ Field	Bit Position	R/W	Value	Description
Halftone Effect Output Delay on P20	7	R/W	xx/x 00/0 00/1 01/0 01/1 10/0 10/1 11/0 11/1	Bits 5, 4 in ROW_SPACE/ bit 7 No Delay Delay by 0.5 Dot-Clock Period Delay by 1.0 Dot-Clock Period Delay by 1.5 Dot-Clock Period Delay by 2.0 Dot-Clock Period Delay by 2.5 Dot-Clock Period Delay by 3.0 Dot-Clock Period Delay by 3.5 Dot-Clock Period
Mesh Color	6, 5, 4	R/W		Defines the mesh color. B,G,R respectively.
P20 for Halftoning	3	R/W	0 1	Normal Mesh effect Use P20 Output for Halftoning
Software Field Number/ Polarity of Halftone Effect Output	2	R/W	0 1	Even Field/Positive Halftone Effect Output Odd Field/Negative Halftone Effect Output
Software Mesh	1	R/W	0 1	Hardware Defines Field Number Software Defined Field Number
Mesh Enable	0	R/W	0 1	Mesh is Disabled Mesh is Enabled

When working with Progressive mode, mesh does not work the same way as in Interlace mode.

Bit 7, Halftone Output Delay on P20, is the amount of time that output of the halftone signal is delayed to compensate for the amount of delay of OSD RGB from external circuitries.

Bits 6, 5, and 4, Mesh Color, define the color of the mesh window. The colors are specified in Blue, Green, Red order, as shown in Table 17.

Table 18 Fade Position Register 1 05h: Bank A (FADE_POS1)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	0	0	0	0

Note: R = Read W = Write X = Indeterminate

Bit/ Field	Bit Position	R/W	Value	Description
Reserved	7, 6, 5, 4	R W		Return 1 No effect
Row Number of the Screen	3, 2, 1, 0	R/W		OSD Row number for fading

Bits 3, 2, 1, and 0 define the boundary row for the fade area. The portion of the OSD above or below the row number fades up or down, as set in Fade Direction, ROW_SPACE(6).

The fade starts at the scan line set in FADE_POS2 (4,3,2,1,0) within the row number set in FADE_POS1 (3,2,1,0).

Table 19 Fade Position Register 2 06h: Bank A (FADE_POS2)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate

Bit/ Field	Bit Position	R/W	Value	Description
Reserved	7, 6, 5	R W		Return 1 No effect
Scan Line Number	4, 3, 2, 1, 0	R/W		Scan Line Number of a row

The Hex Add column is a hexadecimal number that serves as an address for the group of pixels from the starting point of the scan line. Addressing begins at 0000h and ends at 0023h for the first character. There is an address gap between characters. The starting address for the second character is 0040h.

Each bit in the map sets the foreground/background designation of the corresponding pixel:

0 background pixel
1 foreground pixel

The patterns formed by the bits comprise the characters that are displayed when the scan line is output to the screen.

Each of these character pixel maps is one character; 512 characters can be mapped.

Several characters can be combined to form a large icon. Figures 13 is an example of a large icon. Each block marked by the darker grid lines is 14 x 18 pixels, one character.

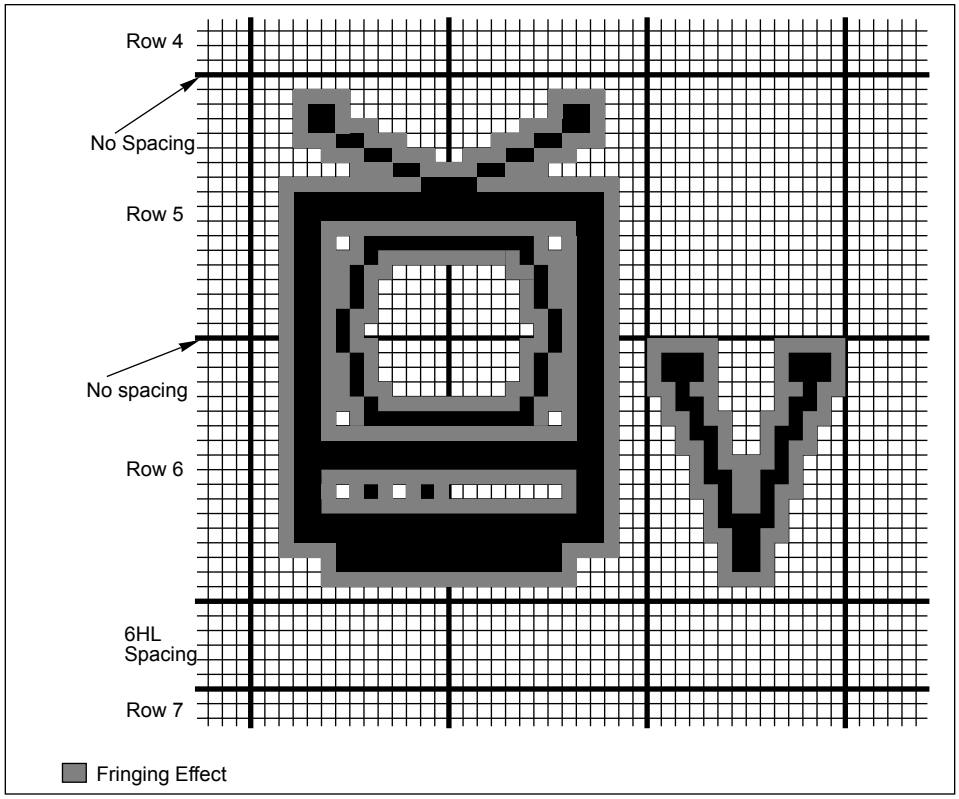


Figure 13 Example of a Multiple Character Icon

Row Attribute Register

The Row Attribute Register (Table 33) is mapped to VRAM, as shown in Table 20. This register controls row background and foreground display. If the Color Index is set to 000h, the display color is read from the Row Attribute Register.

Table 33 Row Attribute Register (ROW_ATTR)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Note: R = Read W = Write X = Indeterminate

Bit/ Field	Bit Position	R/W	Value	Description
Row Foreground Enable	7	R/W	0 1	Row Foreground Color displayed Row Foreground color disabled
Row Foreground Color	6, 5, 4	R/W		Defines the Character Color R, G, B, respectively
Row Background Enable	3	R/W	0 1	Row Background Color disabled Row Background color displayed
Row Background Color	2, 1, 0	R/W		Defines the Row Background Color R, G, B, respectively

5.10 HV Interrupt Processing

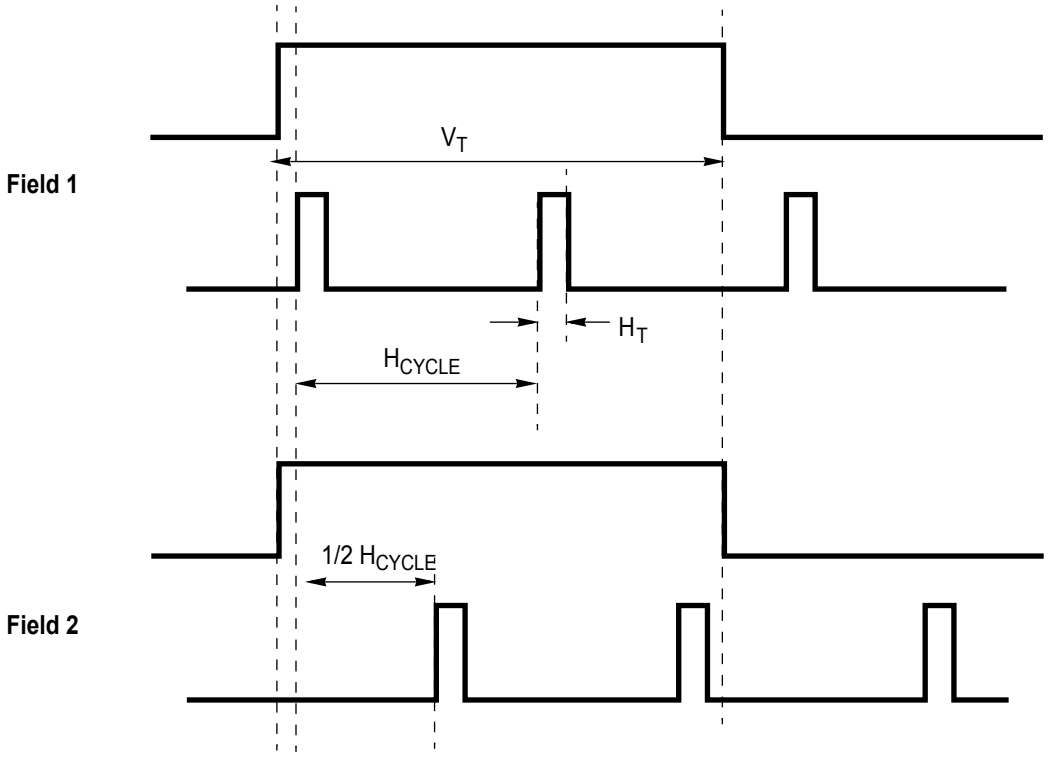
An interrupt is issued at the beginning of a row and at the leading edge of the V_{SYNC} signal. The leading edge of the first H_{SYNC} of a row constitutes the beginning of a row. The Z90255 software tracks this cycle as two recurring events, the Horizontal (H_{SYNC}) Interrupt and the Vertical (V_{SYNC}) Interrupt.

A V_{SYNC} interrupt marks the time for displaying a new field of a TV frame. Displaying subsequent rows coincides with the issuance of the H_{SYNC} interrupt. The interrupts mark the time when displaying a row or start of a field is to occur.

Each text row is comprised of 18 scan lines. Each scan line takes 63.5 µs to be displayed. So, 1143 µs is the amount of time available to change programming for the next row. Double-size and double-height characters span 36 scan lines,

H_{SYNC} and V_{SYNC} Requirements

H_{SYNC} and V_{SYNC} must meet all TV broadcasting specifications. The minimum width of V_{SYNC} must conform to the specification in Figure 16.



V_T must be larger than 1.5 x (H_{CYCLE} +H_T).
The same timing specification must applied in negative polarity.

Figure 16 H_{SYNC} and V_{SYNC} Specification

The rising edge of V_{SYNC} must not coincide with the rising edge of H_{SYNC} to be sure that the controller recognizes both rising edges.

6 Z90255 I2C Master Interface

The Z90255 has a hardware module which supports the I^2C Master interface. Bus arbitration and Masters' arbitration logic is NOT implemented; in other words, the Z90255 is designed for a **Single Master** application.

The I^2C interface can be configured to run at four different transfer speeds defined by bits (1,0) in the I^2C Control Register (I^2C_CNTL: 0Ch, Bank:C).

To circumvent possible problems on both DATA and SCLK lines, digital filters with time constant equal to $3T_{sclk}$ are implemented on all inputs of the I^2C bus interface. The Z90255 has two separate I^2C busses which share the same I^2C state machine.

The I^2C module is enabled by setting bit (2) in the I2C_CNTL register to 1(see Figure 17). This bit blocks out I^2C logic if it is set to 0. To prevent switching the I^2C bus during activation, bits (7,6) of the Port 2 Data Register for I^2C selection 1 (bits (5,4) of Port 2 Data Register for I^2C selection 0) should be set to 1 before the I^2C module is enabled.

Notes: 1 When the I^2C module is enabled, pins used as I^2C must be configured as output in the Port 2 Mode Register (P2M: F6h). If P27/P26 or P25/P24 are used as I^2C pins, then these pins are automatically set to open-drain mode.

2 Port 2 must be configured in standard drive mode (PCON: 00h: Bank F) when the I^2C interface is active.

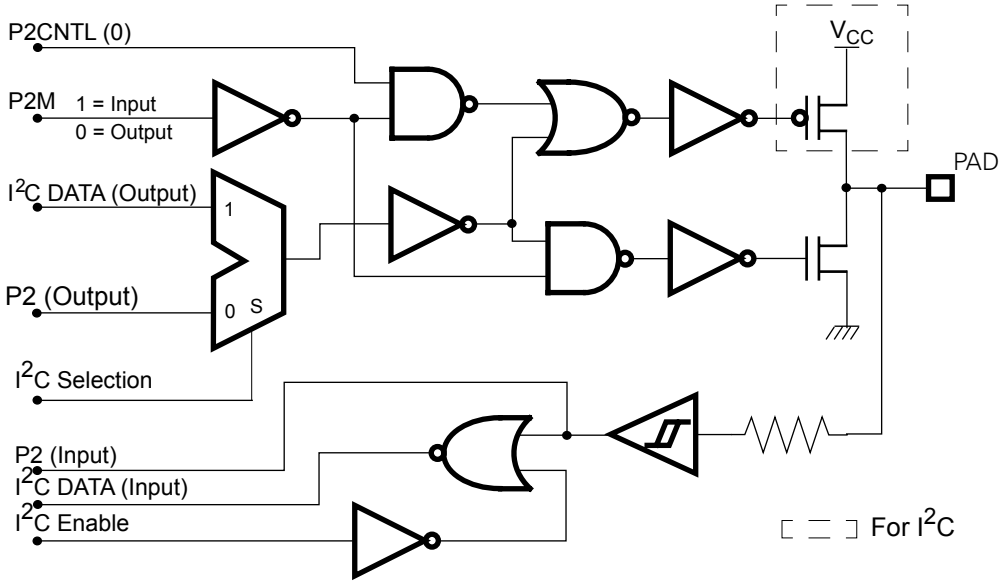


Figure 17 Bidirectional Port Pin Pad Multiplexed with I2C Port

Table 38 Master I^2C Bus Interface Commands

Command	Description
000	Send a Start bit followed by the address byte specified in the I^2C data register, then fetch the acknowledgment bit in I^2C_DATA (0). Used to initialize communication. Nine SCLK cycles are generated.
001	Send the byte of data specified in the I^2C data register, then fetch an acknowledgment bit stored in bit 0. Used in a Write frame. Nine SCLK cycles are generated.
010	Send bit 7 of I^2C_DATA register as an acknowledgment bit (ACK: (0XXXXXXX), NAK: (1XXXXXXX)), then receive a data byte. Used in a Read frame when the next data byte is expected. Nine SCLK cycles are generated. Received data is read in the I^2C data register.
011	Send bit 7 of I^2C_DATA register as an acknowledgment bit (ACK: (0XXXXXXX), NAK: (1XXXXXXX). Used in a Read frame. One SCLK cycle is generated.
10X	Null operation. Must be used with a Reset bit.
110	Received one data byte. Used in a Read frame to receive the first data byte after an address byte is transmitted. Eight SCLK cycles are generated.
111	Send Stop bit. One SCLK cycle is generated.

Table 53 IR Capture Register 1 04h: Bank C (IR_CP1)

Bit	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate

Bit/ Field	Bit Position	R/W	Value	Description
IR Capture Register 1	7,6,5,4,3,2,1,0	R		Reading High Byte of IR Capture Data

9 Pulse Width Modulators

The Z90255 has 11 Pulse Width Modulator channels. PWM1 through PWM10 have 6-bit resolution and are typically used for audio and video level control. PWM11 has 14-bit resolution and is typically used for voltage synthesis tuning. PWM11 uses two registers to accommodate its 14-bit resolution. PWM6 can be configured as either 14-bit or 6-bit.

9.1 PWM Mode Register

PWM Mode Register (Table 54) controls the setting of multiplexed pins 1-7. These pins can be configured to function as PWM output ports or regular output ports. If a bit is reset to 0, the pin outputs the PWM signal. If a bit is set to 1, the pin is a regular output port.

Table 54 PWM Mode Register 0Dh: Bank B (P_MODE)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	1	1	1	1	1	1

Note: R = Read W = Write X = Indeterminate

Figure 18 and Figure 19 illustrate various timing pulses and resultant frequencies for the 6-bit and 14-bit PWMs.

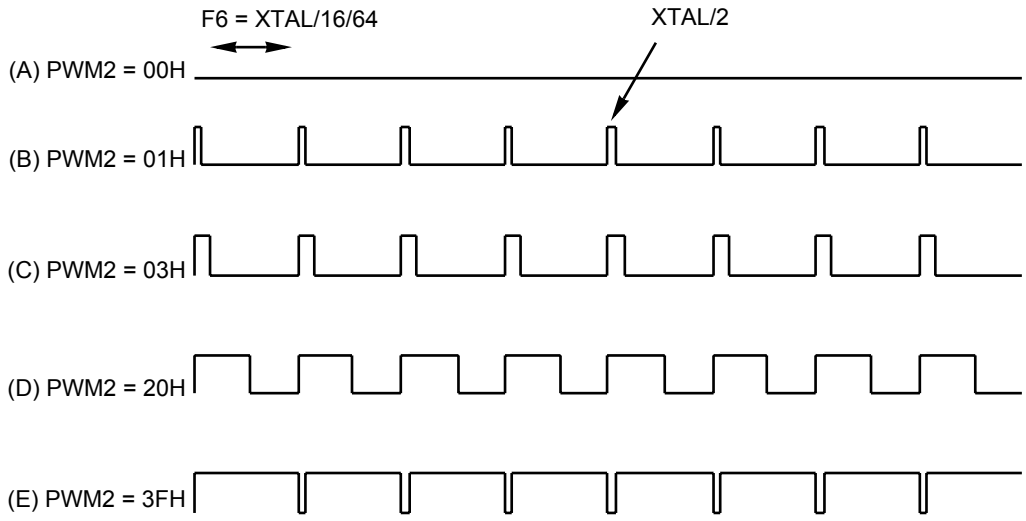


Figure 18 Pulse Width Modulator Timing Diagram, 6 Bit

9.3 Digital/Analog Conversion with PWM

The televison OSD controller can generate square waves which have fixed periods but variable duty cycles. If this type of signal passes through an RC integrator, the output is a DC voltage proportional to the pulse width of the square wave. Refer to Figure 20, Cases A and B show fixed voltage samples while Case C shows a varying voltage example.

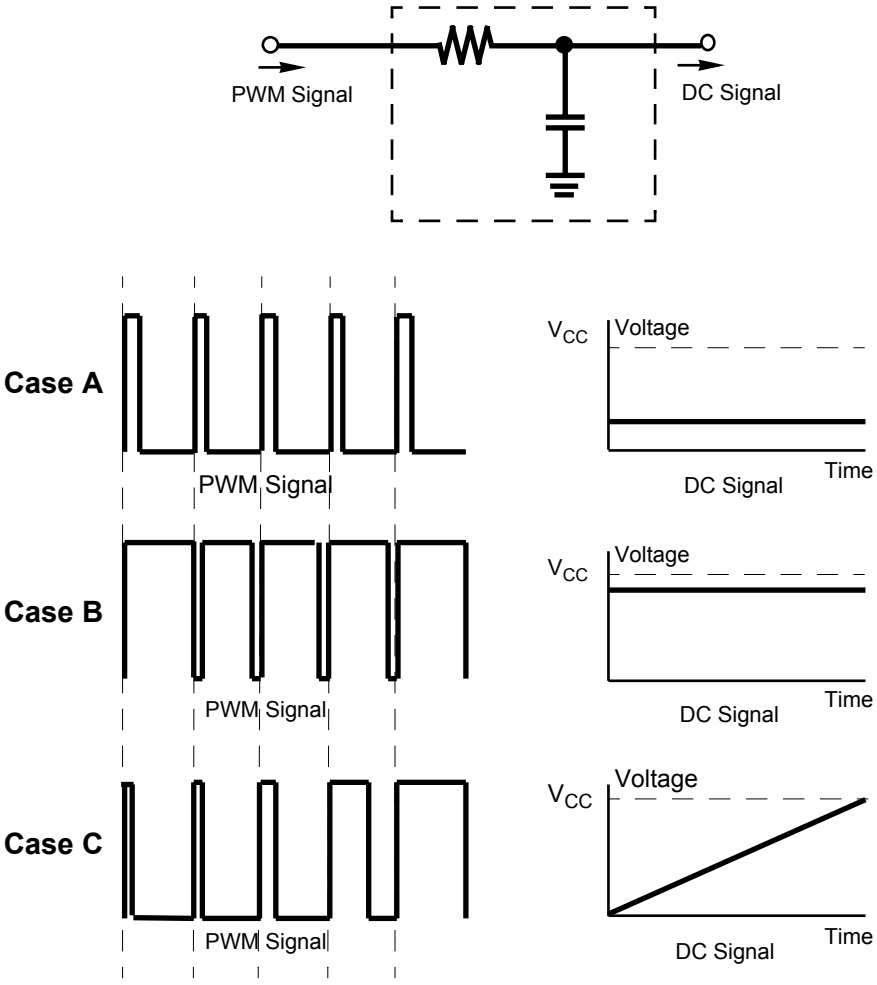


Figure 20 Analog Signals Generated from PWM Signals

10 Analog-to-Digital Converter

The Z90255 is equipped with a 4-bit flash analog-to-digital converter (ADC) that can be used as either three or four bit configurations. There are four multiplexed analog-input channels. There are two register addresses, one for 3-bit (Table 70) ADC (3ADC_DTA: 00h: Bank C), and one for 4-bit (Table 71) ADC (4ADC_DTA: 01h: Bank F). Because no default is set, system software must configure the control register for the preferred ADC.

Converted 3-bit data is available as bits 0, 1, and 2 of the 3-bit ADC data register.

Converted 4-bit data is available as bits 0, 1, 2, and 3 of the 4-bit ADC data register.

Figure 21 illustrates four input pins (P60/ADC3, P61/ADC2, P41/ADC1, and P62/ADC0) which function as analog-input channels and as digital I/O ports. To support the analog function, the digital ports must be configured as analog through software. Analog/digital selection is controlled by bits 4 and 3 of the 3-bit ADC Data Register, and by bits 5 and 4 of 4-bit ADC Data Register.

- If ADC Input Selection equals 00, ADC0 is selected; this value is the default following POR.
- If ADC Input Selection equals 01, ADC1 is selected.
- If ADC Input Selection equals 10, ADC2 is selected.
- If ADC Input Selection equals 11, ADC3 is selected.

Sampling occurs at one-eighth of an ADC-clock tick. One ADC-clock tick equals one-half, one-third, or one-quarter of a system-clock (SCLK) tick, as set by 3ADC_DTA(6,5) for 3-bit or 4ADC_DTA (7,6) for 4-bit. If ADC speed bits are set to 00, the ADC is not operative; this is the default value following POR. If these bits equal 01, ADC speed is based on one-half of a system-clock tick, SCLK/2. If these bits equal 10, ADC speed is based on one-third of a system-clock tick, SCLK/3. If these bits equal 11, ADC speed is based on one-quarter of a system-clock tick, SCLK/4.