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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	20MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	6
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	10-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	10-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10y14dsp-30

○ ROM, RAM capacities

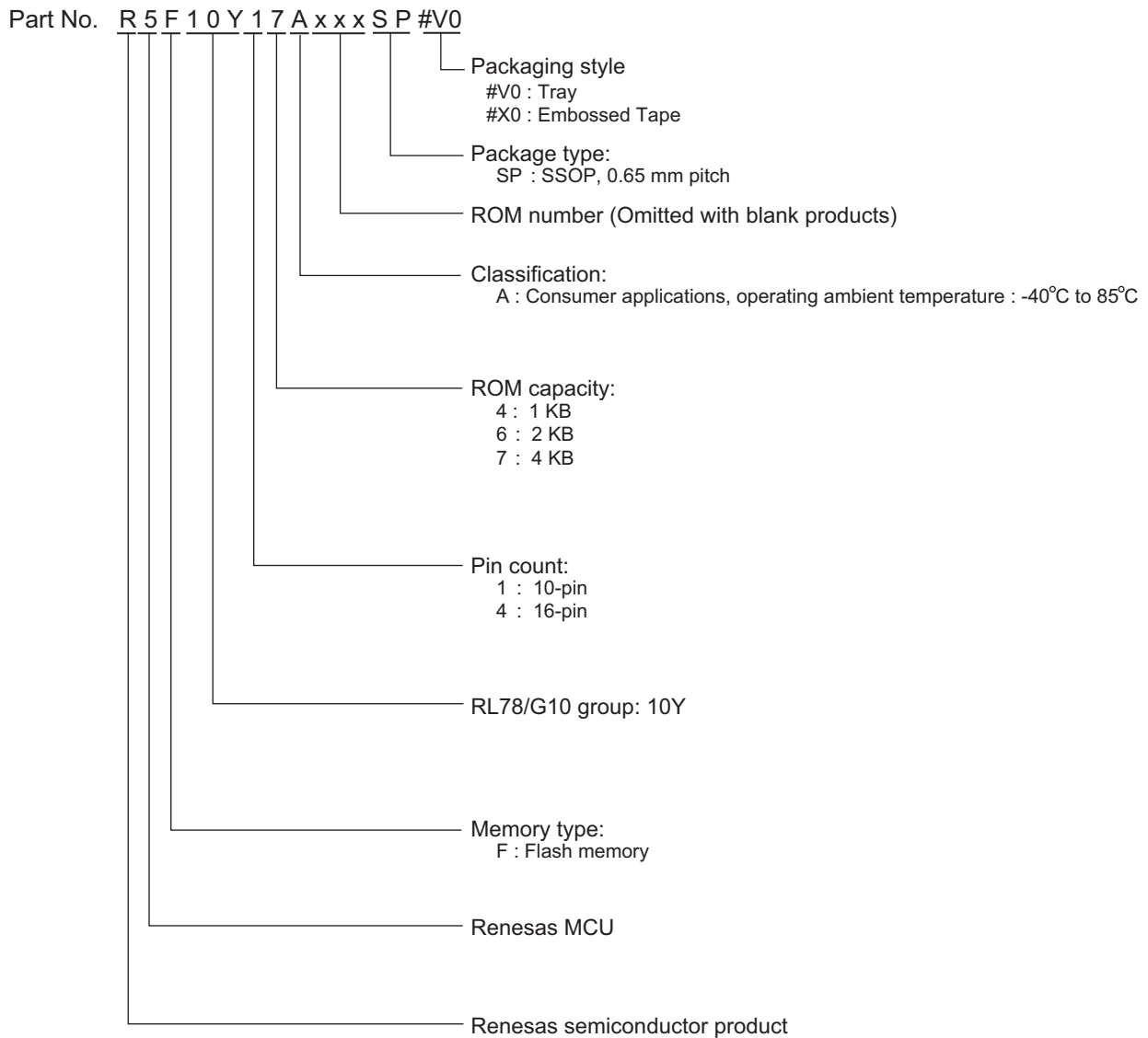
Flash ROM	RAM	10 pins	16 pins
4 KB	512 B	–	R5F10Y47ASP ^{Note 2}
2 KB	256 B	R5F10Y16ASP	R5F10Y46ASP ^{Note 2}
1 KB	128 B	R5F10Y14ASP	R5F10Y44ASP ^{Note 2}

- Notes**
1. 16-pin products only
 2. Under development

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

1.2 List of Part Number

Figure 1-1. Classification of Part Number



Pin count	Package	Part Number
10 pins	10-pin plastic LSSOP (4.4 × 3.6 mm, 0.65mmpitch)	R5F10Y16ASP#V0, R5F10Y16ASP#X0
		R5F10Y14ASP#V0, R5F10Y14ASP#X0
16 pins	16-pin plastic SSOP (4.4 × 5.0 mm, 0.65mmpitch)	R5F10Y47ASP ^{Note}
		R5F10Y46ASP ^{Note}
		R5F10Y44ASP ^{Note}

Note Under development

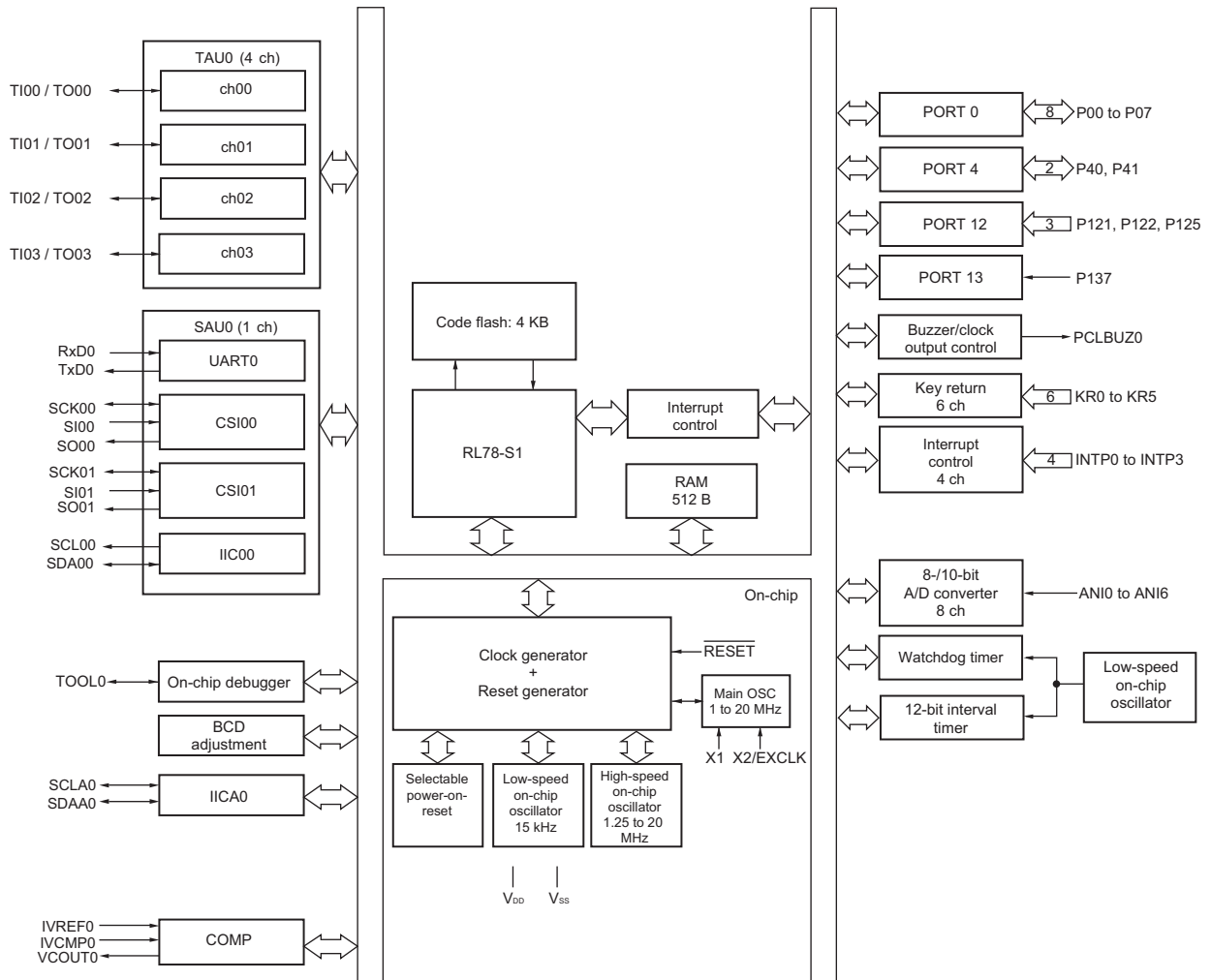
Caution The part number represents the number at the time of publication.

Be sure to review the latest part number through the target product page in the Renesas Electronics Corp.website.

1.4 Pin Identification

ANI0 to ANI6	: Analog Input
INTP0 to INTP3	: External Interrupt Input
KR0 to KR5	: Key Return
P00 to P07	: Port 0
P40, P41	: Port 4
P121, P122, P125	: Port 12
P137	: Port 13
PCLBUZ0	: Programmable Clock Output/ Buzzer Output
EXCLK	: External Clock Input
X1, X2	: Crystal Oscillator
IVCMP0	: Comparator Input
VCOUT0	: Comparator Output
IVREF0	: Comparator Reference Input
$\overline{\text{RESET}}$: Reset
RxD0	: Receive Data
SCK00, SCK01	: Serial Clock Input/Output
SCL00, SCLA0	: Serial Clock Output
SDA00, SDAA0	: Serial Data Input/Output
SI00, SI01	: Serial Data Input
SO00, SO01	: Serial Data Output
TI00 to TI03	: Timer Input
TO00 to TO03	: Timer Output
TOOL0	: Data Input/Output for Tool
TxD0	: Transmit Data
V _{DD}	: Power Supply
V _{SS}	: Ground

1.5.2 16-pin products



1.6 Outline of Functions

This outline describes the function at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

Item		10-pin		16-pin		
		R5F10Y16ASP	R5F10Y14ASP	R5F10Y47ASP	R5F10Y46ASP	R5F10Y44ASP
Code flash memory		2 KB	1 KB	4 KB	2 KB	1 KB
RAM		256 B	128 B	512 B	256 B	128 B
Main system clock	High-speed system clock	—		X1, X2 (crystal/ceramic) oscillation, external main system clock input (EXCLK): 1 to 20 MHz: V _{DD} = 2.7 to 5.5 V 1 to 5 MHz: V _{DD} = 2.0 to 5.5 V		
	High-speed on-chip oscillator clock	<ul style="list-style-type: none"> • 1.25 to 20 MHz (V_{DD} = 2.7 to 5.5 V) • 1.25 to 5 MHz (V_{DD} = 2.0 to 5.5 V) 				
Low-speed on-chip oscillator clock		15 kHz (TYP)				
General-purpose register		8-bit register × 8				
Minimum instruction execution time		0.05 μs (20 MHz operation)				
Instruction set		<ul style="list-style-type: none"> • Data transfer (8 bits) • Adder and subtractor/logical operation (8 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc. 				
I/O port	Total	8		14		
	CMOS I/O	6 (N-ch open-drain output (V _{DD} tolerance): 2)		10 (N-ch open-drain output (V _{DD} tolerance): 4)		
	CMOS input	2		4		
Timer	16-bit timer	2 channels		4 channels		
	Watchdog timer	1 channel				
	12-bit interval timer	—		1 channel		
	Timer output	2 channels (PWM output: 1)		4 channels (PWM outputs: 3 ^{Note 1})		
Clock output/buzzer output		1				
		2.44 kHz to 10 MHz: (Peripheral hardware clock: f _{MAIN} = 20 MHz operation)				
Comparator		—		1		
8-/10-bit resolution A/D converter		4 channels		8 channels		
Serial interface		[10-pin products] CSI: 1 channel/simplified I ² C: 1 channel/UART: 1 channel				
		[16-pin products] CSI: 2 channels/simplified I ² C: 1 channel/UART: 1 channel				
	I ² C bus	—		1 channel		
Vectored interrupt sources	Internal	8		14		
	External	3		5		
Key interrupt		6				
Reset		<ul style="list-style-type: none"> • Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by selectable power-on-reset • Internal reset by illegal instruction execution ^{Note 2} • Internal reset by data retention lower limit voltage 				
Selectable power-on-reset circuit		Detection voltage: 2.0 V/2.4 V/2.7 V/4.0 V				
On-chip debug function		Provided				
Power supply voltage		V _{DD} = 2.0 to 5.5 V				
Operating ambient temperature		T _A = - 40 to + 85 °C				

- Notes**
1. The number of outputs varies, depending on the setting of channels in use and the number of the master (see **6.8.3 Operation as multiple PWM output function in the RL78/G10 User's Manual**).
 2. The illegal instruction is generated when instruction code FFH is executed. Reset by the illegal instruction execution not issued by emulation with the on-chip debug emulator.

2.3 DC Characteristics

2.3.1 Pin characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	I _{OH1}	P00, P01, P02 to P04, P40	Per pin			-10.0 ^{Note 2}	mA
		P40	Total ^{Note 3}	4.0 V ≤ V _{DD} ≤ 5.5 V		-10.0	mA
				2.7 V ≤ V _{DD} < 4.0 V		-2.0	mA
				2.0 V ≤ V _{DD} < 2.7 V		-1.5	mA
		P00, P01, P02 to P04	Total ^{Note 3}	4.0 V ≤ V _{DD} ≤ 5.5 V		-50.0	mA
				2.7 V ≤ V _{DD} < 4.0 V		-10.0	mA
				2.0 V ≤ V _{DD} < 2.7 V		-7.5	mA
Total of all pins ^{Note 3}						-60.0	mA
Output current, low ^{Note 4}	I _{OL1}	P00 to P04, P40	Per pin			20.0 ^{Note 2}	mA
		P40	Total ^{Note 3}	4.0 V ≤ V _{DD} ≤ 5.5 V		20.0	mA
				2.7 V ≤ V _{DD} < 4.0 V		3.0	mA
				2.0 V ≤ V _{DD} < 2.7 V		0.6	mA
		P00 to P04	Total ^{Note 3}	4.0 V ≤ V _{DD} ≤ 5.5 V		80.0	mA
				2.7 V ≤ V _{DD} < 4.0 V		12.0	mA
				2.0 V ≤ V _{DD} < 2.7 V		2.4	mA
Total of all pins ^{Note 3}						100.0	mA
Input voltage, high	V _{IH1}			0.8 V _{DD}		V _{DD}	V
Input voltage, low	V _{IL1}			0		0.2 V _{DD}	V
Output voltage, high ^{Note 5}	V _{OH1}	4.0 V ≤ V _{DD} ≤ 5.5 V	I _{OH} = -10 mA	V _{DD} -1.5			V
			I _{OH} = -3.0 mA	V _{DD} -0.7			V
		2.7 V ≤ V _{DD} ≤ 5.5 V	I _{OH} = -2.0 mA	V _{DD} -0.6			V
		2.0 V ≤ V _{DD} ≤ 5.5 V	I _{OH} = -1.5 mA	V _{DD} -0.5			V
Output voltage, low ^{Note 6}	V _{OL1}	4.0 V ≤ V _{DD} ≤ 5.5 V	I _{OL} = 20 mA			1.3	V
			I _{OL} = 8.5 mA			0.7	V
		2.7 V ≤ V _{DD} ≤ 5.5 V	I _{OL} = 3.0 mA			0.6	V
			I _{OL} = 1.5 mA			0.4	V
2.0 V ≤ V _{DD} ≤ 5.5 V	I _{OL} = 0.6 mA			0.4	V		
Input leakage current, high	I _{LIH1}	V _I = V _{DD}				1	μA
Input leakage current, low	I _{LIL1}	V _I = V _{SS}				-1	μA
On-chip pull-up resistance	R _U	V _I = V _{SS}		10	20	100	kΩ

- Notes**
- Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.
 - Do not exceed the total current value.
 - This is the output current value under conditions where the duty factor ≤ 70%.
The output current value when the duty factor > 70% can be calculated with the following expression (when changing the duty factor to n%).

- Total output current of pins = $(I_{OH} \times 0.7)/(n \times 0.01)$
<Example> Where $n = 80\%$ and $I_{OH} = -10.0\text{ mA}$
Total output current of pins = $(-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7\text{ mA}$
- Total output current of pins = $(I_{OL} \times 0.7)/(n \times 0.01)$
<Example> Where $n = 80\%$ and $I_{OL} = 10.0\text{ mA}$
Total output current of pins = $(10.0 \times 0.7)/(80 \times 0.01) \cong 8.7\text{ mA}$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.
5. The value under the condition which satisfies the high-level output current (I_{OH1}).
6. The value under the condition which satisfies the low-level output current (I_{OL1}).

Cautions 1. P00 and P01 do not output high level in N-ch open-drain mode.

2. **The maximum value of V_{IH} of P00 and P01 is V_{DD} even in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port.

2.3.2 Supply current characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current <small>Note 1</small>	I _{DD1}	Operating mode	Basic operation	f _{IH} = 20 MHz	V _{DD} = 3.0 V, 5.0 V		0.91		mA
			Normal operation	f _{IH} = 20 MHz	V _{DD} = 3.0 V, 5.0 V		1.57	2.04	
				f _{IH} = 5 MHz	V _{DD} = 3.0 V, 5.0 V		0.85	1.15	
	I _{DD2} <small>Note 2</small>	HALT mode		f _{IH} = 20 MHz	V _{DD} = 3.0 V, 5.0 V		350	820	μA
				f _{IH} = 5 MHz	V _{DD} = 3.0 V, 5.0 V		290	600	
I _{DD3} <small>Note 3</small>	STOP mode	V _{DD} = 3.0 V				0.56	2.00	μA	
WDT supply current <small>Note 4</small>	I _{WDT}	f _{IL} = 15 kHz					0.31		μA
ADC supply current <small>Note 5</small>	I _{ADC}	During conversion at the highest speed	V _{DD} = 5.0 V				1.30	1.90	mA
			V _{DD} = 3.0 V				0.50		

- Notes**
- Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the watchdog timer, A/D converter, I/O port, and on-chip pull-up/pull-down resistors.
 - During HALT instruction execution by flash memory.
 - When the high-speed on-chip oscillator is stopped.
 - Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.
 - Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

- Remarks**
- f_{IL}: Low-speed on-chip oscillator clock frequency
 - f_{IH}: High-speed on-chip oscillator clock frequency
 - Temperature condition of the TYP. value is T_A = 25°C

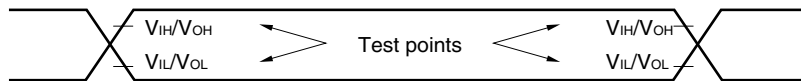
2.4 AC Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

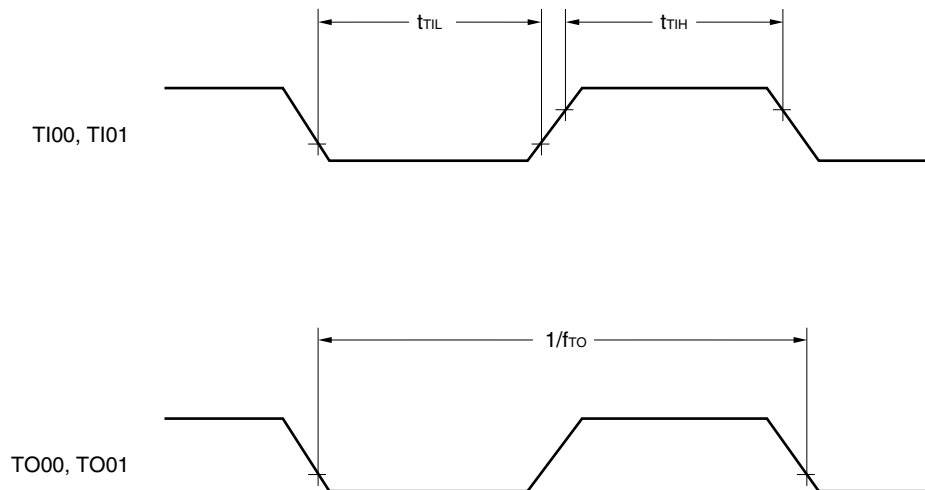
Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.05		0.8	μs
			$2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.2		0.8	μs
TI00, TI01 input high-level width, low-level width	t_{TH}, t_{TL}	Noise filter is not used	$1/f_{MCK} + 10$			ns	
TO00, TO01 output frequency	f_{TO}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			10	MHz	
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$			5	MHz	
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$			2.5	MHz	
PCLBUZ0 output frequency	f_{PCL}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			10	MHz	
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$			5	MHz	
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$			2.5	MHz	
RESET low-level width	t_{RSL}		10			μs	

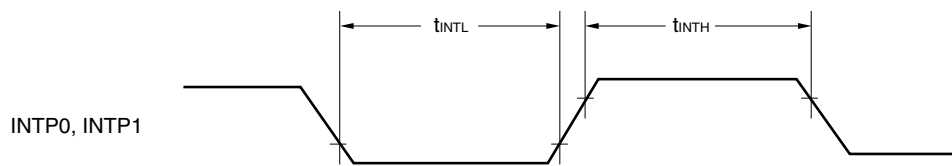
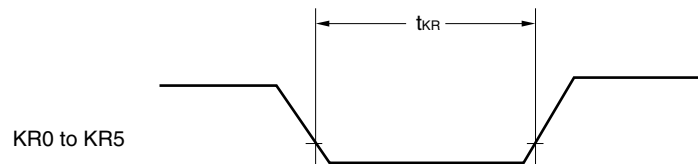
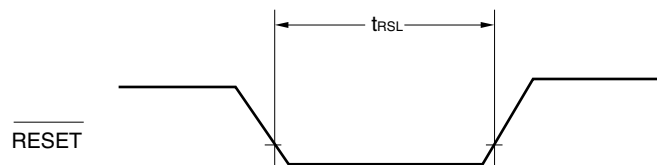
Remark f_{MCK} : Timer array unit operation clock frequency

AC Timing Test Points



TI/TO Timing



Interrupt Request Input Timing**Key Interrupt Input Timing** **$\overline{\text{RESET}}$ Input Timing**

2.5 Serial Communication Characteristics

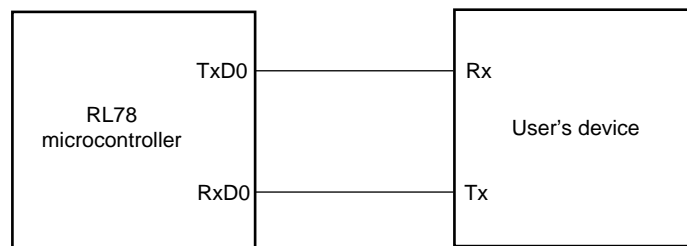
2.5.1 Serial array unit

(1) UART mode

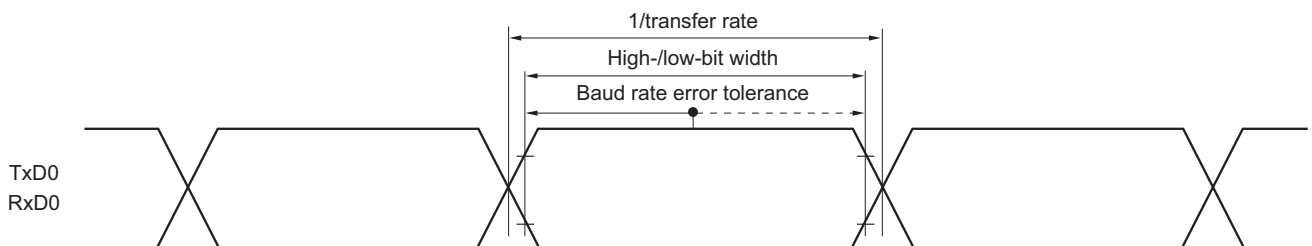
($T_A = -40$ to $+85^\circ\text{C}$, $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					$f_{mck}/6$	bps
		Theoretical value of the maximum transfer rate $f_{CLK} = f_{mck} = 20\text{ MHz}$			3.3	Mbps

UART mode connection diagram



UART mode bit width (reference)



Remark f_{mck} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00))

(3) CSI mode (slave mode, SCKp... external clock input)**($T_A = -40$ to $+85^\circ\text{C}$, $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY2}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$f_{MCK} = 20\text{ MHz}$	$8/f_{MCK}$			ns
			$f_{MCK} \leq 10\text{ MHz}$	$6/f_{MCK}$			ns
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$		$6/f_{MCK}$			ns
SCKp high-/low-level width	t_{KH2} , t_{KL2}	$2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$t_{KCY2}/2$			ns
Slp setup time (to SCKp \uparrow) ^{Note 1}	t_{SIK2}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$1/f_{MCK} + 20$			ns
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$		$1/f_{MCK} + 30$			ns
Slp hold time (from SCKp \uparrow) ^{Note 2}	t_{KSI2}	$2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$1/f_{MCK} + 31$			ns
Delay time from SCKp \downarrow to SOP output ^{Note 3}	t_{KS02}	$C = 30\text{ pF}$ ^{Note 4}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$2/f_{MCK} + 50$	ns
			$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$			$2/f_{MCK} + 110$	ns

- Notes**
1. When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$. The Slp setup time becomes “to SCKp \downarrow ” when $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.
 2. When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$. The Slp hold time becomes “from SCKp \downarrow ” when $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.
 3. When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$. The delay time to SOP output becomes “from SCKp \uparrow ” when $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.
 4. C is the load capacitance of the SOP output lines.

- Remarks**
1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0)
 2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(4) Simplified I²C mode**(T_A = -40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

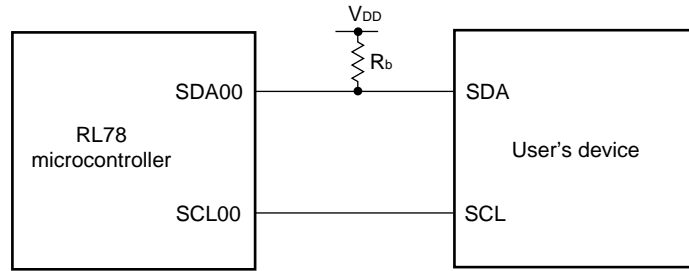
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f _{SCL}	2.0 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ		400 ^{Note 1}	kHz
Hold time when SCLr = "L"	t _{LOW}	2.0 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1150		ns
Hold time when SCLr = "H"	t _{HIGH}	2.0 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1150		ns
Data setup time (reception)	t _{SU: DAT}	2.0 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1/f _{MCK} + 145 ^{Note 2}		ns
Data hold time (transmission)	t _{HD: DAT}	2.0 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	0	355	ns

- Notes**
1. The value must also be equal to or less than f_{MCK}/4.
 2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

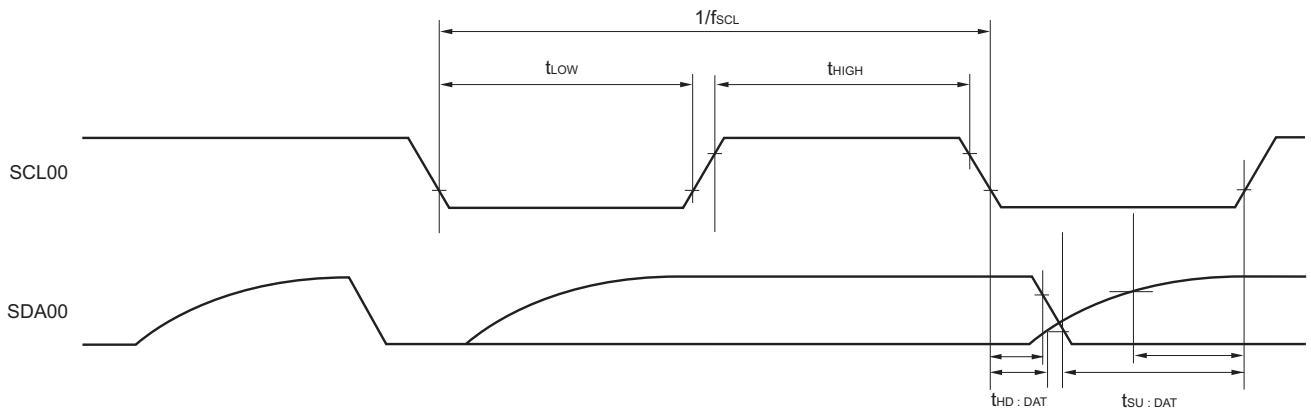
Caution Select the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin by using the port output mode register 0 (POM0).

- Remarks**
1. R_b [Ω]: Communication line (SDAr) pull-up resistance, C_b [F]: Communication line (SCLr, SDAr) load capacitance
 2. r: IIC number (r = 00)
 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

Simplified I²C mode connection diagram



Simplified I²C mode serial transfer timing



2.6 Analog Characteristics

2.6.1 A/D converter characteristics

(Target ANI pin : ANI0 to ANI3)

($T_A = -40$ to $+85^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution	$V_{DD} = 5\text{ V}$		± 1.7	± 3.1 ^{Note 2}	LSB
			$V_{DD} = 3\text{ V}$		± 2.3	± 4.5 ^{Note 2}	LSB
Conversion time	t_{CONV}	10-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.4		18.4	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	4.6		18.4	μs
Zero-scale error ^{Note 1}	E _{ZS}	10-bit resolution	$V_{DD} = 5\text{ V}$			± 0.19 ^{Note 2}	%FSR
			$V_{DD} = 3\text{ V}$			± 0.39 ^{Note 2}	%FSR
Full-scale error ^{Note 1}	E _{FS}	10-bit resolution	$V_{DD} = 5\text{ V}$			± 0.29 ^{Note 2}	%FSR
			$V_{DD} = 3\text{ V}$			± 0.42 ^{Note 2}	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution	$V_{DD} = 5\text{ V}$			± 1.8 ^{Note 2}	LSB
			$V_{DD} = 3\text{ V}$			± 1.7 ^{Note 2}	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution	$V_{DD} = 5\text{ V}$			± 1.4 ^{Note 2}	LSB
			$V_{DD} = 3\text{ V}$			± 1.5 ^{Note 2}	LSB
Analog input voltage	V_{AIN}			0		V_{DD}	V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This is the characteristic evaluation value plus or minus 3. These values are not used in the shipping inspection.

2.6.2 SPOR circuit characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection supply voltage	V_{SPOR0}	Power supply rise time	4.08	4.28	4.45	V
		Power supply fall time	4.00	4.20	4.37	V
	V_{SPOR1}	Power supply rise time	2.76	2.90	3.02	V
		Power supply fall time	2.70	2.84	2.96	V
	V_{SPOR2}	Power supply rise time	2.44	2.57	2.68	V
		Power supply fall time	2.40	2.52	2.62	V
	V_{SPOR3}	Power supply rise time	2.05	2.16	2.25	V
		Power supply fall time	2.00	2.11	2.20	V
Minimum pulse width ^{Note}	T_{SPW}		300			μs

Note Time required for the reset operation by the SPOR when V_{DD} becomes under V_{SPDR} .

2.6.3 Power supply voltage rising slope characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

2.6.4 Data retention power supply voltage characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage range	V_{DDDR}		1.9		5.5	V

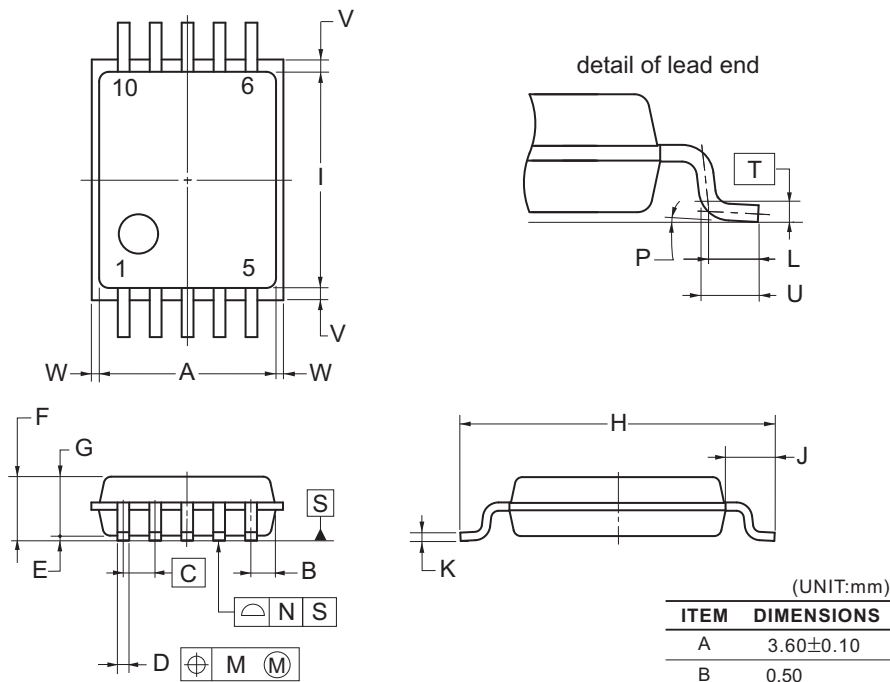
Caution Data is retained until the power supply voltage becomes under the minimum value of the data retention power supply voltage range. Note that data in the RAM and RESF registers might not be cleared even if the power supply voltage becomes under the minimum value of the data retention power supply voltage range.

3. PACKAGE DRAWINGS

3.1 10-pin products

R5F10Y16ASP, R5F10Y14ASP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP10-4.4x3.6-0.65	PLSP0010JA-A	P10MA-65-CAC-2	0.05



NOTE
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

(UNIT:mm)

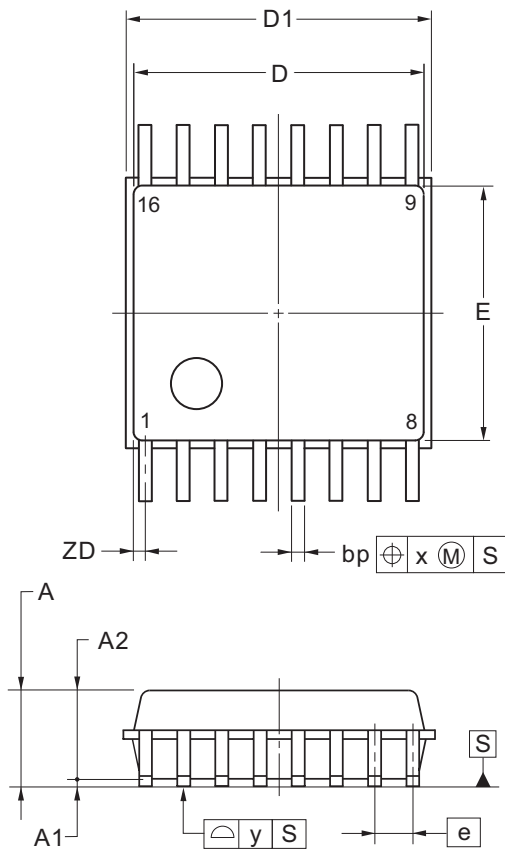
ITEM	DIMENSIONS
A	3.60±0.10
B	0.50
C	0.65 (T.P.)
D	0.24±0.08
E	0.10±0.05
F	1.45 MAX.
G	1.20±0.10
H	6.40±0.20
I	4.40±0.10
J	1.00±0.20
K	0.17 ^{+0.08} _{-0.07}
L	0.50
M	0.13
N	0.10
P	3° ^{+5°} _{-3°}
T	0.25 (T.P.)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

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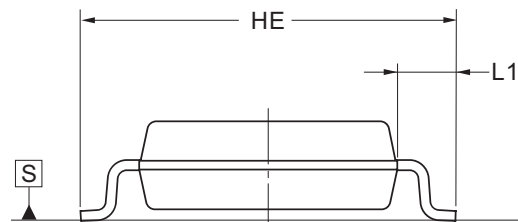
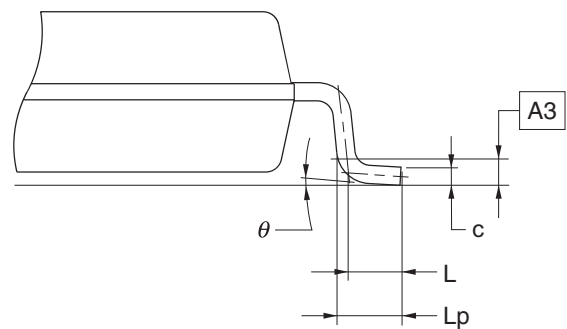
3.2 16-pin products

R5F10Y47ASP, R5F10Y46ASP, R5F10Y44ASP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-SSOP16-4.4x5-0.65	PRSP0016JC-A	P16MA-65-FAA-2	0.08



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	5.00±0.15
D1	5.20±0.15
E	4.40±0.20
HE	6.40±0.20
A	1.725 MAX.
A1	0.125±0.05
A2	1.50
A3	0.25
e	0.65
bp	0.22 ^{+0.08} _{-0.07}
c	0.15 ^{+0.03} _{-0.04}
L	0.50
Lp	0.60±0.10
L1	1.00±0.20
x	0.13
y	0.10
θ	3° ^{+5°} _{-3°}
ZD	0.325

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