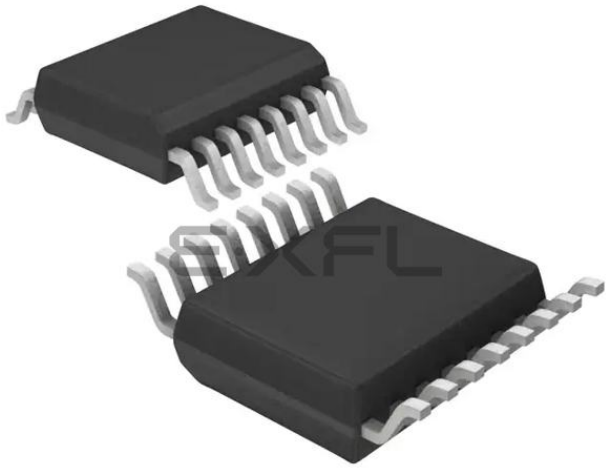
Renesas Electronics America Inc - R5F10Y44ASP#30 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	20MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	10
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 7x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SSOP (0.173", 4.40mm Width)
Supplier Device Package	16-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10y44asp-30

○ ROM, RAM capacities

Flash ROM	RAM	10 pins	16 pins
4 KB	512 B	–	R5F10Y47ASP Note 2
2 KB	256 B	R5F10Y16ASP	R5F10Y46ASP Note 2
1 KB	128 B	R5F10Y14ASP	R5F10Y44ASP Note 2

Notes 1. 16-pin products only

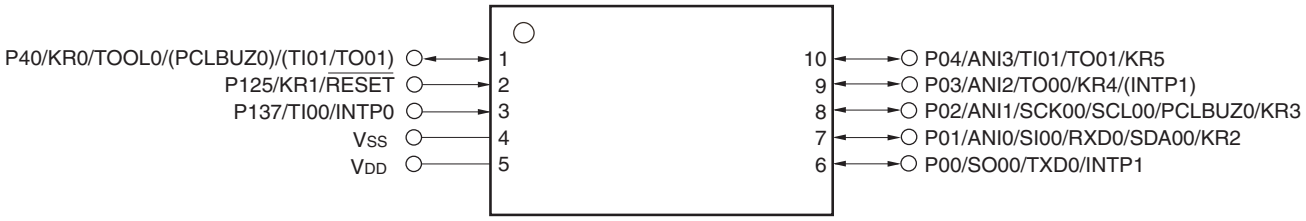
2. Under development

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

1.3 Pin Configuration (Top View)

1.3.1 10-pin products

- 10-pin plastic LSSOP (4.4 × 3.6)

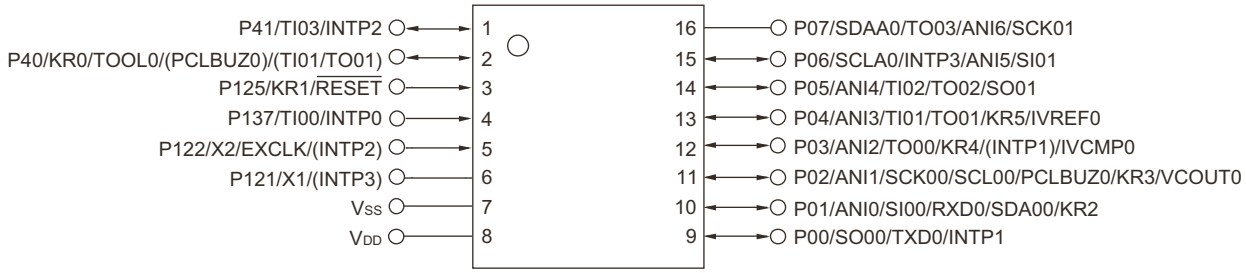


Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.2 16-pin products

- 16-pin plastic SSOP (4.4 × 5.0)



Remarks 1. For pin identification, see **1.4 Pin Identification**.

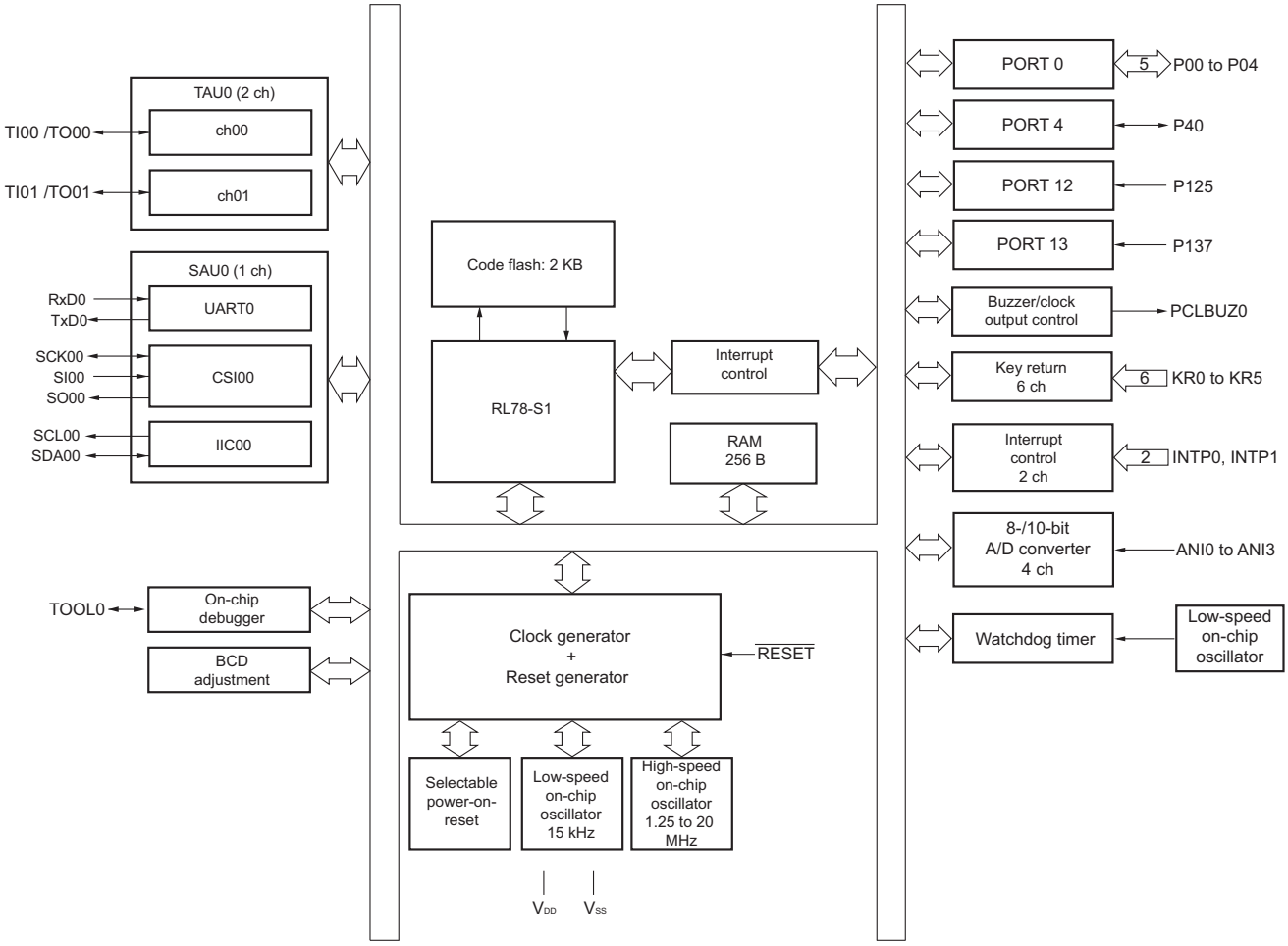
2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.4 Pin Identification

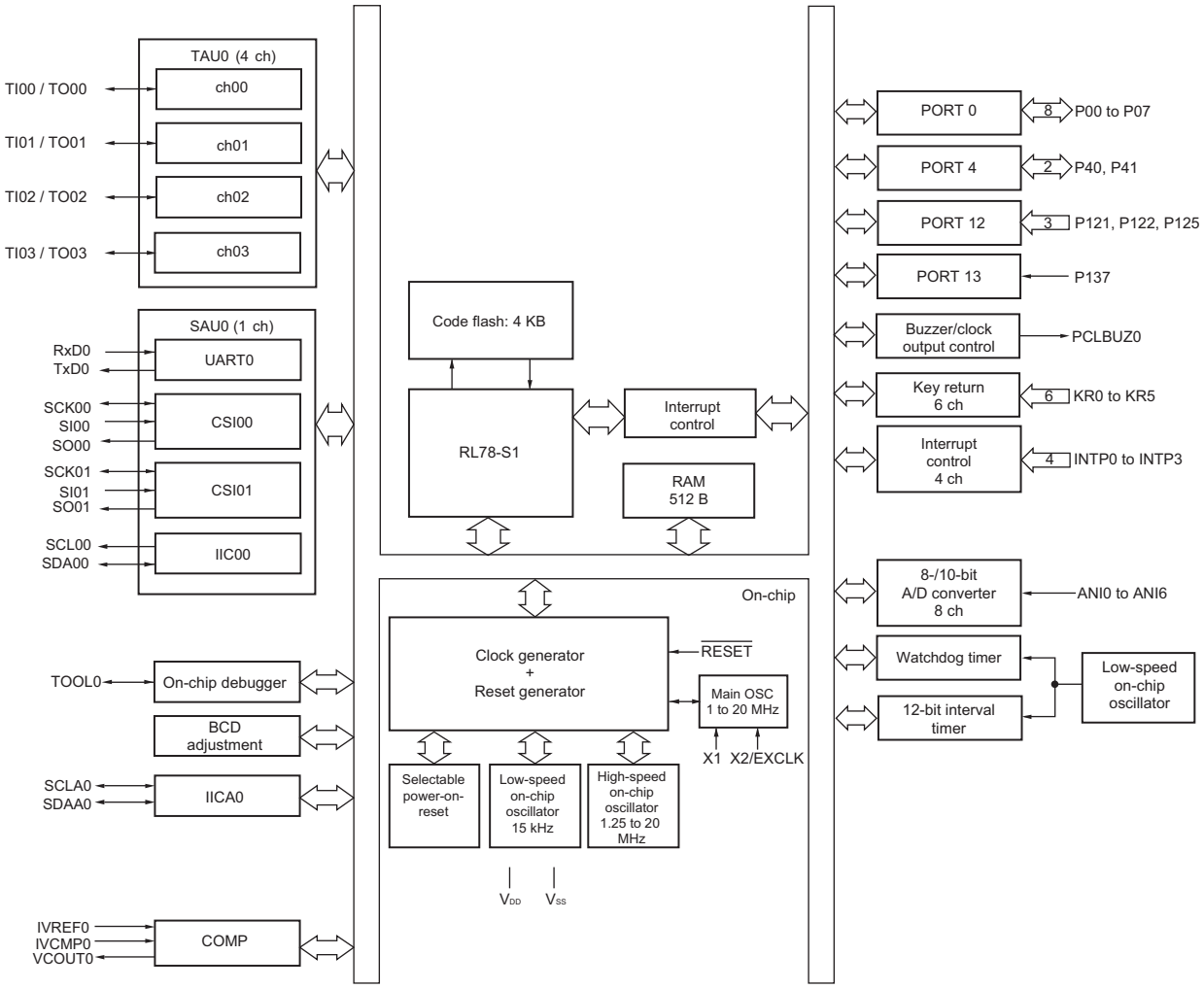
ANI0 to ANI6 : Analog Input
INTP0 to INTP3 : External Interrupt Input
KR0 to KR5 : Key Return
P00 to P07 : Port 0
P40, P41 : Port 4
P121, P122, P125 : Port 12
P137 : Port 13
PCLBUZ0 : Programmable Clock Output/ Buzzer Output
EXCLK : External Clock Input
X1, X2 : Crystal Oscillator
IVCMP0 : Comparator Input
VCOUT0 : Comparator Output
IVREF0 : Comparator Reference Input
$\overline{\text{RESET}}$: Reset
RxD0 : Receive Data
SCK00, SCK01 : Serial Clock Input/Output
SCL00, SCLA0 : Serial Clock Output
SDA00, SDAA0 : Serial Data Input/Output
SI00, SI01 : Serial Data Input
SO00, SO01 : Serial Data Output
TI00 to TI03 : Timer Input
TO00 to TO03 : Timer Output
TOOL0 : Data Input/Output for Tool
TxD0 : Transmit Data
V_{DD} : Power Supply
V_{SS} : Ground

1.5 Block Diagram

1.5.1 10-pin products



1.5.2 16-pin products



1.6 Outline of Functions

This outline describes the function at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

Item		10-pin		16-pin		
		R5F10Y16ASP	R5F10Y14ASP	R5F10Y47ASP	R5F10Y46ASP	R5F10Y44ASP
Code flash memory		2 KB	1 KB	4 KB	2 KB	1 KB
RAM		256 B	128 B	512 B	256 B	128 B
Main system clock	High-speed system clock	—		X1, X2 (crystal/ceramic) oscillation, external main system clock input (EXCLK): 1 to 20 MHz: V_{DD} = 2.7 to 5.5 V 1 to 5 MHz: V_{DD} = 2.0 to 5.5 V		
	High-speed on-chip oscillator clock	• 1.25 to 20 MHz (V_{DD} = 2.7 to 5.5 V) • 1.25 to 5 MHz (V_{DD} = 2.0 to 5.5 V)				
Low-speed on-chip oscillator clock		15 kHz (TYP)				
General-purpose register		8-bit register × 8				
Minimum instruction execution time		0.05 μs (20 MHz operation)				
Instruction set		• Data transfer (8 bits) • Adder and subtractor/logical operation (8 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc.				
I/O port	Total	8		14		
	CMOS I/O	6 (N-ch open-drain output (V_{DD} tolerance): 2)		10 (N-ch open-drain output (V_{DD} tolerance): 4)		
	CMOS input	2		4		
Timer	16-bit timer	2 channels		4 channels		
	Watchdog timer	1 channel				
	12-bit interval timer	—		1 channel		
	Timer output	2 channels (PWM output: 1)		4 channels (PWM outputs: 3[Note 1])		
Clock output/buzzer output		1				
		2.44 kHz to 10 MHz: (Peripheral hardware clock: f_{MAIN} = 20 MHz operation)				
Comparator		—		1		
8-/10-bit resolution A/D converter		4 channels		8 channels		
Serial interface		[10-pin products] CSI: 1 channel/simplified I^2C: 1 channel/UART: 1 channel [16-pin products] CSI: 2 channels/simplified I^2C: 1 channel/UART: 1 channel				
	I^2C bus	—		1 channel		
Vectored interrupt sources	Internal	8		14		
	External	3		5		
Key interrupt		6				
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by selectable power-on-reset • Internal reset by illegal instruction execution [Note 2] • Internal reset by data retention lower limit voltage				
Selectable power-on-reset circuit		Detection voltage: 2.0 V/2.4 V/2.7 V/4.0 V				
On-chip debug function		Provided				
Power supply voltage		V_{DD} = 2.0 to 5.5 V				
Operating ambient temperature		T_A = - 40 to + 85 °C				

2. ELECTRICAL SPECIFICATIONS

Cautions 1. This chapter explains the electrical specifications of two products, the R5F10Y16ASP and the R5F10Y14ASP.

2. Electrical specifications for the 16-pin products are T. B. D. because these products are under development.

3. The RL78/G10 has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

4. The pins mounted depend on the product. Refer to 2.1 Port Functions and 2.2.1 Functions for each product in the RL78/G10 User's Manual.

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
  <Example> Where n = 80 % and I_{OH} = - 10.0 mA
  Total output current of pins = (- 10.0 × 0.7)/(80 × 0.01) ≅ - 8.7 mA
- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)
  <Example> Where n = 80 % and I_{OL} = 10.0 mA
  Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.
5. The value under the condition which satisfies the high-level output current (I_{OH1}).
6. The value under the condition which satisfies the low-level output current (I_{OL1}).

Cautions 1. P00 and P01 do not output high level in N-ch open-drain mode.
2. The maximum value of V_{IH} of P00 and P01 is V_{DD} even in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port.

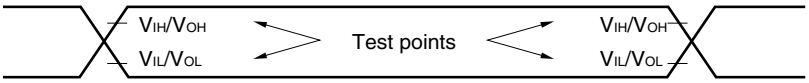
2.4 AC Characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

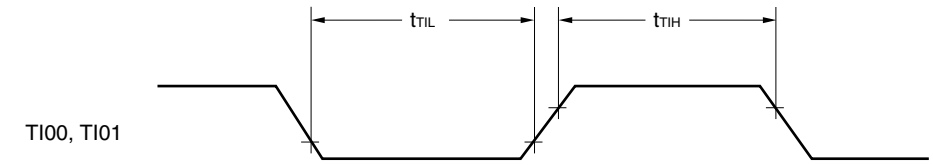
Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	2.7 V ≤ V_{DD} ≤ 5.5 V	0.05		0.8	μs
			2.0 V ≤ V_{DD} ≤ 5.5 V	0.2		0.8	μs
TI00, TI01 input high-level width, low-level width	t_{TIH}, t_{TIL}	Noise filter is not used		1/f_{MCK} + 10			ns
TO00, TO01 output frequency	f_{TO}	4.0 V ≤ V_{DD} ≤ 5.5 V				10	MHz
		2.7 V ≤ V_{DD} < 4.0 V				5	MHz
		2.0 V ≤ V_{DD} < 2.7 V				2.5	MHz
PCLBUZ0 output frequency	f_{PCL}	4.0 V ≤ V_{DD} ≤ 5.5 V				10	MHz
		2.7 V ≤ V_{DD} < 4.0 V				5	MHz
		2.0 V ≤ V_{DD} < 2.7 V				2.5	MHz
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

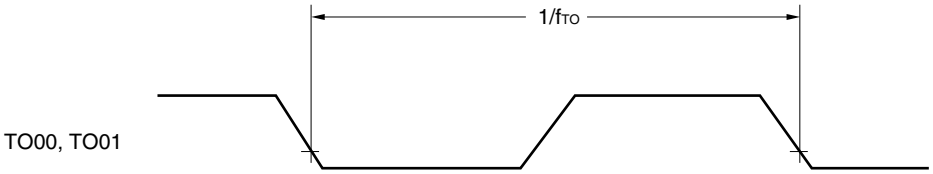
Remark f_{MCK}: Timer array unit operation clock frequency

AC Timing Test Points

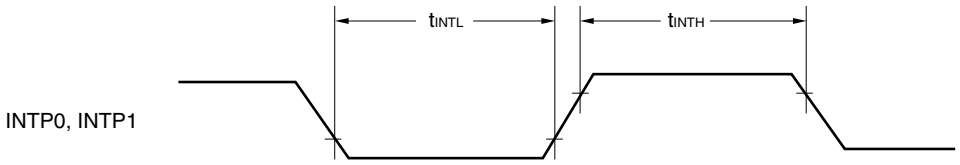


TI/TO Timing

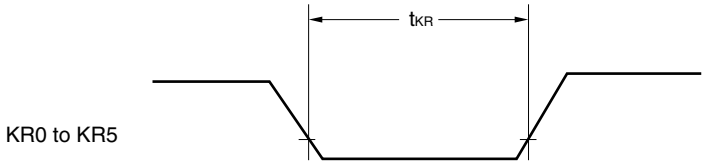




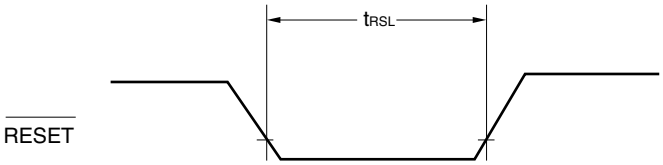
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



2.5 Serial Communication Characteristics

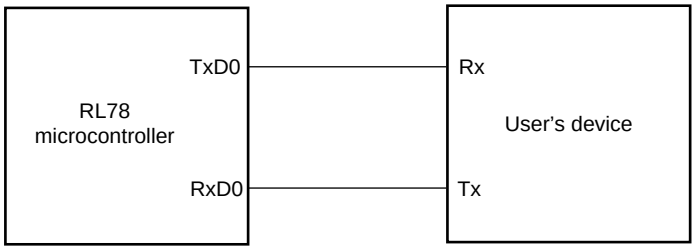
2.5.1 Serial array unit

(1) UART mode

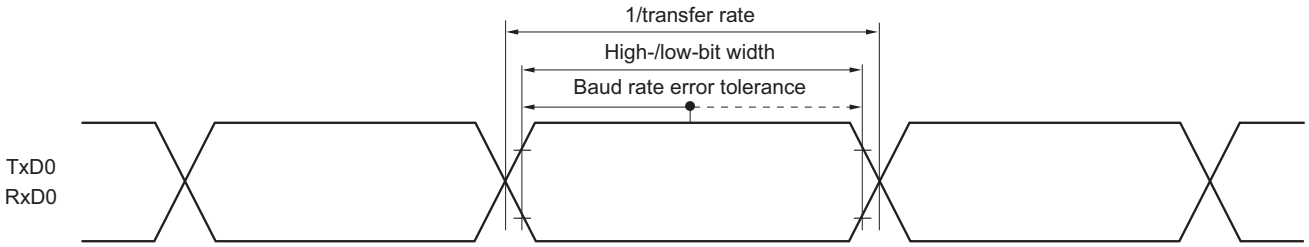
(T_A = −40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{CLK} = f_{MCK} = 20 MHz			3.3	Mbps

UART mode connection diagram



UART mode bit width (reference)



Remark f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

(2) CSI mode (master mode, SCKp... internal clock output)

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	2.7 V ≤ V_{DD} ≤ 5.5 V	200			ns
			2.0 V ≤ V_{DD} ≤ 5.5 V	800			ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2-18			ns
		2.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2-50			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 5.5 V		47			ns
		2.0 V ≤ V_{DD} ≤ 5.5 V		110			ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}			19			ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4				25	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

Remarks 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

(3) CSI mode (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY2}	2.7 V ≤ V_{DD} ≤ 5.5 V	f_{MCK} = 20 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 10 MHz	6/f_{MCK}			ns
		2.0 V ≤ V_{DD} < 2.7 V		6/f_{MCK}			ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2			ns
SIp setup time (to SCKp↑)[Note 1]	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 20			ns
		2.0 V ≤ V_{DD} < 2.7 V		1/f_{MCK} + 30			ns
SIp hold time (from SCKp↑) [Note 2]	t_{KSI2}	2.0 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 31			ns
Delay time from SCKp↓ to SOp output [Note 3]	t_{KSO2}	C = 30 pF [Note 4]	2.7 V ≤ V_{DD} ≤ 5.5 V			2/f_{MCK} + 50	ns
			2.0 V ≤ V_{DD} < 2.7 V			2/f_{MCK} + 110	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SOp output lines.

Remarks 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(4) Simplified I²C mode

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	2.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1	kHz
Hold time when SCLr = "L"	t_{LOW}	2.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		ns
Hold time when SCLr = "H"	t_{HIGH}	2.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		ns
Data setup time (reception)	$t_{SU:DAT}$	2.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 145 Note 2		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	355	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.

2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

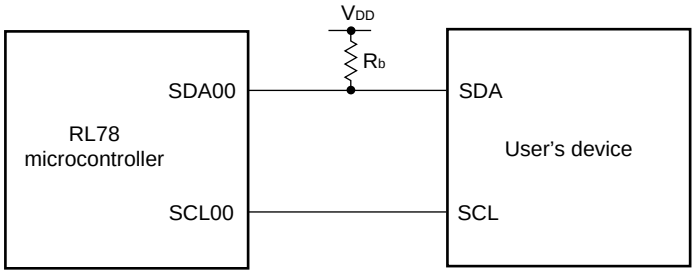
Caution Select the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin by using the port output mode register 0 (POM0).

Remarks 1. R_b [Ω]: Communication line (SDAr) pull-up resistance, C_b [F]: Communication line (SCLr, SDAr) load capacitance

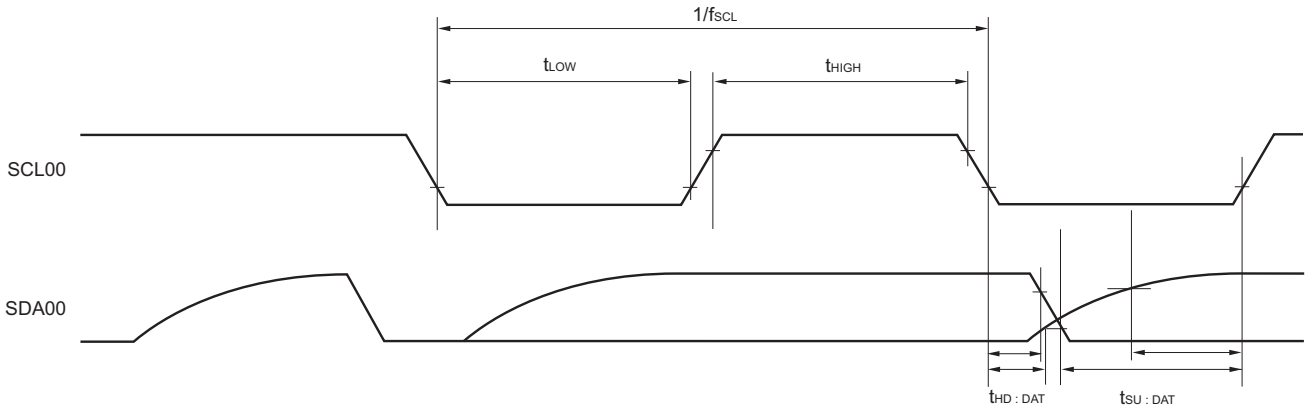
2. r: IIC number (r = 00)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

Simplified I²C mode connection diagram



Simplified I²C mode serial transfer timing



2.6 Analog Characteristics

2.6.1 A/D converter characteristics

(Target ANI pin : ANI0 to ANI3)

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution	V_{DD} = 5 V		±1.7	±3.1[Note 2]	LSB
			V_{DD} = 3 V		±2.3	±4.5[Note 2]	LSB
Conversion time	t_{CONV}	10-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V	3.4		18.4	µs
			2.4 V ≤ V_{DD} ≤ 5.5 V	4.6		18.4	µs
Zero-scale error[Note 1]	E_{ZS}	10-bit resolution	V_{DD} = 5 V			±0.19[Note 2]	%FSR
			V_{DD} = 3 V			±0.39[Note 2]	%FSR
Full-scale error[Note 1]	E_{FS}	10-bit resolution	V_{DD} = 5 V			±0.29[Note 2]	%FSR
			V_{DD} = 3 V			±0.42[Note 2]	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution	V_{DD} = 5 V			±1.8[Note 2]	LSB
			V_{DD} = 3 V			±1.7[Note 2]	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution	V_{DD} = 5 V			±1.4[Note 2]	LSB
			V_{DD} = 3 V			±1.5[Note 2]	LSB
Analog input voltage	V_{AIN}			0		V_{DD}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This is the characteristic evaluation value plus or minus 3. These values are not used in the shipping inspection.

2.6.2 SPOR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection supply voltage	V_{SPOR0}	Power supply rise time	4.08	4.28	4.45	V
		Power supply fall time	4.00	4.20	4.37	V
	V_{SPOR1}	Power supply rise time	2.76	2.90	3.02	V
		Power supply fall time	2.70	2.84	2.96	V
	V_{SPOR2}	Power supply rise time	2.44	2.57	2.68	V
		Power supply fall time	2.40	2.52	2.62	V
	V_{SPOR3}	Power supply rise time	2.05	2.16	2.25	V
		Power supply fall time	2.00	2.11	2.20	V
Minimum pulse width[Note]	T_{SPW}		300			µs

Note Time required for the reset operation by the SPOR when V_{DD} becomes under V_{SPDR}.

2.6.3 Power supply voltage rising slope characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

2.6.4 Data retention power supply voltage characteristics

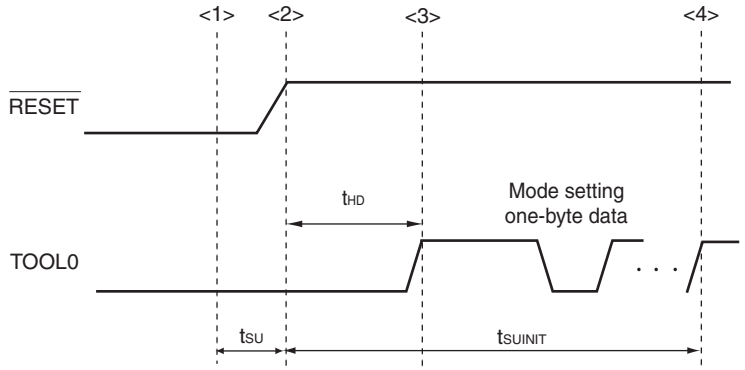
(T_A = –40 to +85°C, Vss = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage range	V_{DDDR}		1.9		5.5	V

Caution Data is retained until the power supply voltage becomes under the minimum value of the data retention power supply voltage range. Note that data in the RAM and RESF registers might not be cleared even if the power supply voltage becomes under the minimum value of the data retention power supply voltage range.

2.9 Timing of Entry to Flash Memory Programming Modes

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	SPOR reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t_{SU}	SPOR reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends	t_{HD}	SPOR reset must end before the external reset ends.	1			ms



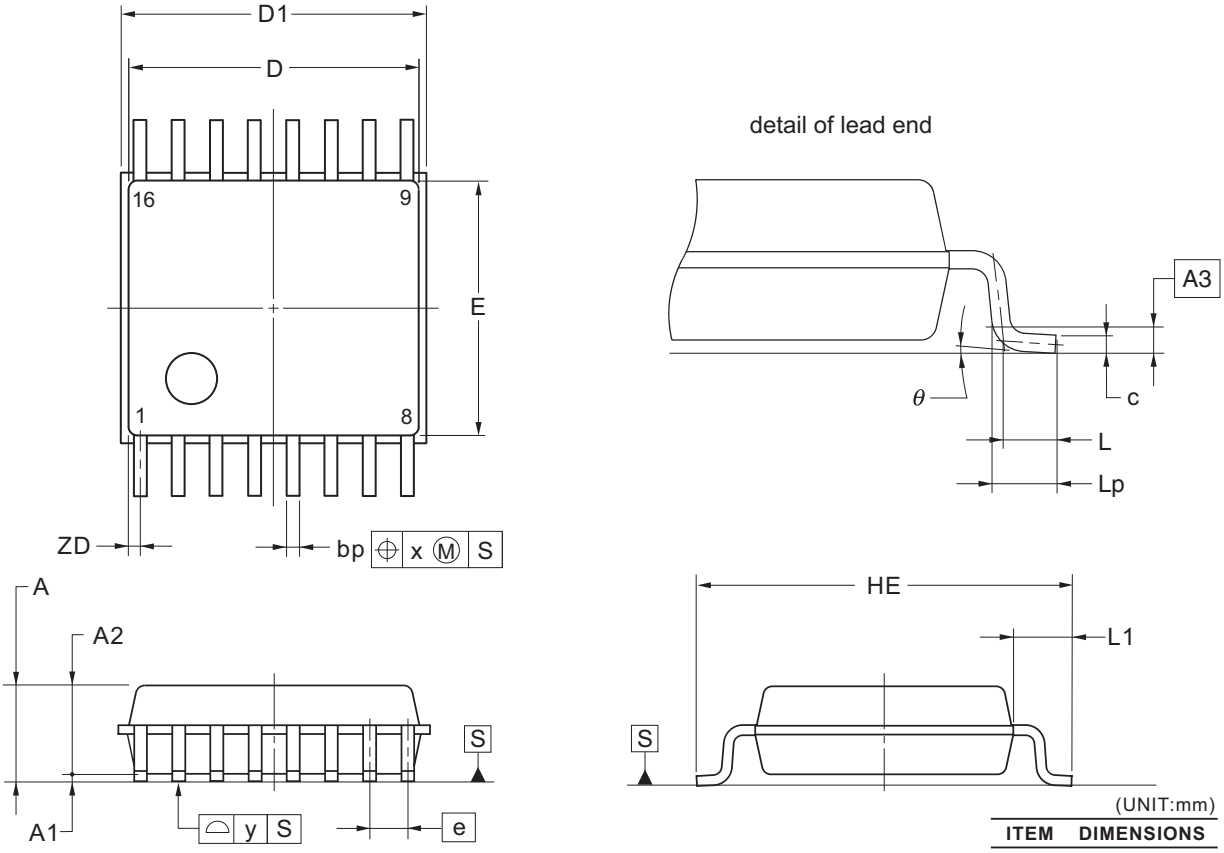
<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (SPOR reset must end before the external reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of entry to the flash memory programming mode by UART reception.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.
t_{SU}: How long from when the TOOL0 pin is placed at the low level until an external reset ends (MIN. 10 μs)
t_{HD}: How long to keep the TOOL0 pin at the low level from when the external reset ends

3.2 16-pin products

R5F10Y47ASP, R5F10Y46ASP, R5F10Y44ASP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-SSOP16-4.4x5-0.65	PRSP0016JC-A	P16MA-65-FAA-2	0.08



(UNIT:mm)

ITEM	DIMENSIONS
D	5.00±0.15
D1	5.20±0.15
E	4.40±0.20
HE	6.40±0.20
A	1.725 MAX.
A1	0.125±0.05
A2	1.50
A3	0.25
e	0.65
bp	$0.22^{+0.08}_{-0.07}$
c	$0.15^{+0.03}_{-0.04}$
L	0.50
Lp	0.60±0.10
L1	1.00±0.20
x	0.13
y	0.10
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
ZD	0.325

Revision History	RL78/G10 Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Apr 15, 2013	-	First Edition issued

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