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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	20MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	10
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 7x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SSOP (0.173", 4.40mm Width)
Supplier Device Package	16-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10y46asp-50

○ ROM, RAM capacities

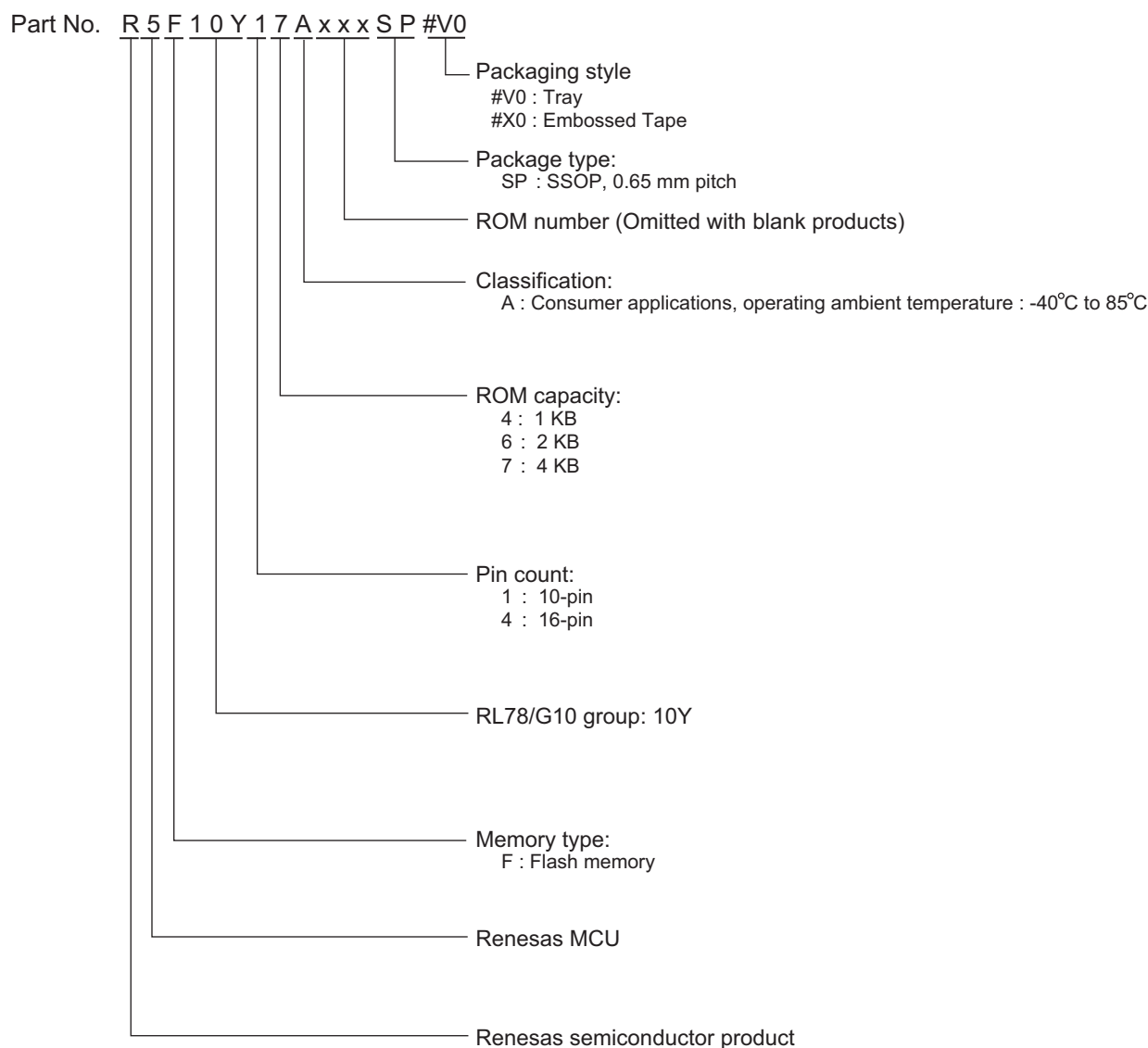
Flash ROM	RAM	10 pins	16 pins
4 KB	512 B	–	R5F10Y47ASP ^{Note 2}
2 KB	256 B	R5F10Y16ASP	R5F10Y46ASP ^{Note 2}
1 KB	128 B	R5F10Y14ASP	R5F10Y44ASP ^{Note 2}

- Notes**
1. 16-pin products only
 2. Under development

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

1.2 List of Part Number

Figure 1-1. Classification of Part Number



Pin count	Package	Part Number
10 pins	10-pin plastic LSSOP (4.4 × 3.6 mm, 0.65mmpitch)	R5F10Y16ASP#V0, R5F10Y16ASP#X0
		R5F10Y14ASP#V0, R5F10Y14ASP#X0
16 pins	16-pin plastic SSOP (4.4 × 5.0 mm, 0.65mmpitch)	R5F10Y47ASP ^{Note}
		R5F10Y46ASP ^{Note}
		R5F10Y44ASP ^{Note}

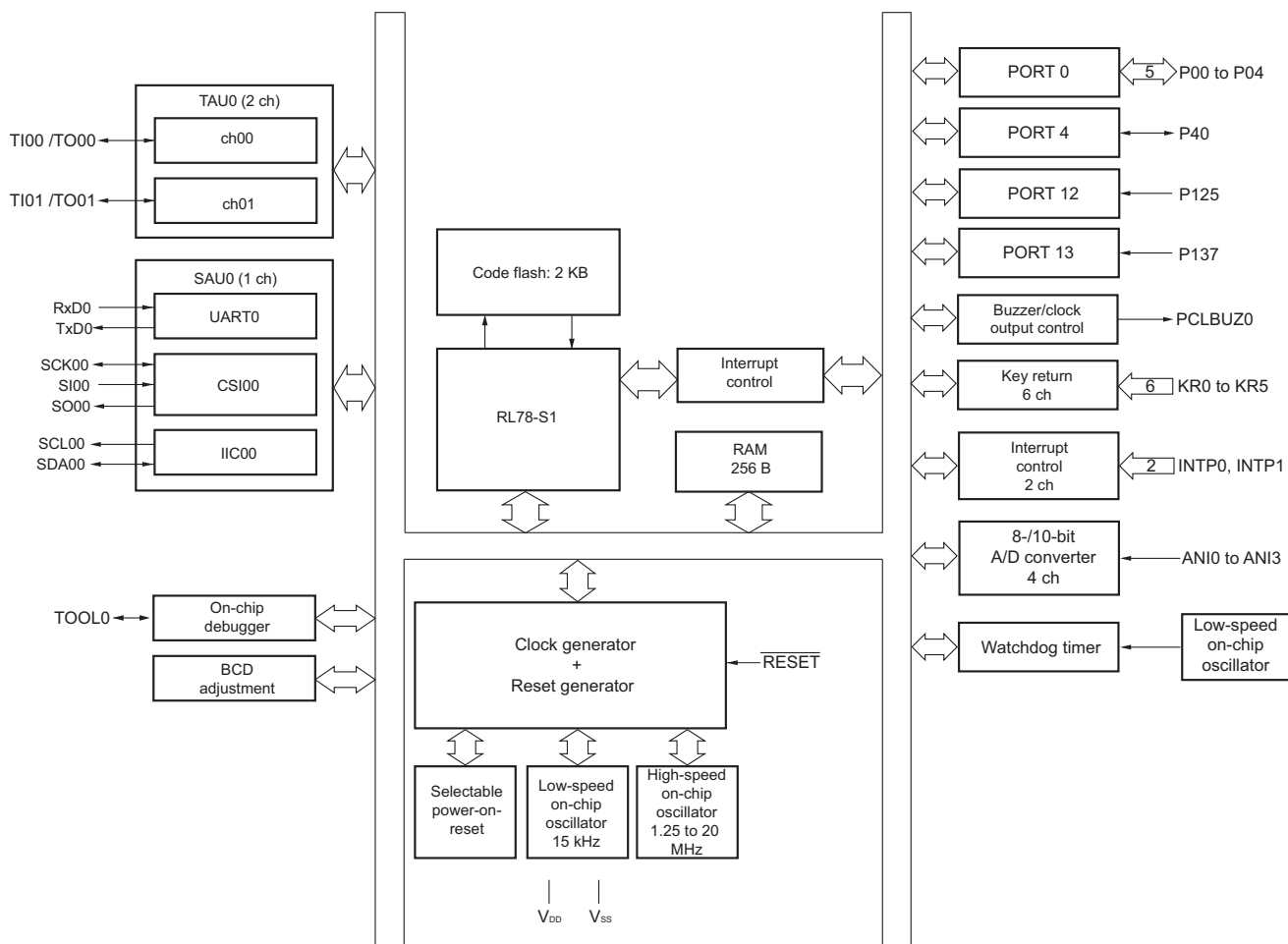
Note Under development

Caution The part number represents the number at the time of publication.

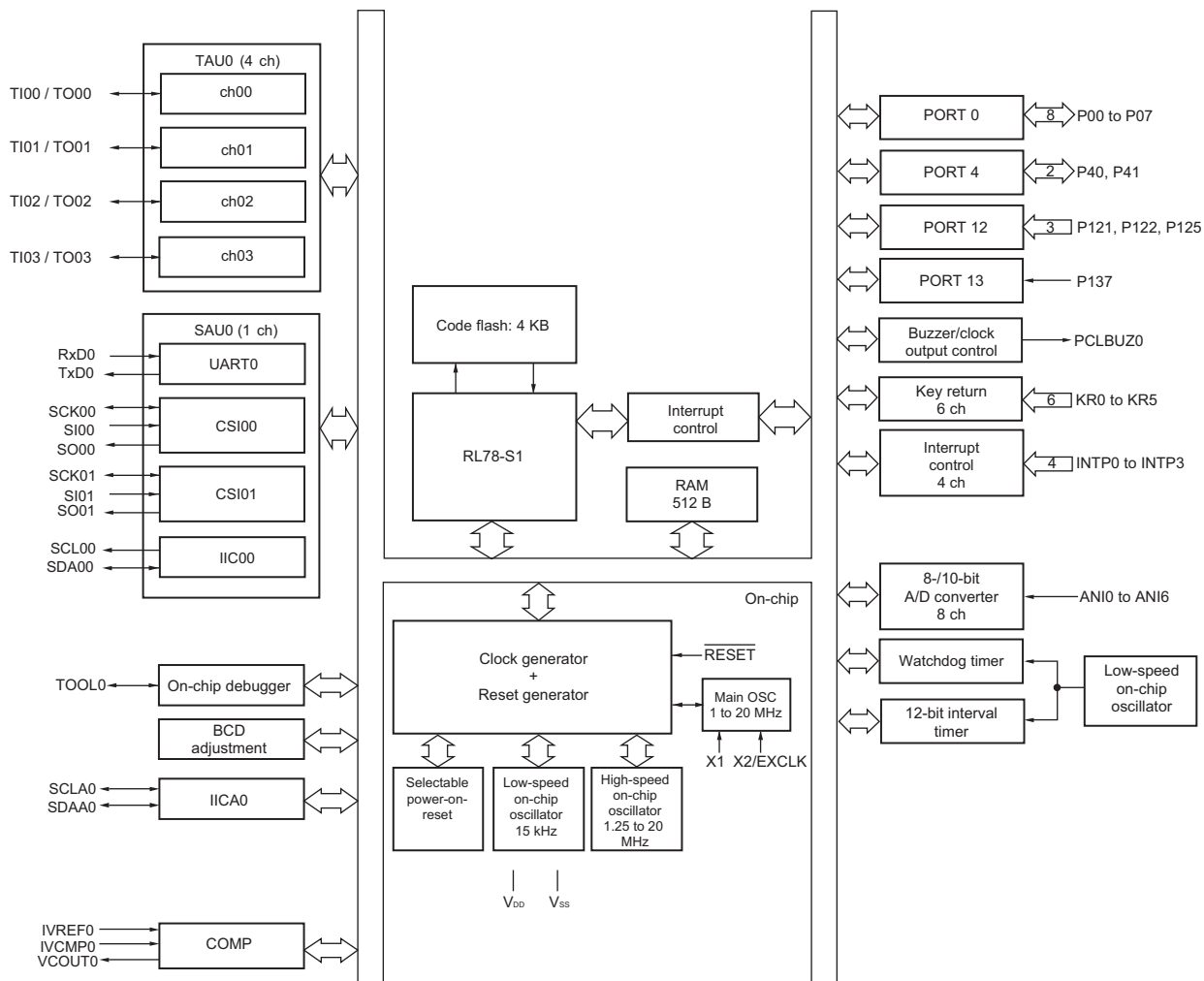
Be sure to review the latest part number through the target product page in the Renesas Electronics Corp.website.

1.5 Block Diagram

1.5.1 10-pin products



1.5.2 16-pin products



1.6 Outline of Functions

This outline describes the function at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

Item		10-pin		16-pin		
		R5F10Y16ASP	R5F10Y14ASP	R5F10Y47ASP	R5F10Y46ASP	R5F10Y44ASP
Code flash memory		2 KB	1 KB	4 KB	2 KB	1 KB
RAM		256 B	128 B	512 B	256 B	128 B
Main system clock	High-speed system clock	—		X1, X2 (crystal/ceramic) oscillation, external main system clock input (EXCLK): 1 to 20 MHz: V _{DD} = 2.7 to 5.5 V 1 to 5 MHz: V _{DD} = 2.0 to 5.5 V		
	High-speed on-chip oscillator clock	• 1.25 to 20 MHz (V _{DD} = 2.7 to 5.5 V) • 1.25 to 5 MHz (V _{DD} = 2.0 to 5.5 V)				
Low-speed on-chip oscillator clock		15 kHz (TYP)				
General-purpose register		8-bit register × 8				
Minimum instruction execution time		0.05 μs (20 MHz operation)				
Instruction set		• Data transfer (8 bits) • Adder and subtractor/logical operation (8 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc.				
I/O port	Total	8		14		
	CMOS I/O	6 (N-ch open-drain output (V _{DD} tolerance): 2)		10 (N-ch open-drain output (V _{DD} tolerance): 4)		
	CMOS input	2		4		
Timer	16-bit timer	2 channels		4 channels		
	Watchdog timer	1 channel				
	12-bit interval timer	—		1 channel		
	Timer output	2 channels (PWM output: 1)		4 channels (PWM outputs: 3 ^{Note 1})		
Clock output/buzzer output		1				
		2.44 kHz to 10 MHz: (Peripheral hardware clock: f _{MAIN} = 20 MHz operation)				
Comparator		—		1		
8-/10-bit resolution A/D converter		4 channels		8 channels		
Serial interface		[10-pin products] CSI: 1 channel/simplified I ² C: 1 channel/UART: 1 channel [16-pin products] CSI: 2 channels/simplified I ² C: 1 channel/UART: 1 channel				
		I ² C bus	—		1 channel	
Vectored interrupt sources	Internal	8		14		
	External	3		5		
Key interrupt		6				
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by selectable power-on-reset • Internal reset by illegal instruction execution ^{Note 2} • Internal reset by data retention lower limit voltage				
Selectable power-on-reset circuit		Detection voltage: 2.0 V/2.4 V/2.7 V/4.0 V				
On-chip debug function		Provided				
Power supply voltage		V _{DD} = 2.0 to 5.5 V				
Operating ambient temperature		T _A = - 40 to + 85 °C				

- Notes**
1. The number of outputs varies, depending on the setting of channels in use and the number of the master (see **6.8.3 Operation as multiple PWM output function in the RL78/G10 User's Manual**).
 2. The illegal instruction is generated when instruction code FFH is executed. Reset by the illegal instruction execution not issued by emulation with the on-chip debug emulator.

2. ELECTRICAL SPECIFICATIONS

- Cautions**
1. This chapter explains the electrical specifications of two products, the R5F10Y16ASP and the R5F10Y14ASP.
 2. Electrical specifications for the 16-pin products are T. B. D. because these products are under development.
 3. The RL78/G10 has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
 4. The pins mounted depend on the product. Refer to 2.1 Port Functions and 2.2.1 Functions for each product in the RL78/G10 User's Manual.

2.1 Absolute Maximum Ratings

($T_A = 25^\circ\text{C}$)

Parameter	Symbols	Conditions		Ratings	Unit
Supply Voltage	V_{DD}			-0.5 to +6.5	V
Input Voltage	V_{I1}			-0.3 to $V_{DD} + 0.3^{\text{Note}}$	V
Output Voltage	V_{O1}			-0.3 to $V_{DD} + 0.3$	V
Output current, high	I_{OH1}	Per pin		-40	mA
		Total of all pins	P40	-40	mA
		-140 mA	P00 to P04	-100	mA
Output current, low	I_{OL1}	Per pin		40	mA
		Total of all pins	P40	40	mA
		140 mA	P00 to P04	100	mA
Operating ambient temperature	T_A			-40 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}			-65 to +150	$^\circ\text{C}$

Note Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. The reference voltage is V_{SS} .

2.2 Oscillator Characteristics

2.2.1 On-chip oscillator characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator oscillation clock frequency ^{Notes 1, 2}	f_{IH}		1.25		20	MHz
High-speed on-chip oscillator oscillation clock frequency accuracy		$T_A = -20$ to $+85^\circ\text{C}$	-2.0		+2.0	%
		$T_A = -40$ to -20°C	-3.0		+3.0	%
Low-speed on-chip oscillator oscillation clock frequency ^{Note 3}	f_{IL}			15		kHz
Low-speed on-chip oscillator oscillation clock frequency accuracy			-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 2 of option byte (000C2H).

2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

3. This only indicates the oscillator characteristics.

2.3 DC Characteristics

2.3.1 Pin characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	I _{OH1}	P00, P01, P02 to P04, P40	Per pin				-10.0 ^{Note 2}	mA
		P40	Total ^{Note 3}	4.0 V ≤ V _{DD} ≤ 5.5 V			-10.0	mA
				2.7 V ≤ V _{DD} < 4.0 V			-2.0	mA
				2.0 V ≤ V _{DD} < 2.7 V			-1.5	mA
		P00, P01, P02 to P04	Total ^{Note 3}	4.0 V ≤ V _{DD} ≤ 5.5 V			-50.0	mA
				2.7 V ≤ V _{DD} < 4.0 V			-10.0	mA
				2.0 V ≤ V _{DD} < 2.7 V			-7.5	mA
Total of all pins ^{Note 3}						-60.0	mA	
Output current, low ^{Note 4}	I _{OL1}	P00 to P04, P40	Per pin				20.0 ^{Note 2}	mA
		P40	Total ^{Note 3}	4.0 V ≤ V _{DD} ≤ 5.5 V			20.0	mA
				2.7 V ≤ V _{DD} < 4.0 V			3.0	mA
				2.0 V ≤ V _{DD} < 2.7 V			0.6	mA
		P00 to P04	Total ^{Note 3}	4.0 V ≤ V _{DD} ≤ 5.5 V			80.0	mA
				2.7 V ≤ V _{DD} < 4.0 V			12.0	mA
				2.0 V ≤ V _{DD} < 2.7 V			2.4	mA
Total of all pins ^{Note 3}						100.0	mA	
Input voltage, high	V _{IH1}				0.8 V _{DD}		V _{DD}	V
Input voltage, low	V _{IL1}				0		0.2 V _{DD}	V
Output voltage, high ^{Note 5}	V _{OH1}	4.0 V ≤ V _{DD} ≤ 5.5 V	I _{OH} = -10 mA		V _{DD} -1.5			V
			I _{OH} = -3.0 mA		V _{DD} -0.7			V
		2.7 V ≤ V _{DD} ≤ 5.5 V	I _{OH} = -2.0 mA		V _{DD} -0.6			V
		2.0 V ≤ V _{DD} ≤ 5.5 V	I _{OH} = -1.5 mA		V _{DD} -0.5			V
Output voltage, low ^{Note 6}	V _{OL1}	4.0 V ≤ V _{DD} ≤ 5.5 V	I _{OL} = 20 mA				1.3	V
			I _{OL} = 8.5 mA				0.7	V
		2.7 V ≤ V _{DD} ≤ 5.5 V	I _{OL} = 3.0 mA				0.6	V
			I _{OL} = 1.5 mA				0.4	V
		2.0 V ≤ V _{DD} ≤ 5.5 V	I _{OL} = 0.6 mA				0.4	V
Input leakage current, high	I _{LH1}	V _I = V _{DD}					1	μA
Input leakage current, low	I _{LIL1}	V _I = V _{SS}					-1	μA
On-chip pull-up resistance	R _U	V _I = V _{SS}			10	20	100	kΩ

- Notes**
1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.
 2. Do not exceed the total current value.
 3. This is the output current value under conditions where the duty factor $\leq 70\%$.
The output current value when the duty factor $> 70\%$ can be calculated with the following expression (when changing the duty factor to n%).

- Total output current of pins = $(I_{OH} \times 0.7)/(n \times 0.01)$
<Example> Where $n = 80\%$ and $I_{OH} = -10.0\text{ mA}$
Total output current of pins = $(-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7\text{ mA}$
- Total output current of pins = $(I_{OL} \times 0.7)/(n \times 0.01)$
<Example> Where $n = 80\%$ and $I_{OL} = 10.0\text{ mA}$
Total output current of pins = $(10.0 \times 0.7)/(80 \times 0.01) \cong 8.7\text{ mA}$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.
5. The value under the condition which satisfies the high-level output current (I_{OH1}).
6. The value under the condition which satisfies the low-level output current (I_{OL1}).

Cautions 1. P00 and P01 do not output high level in N-ch open-drain mode.

2. **The maximum value of V_{IH} of P00 and P01 is V_{DD} even in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port.

2.3.2 Supply current characteristics

(T_A = -40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current ^{Note 1}	I _{DD1}	Operating mode	Basic operation	f _{IH} = 20 MHz	V _{DD} = 3.0 V, 5.0 V		0.91		mA
				Normal operation	f _{IH} = 20 MHz	V _{DD} = 3.0 V, 5.0 V		1.57	
			f _{IH} = 5 MHz		V _{DD} = 3.0 V, 5.0 V		0.85	1.15	
	I _{DD2} ^{Note 2}	HALT mode	f _{IH} = 20 MHz	V _{DD} = 3.0 V, 5.0 V		350	820	μA	
			f _{IH} = 5 MHz	V _{DD} = 3.0 V, 5.0 V		290	600		
	I _{DD3} ^{Note 3}	STOP mode	V _{DD} = 3.0 V			0.56	2.00	μA	
WDT supply current ^{Note 4}	I _{WDT}	f _{IL} = 15 kHz					0.31		μA
ADC supply current ^{Note 5}	I _{ADC}	During conversion at the highest speed	V _{DD} = 5.0 V			1.30	1.90	mA	
			V _{DD} = 3.0 V			0.50			

- Notes**
1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the watchdog timer, A/D converter, I/O port, and on-chip pull-up/pull-down resistors.
 2. During HALT instruction execution by flash memory.
 3. When the high-speed on-chip oscillator is stopped.
 4. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.
 5. Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

- Remarks**
1. f_{IL}: Low-speed on-chip oscillator clock frequency
 2. f_{IH}: High-speed on-chip oscillator clock frequency
 3. Temperature condition of the TYP. value is T_A = 25°C

(2) CSI mode (master mode, SCKp... internal clock output)**(T_A = -40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK}				
		2.7 V ≤ V _{DD} ≤ 5.5 V	200			ns
		2.0 V ≤ V _{DD} ≤ 5.5 V	800			ns
SCKp high-/low-level width	t _{KH1} , t _{KL1}	2.7 V ≤ V _{DD} ≤ 5.5 V	t _{KCY1} /2-18			ns
		2.0 V ≤ V _{DD} ≤ 5.5 V	t _{KCY1} /2-50			ns
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK1}	2.7 V ≤ V _{DD} ≤ 5.5 V	47			ns
		2.0 V ≤ V _{DD} ≤ 5.5 V	110			ns
Slp hold time (from SCKp↑) ^{Note 2}	t _{SH1}		19			ns
Delay time from SCKp↓ to SOp output ^{Note 3}	t _{KSO1}	C = 30 pF ^{Note 4}			25	ns

- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 4. C is the load capacitance of the SCKp and SOp output lines.

- Remarks**
1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0)
 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

(3) CSI mode (slave mode, SCKp... external clock input)**($T_A = -40$ to $+85^\circ\text{C}$, $2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY2}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$f_{MCK} = 20\text{ MHz}$	$8/f_{MCK}$			ns
			$f_{MCK} \leq 10\text{ MHz}$	$6/f_{MCK}$			ns
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$		$6/f_{MCK}$			ns
SCKp high-/low-level width	t_{KH2} , t_{KL2}	$2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$t_{KCY2}/2$			ns
Slp setup time (to SCKp \uparrow) ^{Note 1}	t_{SIK2}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$1/f_{MCK} + 20$			ns
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$		$1/f_{MCK} + 30$			ns
Slp hold time (from SCKp \uparrow) ^{Note 2}	t_{HSI2}	$2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$1/f_{MCK} + 31$			ns
Delay time from SCKp \downarrow to SOp output ^{Note 3}	t_{KS02}	$C = 30\text{ pF}$ ^{Note 4}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$2/f_{MCK} + 50$	ns
			$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$			$2/f_{MCK} + 110$	ns

- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp \downarrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp \downarrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp \uparrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 4. C is the load capacitance of the SOp output lines.

Remarks 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0)

2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

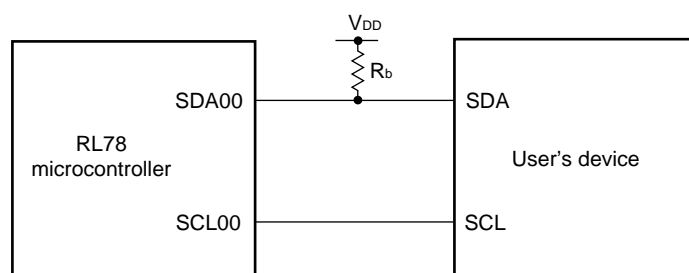
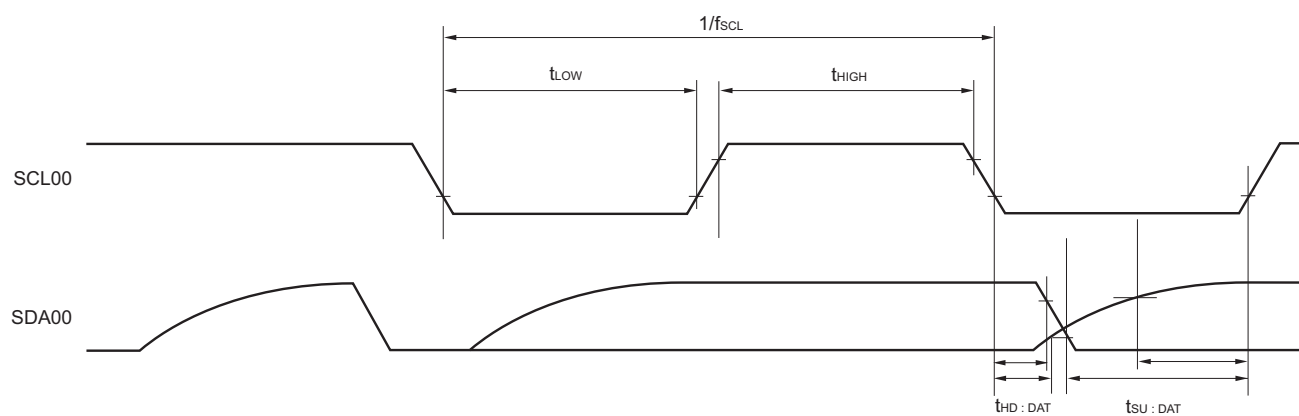
(4) Simplified I²C mode**(T_A = -40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f _{SCL}	2.0 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ		400 ^{Note 1}	kHz
Hold time when SCLr = "L"	t _{LOW}	2.0 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1150		ns
Hold time when SCLr = "H"	t _{HIGH}	2.0 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1150		ns
Data setup time (reception)	t _{SU: DAT}	2.0 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1/f _{MCK} + 145 ^{Note 2}		ns
Data hold time (transmission)	t _{HD: DAT}	2.0 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	0	355	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".**Caution** Select the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin by using the port output mode register 0 (POM0).**Remarks** 1. R_b [Ω]: Communication line (SDAr) pull-up resistance, C_b [F]: Communication line (SCLr, SDAr) load capacitance

2. r: IIC number (r = 00)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

Simplified I²C mode connection diagram**Simplified I²C mode serial transfer timing**

2.6.4 Data retention power supply voltage characteristics

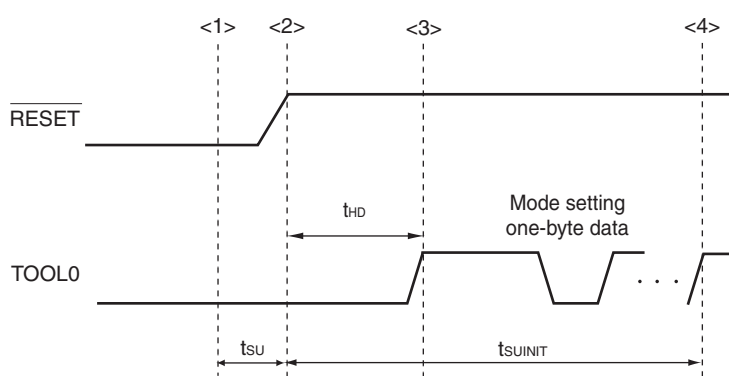
($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage range	V_{DDDR}		1.9		5.5	V

Caution Data is retained until the power supply voltage becomes under the minimum value of the data retention power supply voltage range. Note that data in the RAM and RESF registers might not be cleared even if the power supply voltage becomes under the minimum value of the data retention power supply voltage range.

2.9 Timing of Entry to Flash Memory Programming Modes

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUNIT}	SPOR reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t_{SU}	SPOR reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends	t_{HD}	SPOR reset must end before the external reset ends.	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset ends (SPOR reset must end before the external reset ends.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of entry to the flash memory programming mode by UART reception.

Remark t_{SUNIT} : The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

t_{SU} : How long from when the TOOL0 pin is placed at the low level until an external reset ends (MIN. 10 μs)

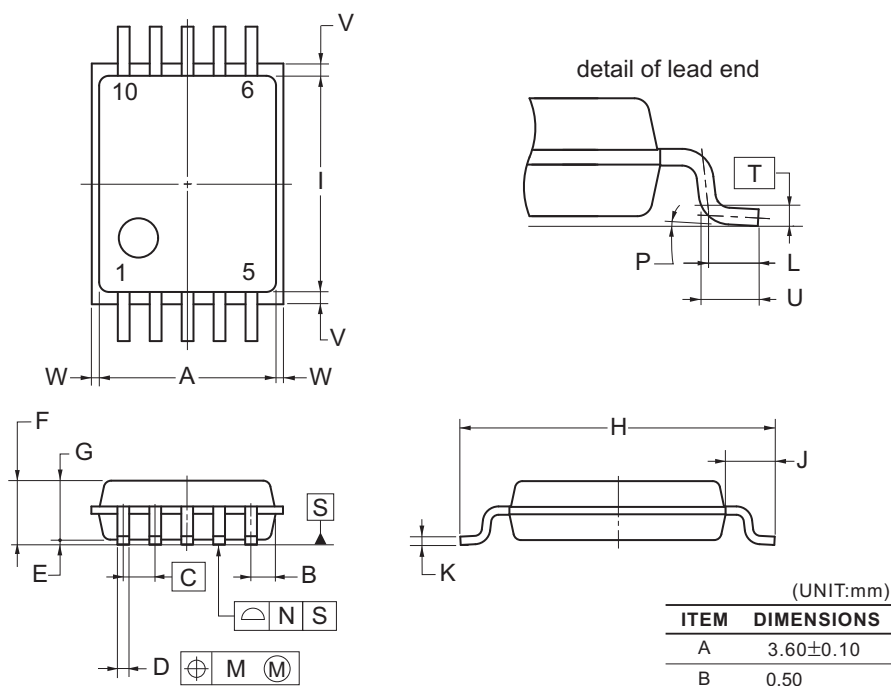
t_{HD} : How long to keep the TOOL0 pin at the low level from when the external reset ends

3. PACKAGE DRAWINGS

3.1 10-pin products

R5F10Y16ASP, R5F10Y14ASP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP10-4.4x3.6-0.65	PLSP0010JA-A	P10MA-65-CAC-2	0.05



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

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Revision History	RL78/G10 Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	Apr 15, 2013	-	First Edition issued

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NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.