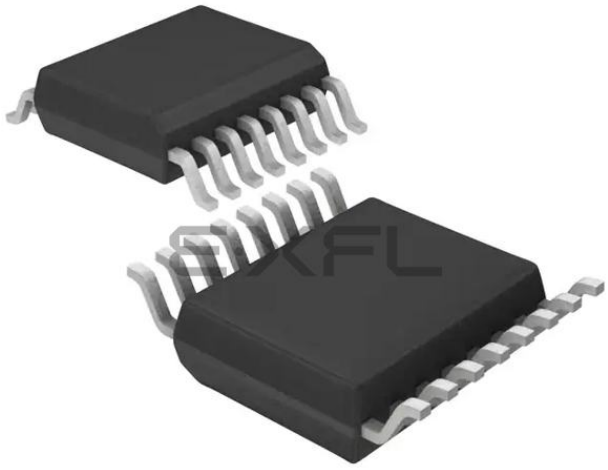
Renesas Electronics America Inc - R5F10Y47DSP#30 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	20MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	10
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 7x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SSOP (0.173", 4.40mm Width)
Supplier Device Package	16-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10y47dsp-30

○ ROM, RAM capacities

Flash ROM	RAM	10 pins	16 pins
4 KB	512 B	–	R5F10Y47ASP Note 2
2 KB	256 B	R5F10Y16ASP	R5F10Y46ASP Note 2
1 KB	128 B	R5F10Y14ASP	R5F10Y44ASP Note 2

Notes 1. 16-pin products only

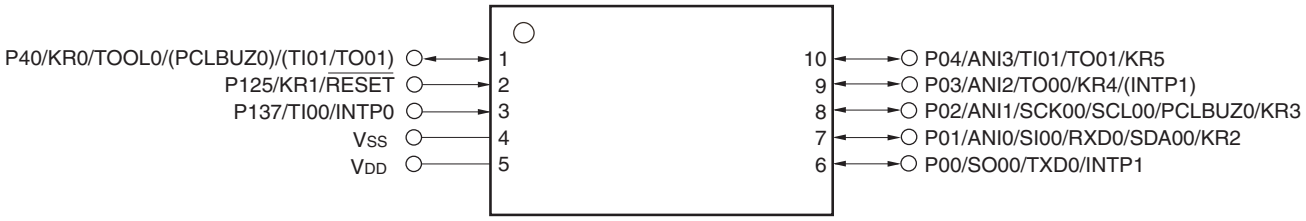
2. Under development

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

1.3 Pin Configuration (Top View)

1.3.1 10-pin products

- 10-pin plastic LSSOP (4.4 × 3.6)

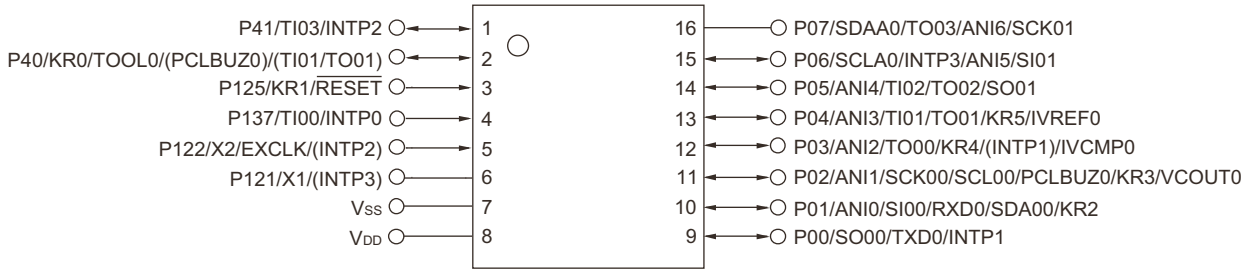


Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.2 16-pin products

- 16-pin plastic SSOP (4.4 × 5.0)



Remarks 1. For pin identification, see **1.4 Pin Identification**.

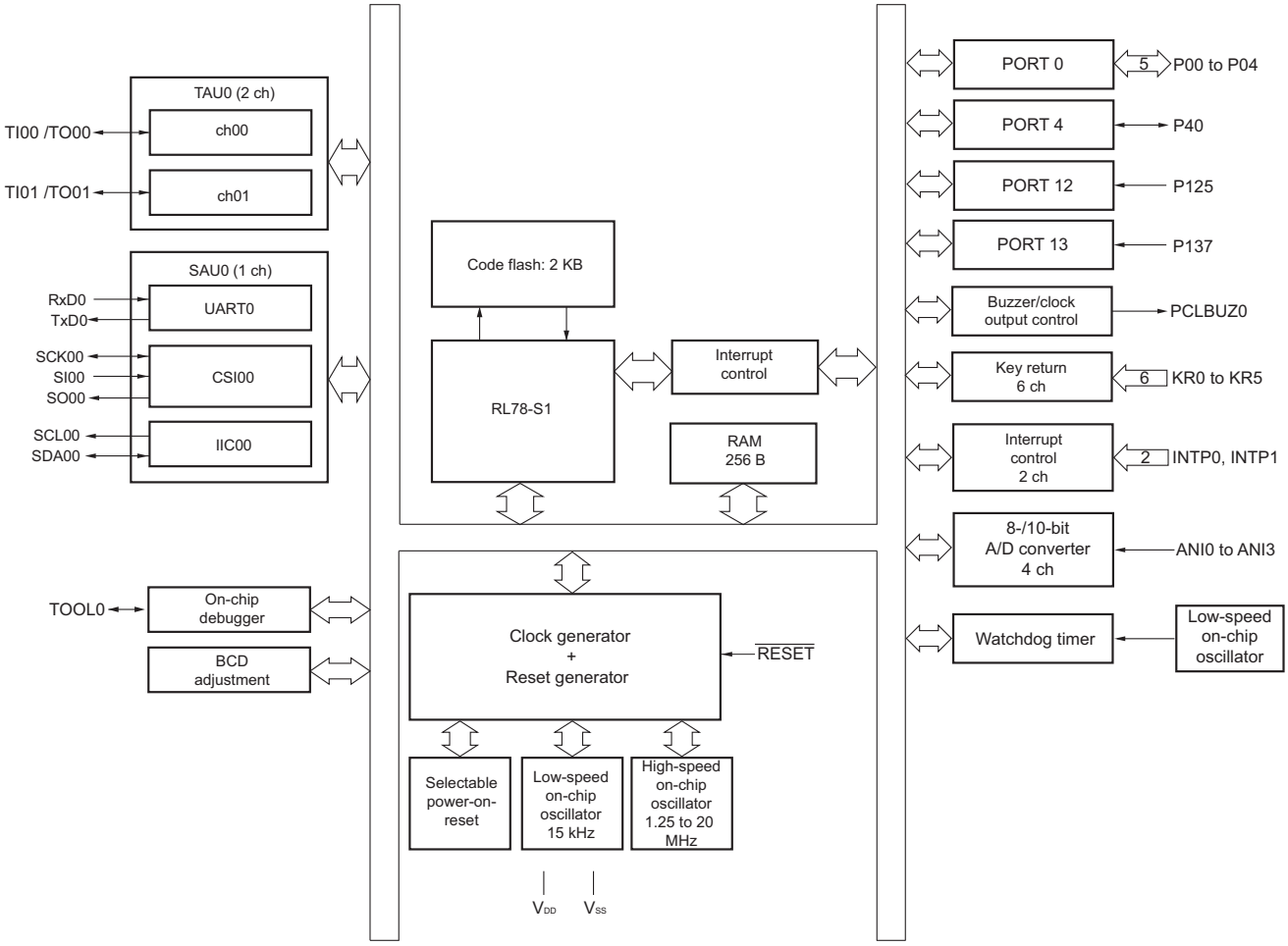
2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.4 Pin Identification

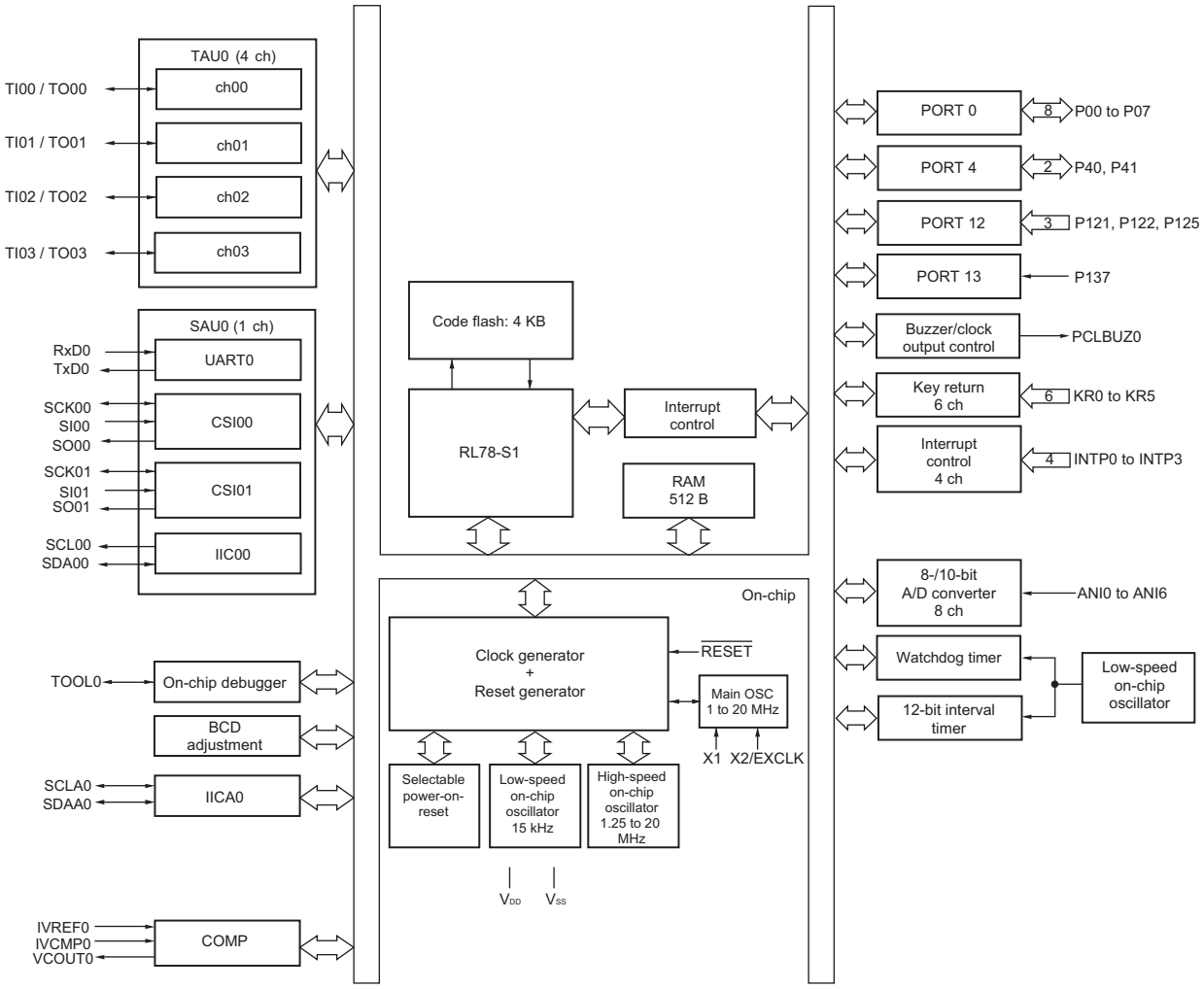
ANI0 to ANI6 : Analog Input
INTP0 to INTP3 : External Interrupt Input
KR0 to KR5 : Key Return
P00 to P07 : Port 0
P40, P41 : Port 4
P121, P122, P125 : Port 12
P137 : Port 13
PCLBUZ0 : Programmable Clock Output/ Buzzer Output
EXCLK : External Clock Input
X1, X2 : Crystal Oscillator
IVCMP0 : Comparator Input
VCOUT0 : Comparator Output
IVREF0 : Comparator Reference Input
$\overline{\text{RESET}}$: Reset
RxD0 : Receive Data
SCK00, SCK01 : Serial Clock Input/Output
SCL00, SCLA0 : Serial Clock Output
SDA00, SDAA0 : Serial Data Input/Output
SI00, SI01 : Serial Data Input
SO00, SO01 : Serial Data Output
TI00 to TI03 : Timer Input
TO00 to TO03 : Timer Output
TOOL0 : Data Input/Output for Tool
TxD0 : Transmit Data
V_{DD} : Power Supply
V_{SS} : Ground

1.5 Block Diagram

1.5.1 10-pin products



1.5.2 16-pin products



2.1 Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbols	Conditions		Ratings	Unit
Supply Voltage	V_{DD}			−0.5 to +6.5	V
Input Voltage	V_{I1}			−0.3 to V_{DD} + 0.3[Note]	V
Output Voltage	V_{O1}			−0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH1}	Per pin		−40	mA
		Total of all pins -140 mA	P40	−40	mA
			P00 to P04	−100	mA
Output current, low	I_{OL1}	Per pin		40	mA
		Total of all pins 140 mA	P40	40	mA
			P00 to P04	100	mA
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

Note Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. The reference voltage is V_{SS}.

2.2 Oscillator Characteristics

2.2.1 On-chip oscillator characteristics

(T_A = −40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator oscillation clock frequency [Notes 1, 2]	f_{IH}		1.25		20	MHz
High-speed on-chip oscillator oscillation clock frequency accuracy		T_A = -20 to +85°C	-2.0		+2.0	%
		T_A = -40 to -20°C	-3.0		+3.0	%
Low-speed on-chip oscillator oscillation clock frequency [Note 3]	f_{IL}			15		kHz
Low-speed on-chip oscillator oscillation clock frequency accuracy			-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 2 of option byte (000C2H).

2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

3. This only indicates the oscillator characteristics.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	P00, P01, P02 to P04, P40	Per pin				-10.0[Note 2]	mA
		P40	Total[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			-10.0	mA
				2.7 V ≤ V_{DD} < 4.0 V			-2.0	mA
				2.0 V ≤ V_{DD} < 2.7 V			-1.5	mA
		P00, P01, P02 to P04	Total[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			-50.0	mA
				2.7 V ≤ V_{DD} < 4.0 V			-10.0	mA
				2.0 V ≤ V_{DD} < 2.7 V			-7.5	mA
		Total of all pins[Note 3]					-60.0	mA
Output current, low[Note 4]	I_{OL1}	P00 to P04, P40	Per pin				20.0[Note 2]	mA
		P40	Total[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			20.0	mA
				2.7 V ≤ V_{DD} < 4.0 V			3.0	mA
				2.0 V ≤ V_{DD} < 2.7 V			0.6	mA
		P00 to P04	Total[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			80.0	mA
				2.7 V ≤ V_{DD} < 4.0 V			12.0	mA
				2.0 V ≤ V_{DD} < 2.7 V			2.4	mA
		Total of all pins[Note 3]					100.0	mA
Input voltage, high	V_{IH1}				0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}				0		0.2 V_{DD}	V
Output voltage, high[Note 5]	V_{OH1}	4.0 V ≤ V_{DD} ≤ 5.5 V		I_{OH} = -10 mA	V_{DD}-1.5			V
				I_{OH} = -3.0 mA	V_{DD}-0.7			V
		2.7 V ≤ V_{DD} ≤ 5.5 V		I_{OH} = -2.0 mA	V_{DD}-0.6			V
		2.0 V ≤ V_{DD} ≤ 5.5 V		I_{OH} = -1.5 mA	V_{DD}-0.5			V
Output voltage, low[Note 6]	V_{OL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		I_{OL} = 20 mA			1.3	V
				I_{OL} = 8.5 mA			0.7	V
		2.7 V ≤ V_{DD} ≤ 5.5 V		I_{OL} = 3.0 mA			0.6	V
				I_{OL} = 1.5 mA			0.4	V
		2.0 V ≤ V_{DD} ≤ 5.5 V		I_{OL} = 0.6 mA			0.4	V
Input leakage current, high	I_{LIH1}	V_I = V_{DD}					1	μA
Input leakage current,low	I_{LIL1}	V_I = V_{SS}					-1	μA
On-chip pull-up resistance	R_U	V_I = V_{SS}			10	20	100	kΩ

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. Do not exceed the total current value.

3. This is the output current value under conditions where the duty factor ≤ 70%.
The output current value when the duty factor > 70% can be calculated with the following expression (when changing the duty factor to n%).

2.3.2 Supply current characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Basic operation	f_{IH} = 20 MHz	V_{DD} = 3.0 V, 5.0 V		0.91		mA
			Normal operation	f_{IH} = 20 MHz	V_{DD} = 3.0 V, 5.0 V		1.57	2.04	
				f_{IH} = 5 MHz	V_{DD} = 3.0 V, 5.0 V		0.85	1.15	
	I_{DD2} Note 2	HALT mode		f_{IH} = 20 MHz	V_{DD} = 3.0 V, 5.0 V		350	820	µA
				f_{IH} = 5 MHz	V_{DD} = 3.0 V, 5.0 V		290	600	
	I_{DD3} Note 3	STOP mode		V_{DD} = 3.0 V			0.56	2.00	µA
WDT supply current Note 4	I_{WDT}	f_{IL} = 15 kHz					0.31		µA
ADC supply current Note 5	I_{ADC}	During conversion at the highest speed		V_{DD} = 5.0 V			1.30	1.90	mA
				V_{DD} = 3.0 V			0.50		

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the watchdog timer, A/D converter, I/O port, and on-chip pull-up/pull-down resistors.

2. During HALT instruction execution by flash memory.

3. When the high-speed on-chip oscillator is stopped.

4. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.

5. Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. Temperature condition of the TYP. value is T_A = 25°C

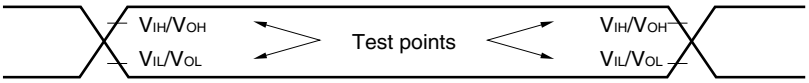
2.4 AC Characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

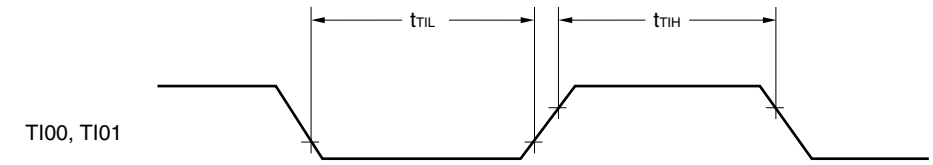
Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	2.7 V ≤ V_{DD} ≤ 5.5 V	0.05		0.8	μs
			2.0 V ≤ V_{DD} ≤ 5.5 V	0.2		0.8	μs
TI00, TI01 input high-level width, low-level width	t_{TIH}, t_{TIL}	Noise filter is not used		1/f_{MCK} + 10			ns
TO00, TO01 output frequency	f_{TO}	4.0 V ≤ V_{DD} ≤ 5.5 V				10	MHz
		2.7 V ≤ V_{DD} < 4.0 V				5	MHz
		2.0 V ≤ V_{DD} < 2.7 V				2.5	MHz
PCLBUZ0 output frequency	f_{PCL}	4.0 V ≤ V_{DD} ≤ 5.5 V				10	MHz
		2.7 V ≤ V_{DD} < 4.0 V				5	MHz
		2.0 V ≤ V_{DD} < 2.7 V				2.5	MHz
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

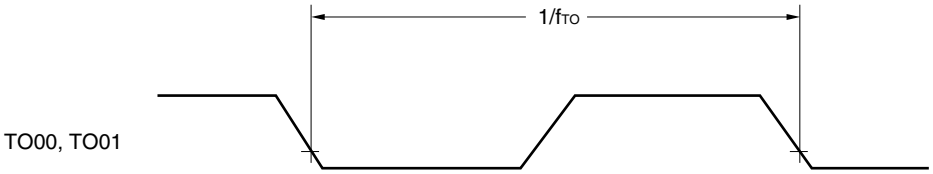
Remark f_{MCK}: Timer array unit operation clock frequency

AC Timing Test Points

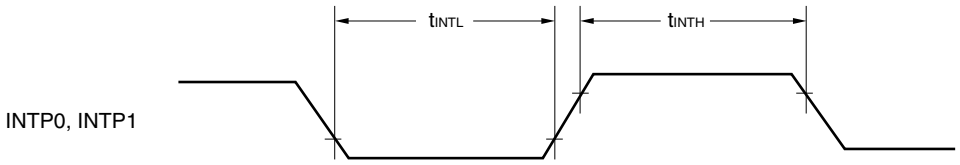


TI/TO Timing

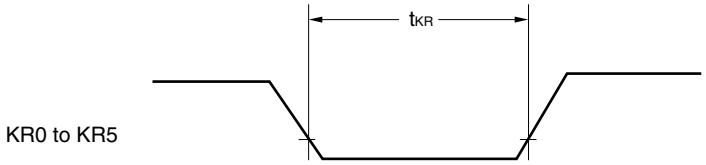




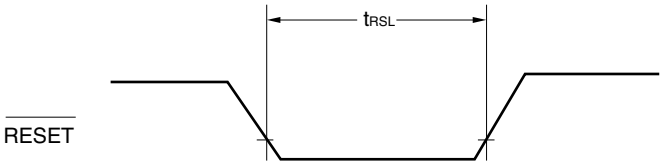
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



2.5 Serial Communication Characteristics

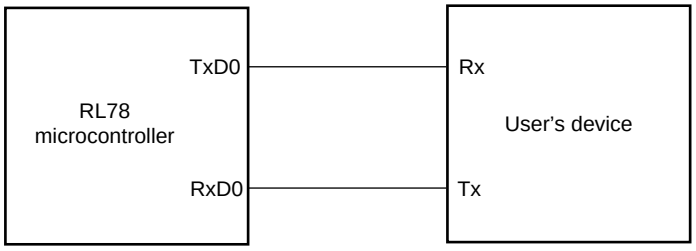
2.5.1 Serial array unit

(1) UART mode

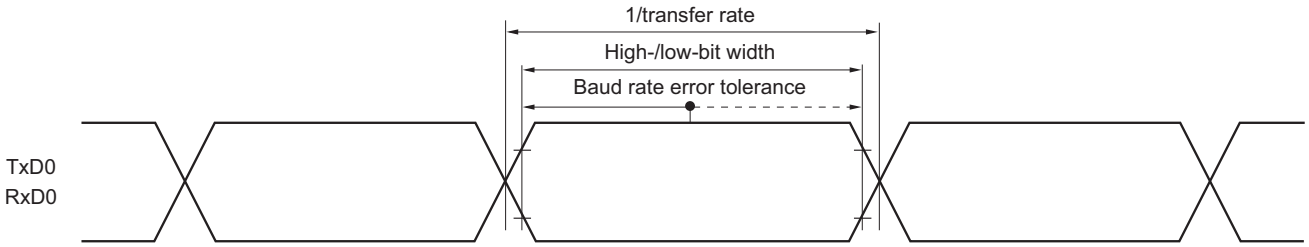
(T_A = −40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{CLK} = f_{MCK} = 20 MHz			3.3	Mbps

UART mode connection diagram



UART mode bit width (reference)



Remark f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

(3) CSI mode (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY2}	2.7 V ≤ V_{DD} ≤ 5.5 V	f_{MCK} = 20 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 10 MHz	6/f_{MCK}			ns
		2.0 V ≤ V_{DD} < 2.7 V		6/f_{MCK}			ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2			ns
SIp setup time (to SCKp↑)[Note 1]	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 20			ns
		2.0 V ≤ V_{DD} < 2.7 V		1/f_{MCK} + 30			ns
SIp hold time (from SCKp↑) [Note 2]	t_{KSI2}	2.0 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 31			ns
Delay time from SCKp↓ to SOp output [Note 3]	t_{KSO2}	C = 30 pF [Note 4]	2.7 V ≤ V_{DD} ≤ 5.5 V			2/f_{MCK} + 50	ns
			2.0 V ≤ V_{DD} < 2.7 V			2/f_{MCK} + 110	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

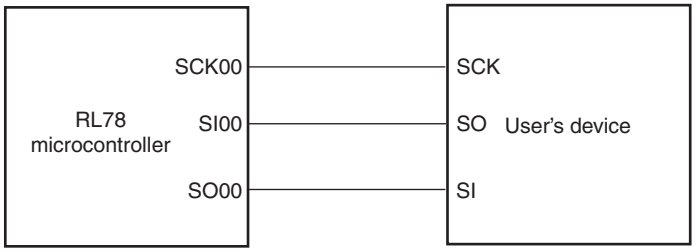
3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SOp output lines.

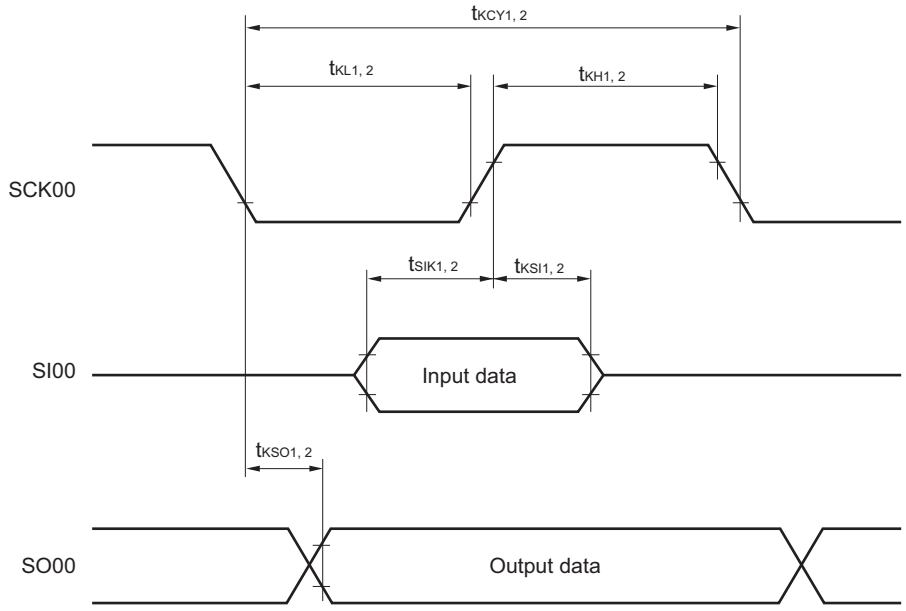
Remarks 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

CSI mode connection diagram



CSI mode serial transfer timing
(When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1.)



(4) Simplified I²C mode

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	2.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1	kHz
Hold time when SCLr = "L"	t_{LOW}	2.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		ns
Hold time when SCLr = "H"	t_{HIGH}	2.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		ns
Data setup time (reception)	$t_{SU:DAT}$	2.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 145 Note 2		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	355	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.

2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin by using the port output mode register 0 (POM0).

Remarks 1. R_b [Ω]: Communication line (SDAr) pull-up resistance, C_b [F]: Communication line (SCLr, SDAr) load capacitance

2. r: IIC number (r = 00)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

(Target ANI pin : ANI0 to ANI3)

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution	V_{DD} = 5 V		±1.7	±3.1[Note 2]	LSB
			V_{DD} = 3 V		±2.3	±4.5[Note 2]	LSB
Conversion time	t_{CONV}	10-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V	3.4		18.4	µs
			2.4 V ≤ V_{DD} ≤ 5.5 V	4.6		18.4	µs
Zero-scale error[Note 1]	E_{ZS}	10-bit resolution	V_{DD} = 5 V			±0.19[Note 2]	%FSR
			V_{DD} = 3 V			±0.39[Note 2]	%FSR
Full-scale error[Note 1]	E_{FS}	10-bit resolution	V_{DD} = 5 V			±0.29[Note 2]	%FSR
			V_{DD} = 3 V			±0.42[Note 2]	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution	V_{DD} = 5 V			±1.8[Note 2]	LSB
			V_{DD} = 3 V			±1.7[Note 2]	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution	V_{DD} = 5 V			±1.4[Note 2]	LSB
			V_{DD} = 3 V			±1.5[Note 2]	LSB
Analog input voltage	V_{AIN}			0		V_{DD}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This is the characteristic evaluation value plus or minus 3. These values are not used in the shipping inspection.

2.6.2 SPOR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection supply voltage	V_{SPOR0}	Power supply rise time	4.08	4.28	4.45	V
		Power supply fall time	4.00	4.20	4.37	V
	V_{SPOR1}	Power supply rise time	2.76	2.90	3.02	V
		Power supply fall time	2.70	2.84	2.96	V
	V_{SPOR2}	Power supply rise time	2.44	2.57	2.68	V
		Power supply fall time	2.40	2.52	2.62	V
	V_{SPOR3}	Power supply rise time	2.05	2.16	2.25	V
		Power supply fall time	2.00	2.11	2.20	V
Minimum pulse width[Note]	T_{SPW}		300			µs

Note Time required for the reset operation by the SPOR when V_{DD} becomes under V_{SPDR}.

2.6.3 Power supply voltage rising slope characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

2.7 Flash Memory Programming Characteristics

(T_A = 0 to + 40°C, 4.5 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Code flash memory rewritable times Notes 1, 2, 3	C_{erwr}	Retained for 20 years.	T_A = + 85°C	1000			Times

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer.

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.8 Dedicated Flash Memory Programmer Communication (UART)

(T_A = 0 to + 40°C, 4.5 V ≤ V_{DD} ≤ 5.5V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate				115,200		bps

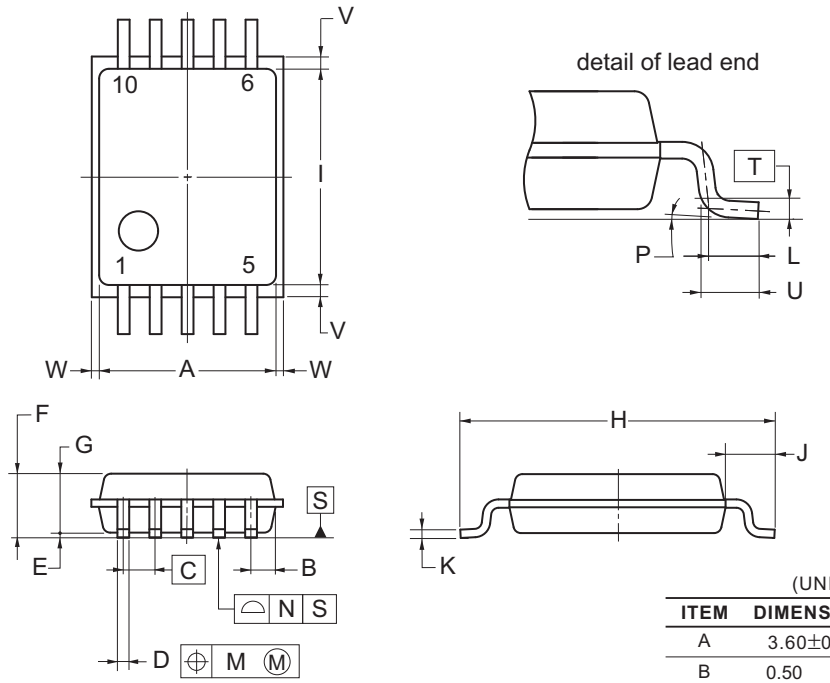
Remark The transfer rate during flash memory programming is fixed to 115,200 bps.

3. PACKAGE DRAWINGS

3.1 10-pin products

R5F10Y16ASP, R5F10Y14ASP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP10-4.4x3.6-0.65	PLSP0010JA-A	P10MA-65-CAC-2	0.05



(UNIT:mm)

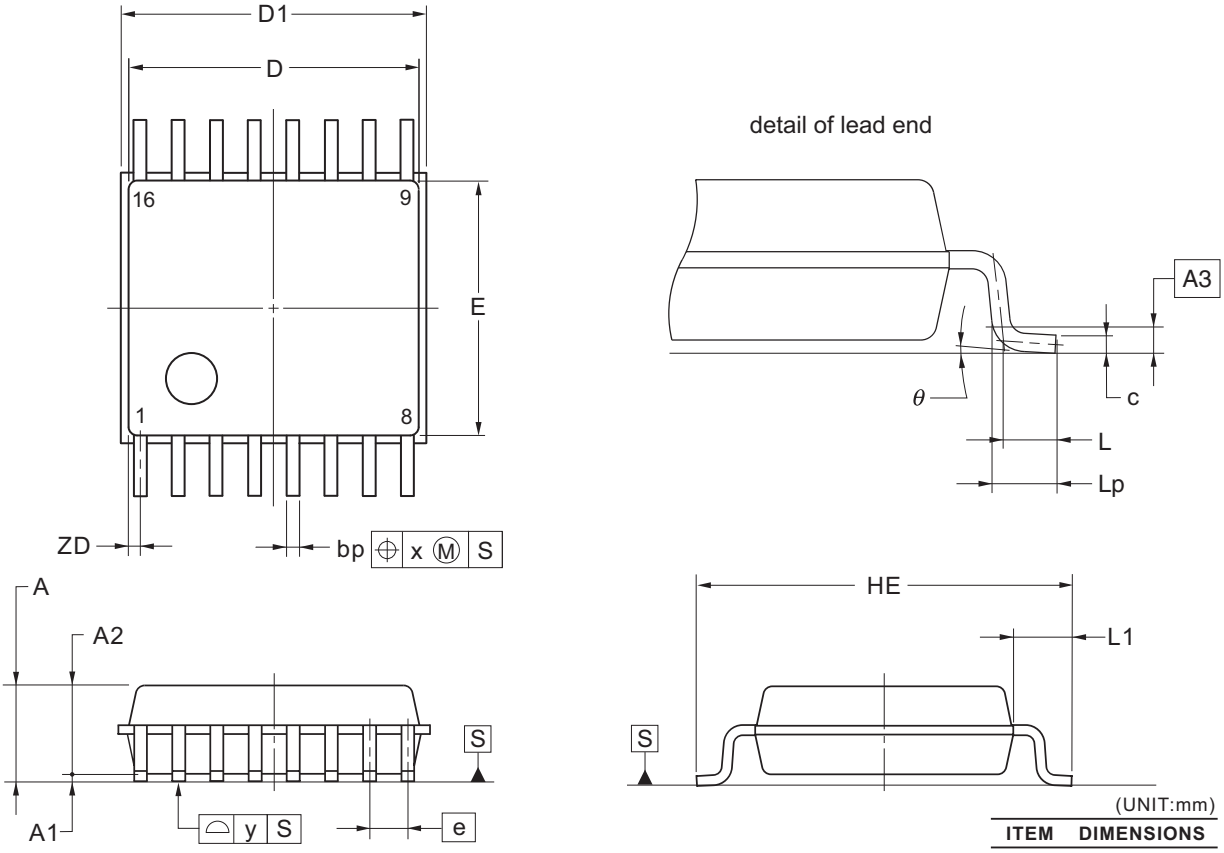
ITEM	DIMENSIONS
A	3.60±0.10
B	0.50
C	0.65 (T.P.)
D	0.24±0.08
E	0.10±0.05
F	1.45 MAX.
G	1.20±0.10
H	6.40±0.20
I	4.40±0.10
J	1.00±0.20
K	$0.17^{+0.08}_{-0.07}$
L	0.50
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25 (T.P.)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

NOTE
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

3.2 16-pin products

R5F10Y47ASP, R5F10Y46ASP, R5F10Y44ASP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-SSOP16-4.4x5-0.65	PRSP0016JC-A	P16MA-65-FAA-2	0.08



(UNIT:mm)

ITEM	DIMENSIONS
D	5.00±0.15
D1	5.20±0.15
E	4.40±0.20
HE	6.40±0.20
A	1.725 MAX.
A1	0.125±0.05
A2	1.50
A3	0.25
e	0.65
bp	$0.22^{+0.08}_{-0.07}$
c	$0.15^{+0.03}_{-0.04}$
L	0.50
Lp	0.60±0.10
L1	1.00±0.20
x	0.13
y	0.10
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
ZD	0.325

Revision History	RL78/G10 Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Apr 15, 2013	-	First Edition issued

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