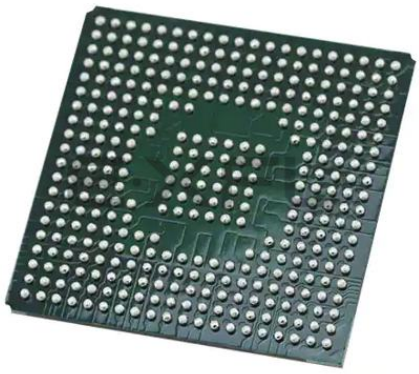


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	Math Engine; MaverickCrunch™
RAM Controllers	SDRAM
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	1/10/100Mbps (1)
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Hardware ID
Package / Case	352-BBGA
Supplier Device Package	352-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep9315-cb

OVERVIEW

The EP9315 is an ARM920T-based system-on-a-chip design with a large peripheral set targeted to a variety of applications:

- Thin Client Computers for Business and Home
- Internet Radio
- Internet Access Devices
- Industrial Computers
- Specialized Terminals
- Point-of-sale Terminals
- Test and Measurement Equipment

The ARM920T microprocessor core with separate 16-kbyte, 64-way set-associative instruction and data caches is augmented by the MaverickCrunch™ co-processor, enabling high-speed floating point calculations.

MaverickKey™ unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

A high-performance 1/10/100-Mbps Ethernet media access controller (EMAC) is included along with external interfaces to SPI, I^2S audio, Raster/LCD, IDE storage peripherals, keypad, and touchscreen. A three-port USB 2.0 Full Speed Host (OHCI) (12 Mbits per second) and three UARTs are included as well.

The EP9315 is a high-performance, low-power, RISC-based, single-chip computer built around an ARM920T microprocessor core with a maximum operating clock rate of 200 MHz (184 MHz for industrial conditions). The ARM core operates from a 1.8 V supply, while the I/O operates at 3.3 V with power usage between 100 mW and 750 mW (dependent on speed).

Table A. Change History

Revision	Date	Changes
PP1	January 2004	Initial Release.
PP2	July 2004	Update AC data. Add ADC data.
PP3	Febuary 2005	Update electrical characteristics based upon more complete characterization data.
PP4	March 2005	Minor correction to block diagram on page 1. DD7 changed to pull down.

List of Figures

- Timing and interface signals for digital LCD and TFT displays
- Full programmability for either non-interlaced or dual-scan color and grayscale flat panel displays
- Dedicated data path to SDRAM controller for improved system performance
- Pixel depths of 4, 8, 16, or 24 bits per pixel or 256 levels of grayscale
- Hardware Cursor up to 64 x 64 pixels
- 256 x 18 Color Lookup Table
- Hardware Blinking
- 8-bit interface to low end panel

Table F. LCD Interface Pin Assignments

Pin Mnemonic	Pin Description
SPCLK	Pixel Clock
P[17:0]	Pixel Data Bus [17:0]
HSYNC / LP	Horizontal Synchronization / Line Pulse
VCSYNC / FP	Vertical or Composite Synchronization / Frame Pulse
BLANK	Composite Blank
BRIGHT	Pulse Width Modulated Brightness

Graphics Accelerator

The EP9315 contains a hardware graphics acceleration engine that improves graphic performance by handling block copy, block fill and hardware line draw operations. The Graphics Accelerator is used in the system to off-load graphics operations from the processor.

Pixel depths supported by the Graphics Accelerator are 4, 8, 16 or 24 bits per pixel. The 24 bits per pixel mode can be operated as packed (4 pixels every 3 words) or unpacked (1 pixel per word with the high byte unused.)

The block copy operations of the Graphics Accelerator are similar to a DMA (Direct Memory Access) transfer that understands pixel organization, block width, transparency, and transformation from 1bpp to higher 4, 8, 16 or 24bpp.

The line draw operations also allow for solid lines or dashed lines. The colors for line drawing can be either foreground color and background color or foreground color with the background being transparent.

Touch Screen Interface with 12-bit Analog-to-digital Converter (ADC)

The touch screen interface performs all sampling, averaging, ADC range checking, and control for a wide variety of analog resistive touch screens. This controller only interrupts the processor when a meaningful change occurs. The touch screen hardware may be disabled and the switch matrix and ADC controlled directly if desired. Features include:

- Support for 4-, 5-, 7-, or 8-wire analog resistive touch screens.
- Flexibility - unused lines may be used for temperature sensing or other functions.
- Touch screen interrupt function.

Table G. Touch Screen Interface with 12-bit Analog-to-Digital Converter Pin Assignments

Pin Mnemonic	Pin Description
Xp, Xm	Touch screen ADC X Axis
Yp, Ym	Touch screen ADC Y Axis
SXp, SXm	Touch screen ADC X Axis Voltage Feedback
SYp, SYm	Touch screen ADC Y Axis Voltage Feedback

64-Key Keypad Interface

The keypad circuitry scans an 8 x 8 array of 64 normally open, single-pole switches. Any one or two keys depressed will be de-bounced and decoded. An interrupt is generated whenever a stable set of depressed keys is detected. If the keypad is not utilized, the 16 column/row pins may be used as general purpose I/O. The Keypad interface:

- Provides scanning, debounce, and decoding for a 64-key switch array.
- Scans an 8-row by 8-column matrix.
- May decode 2 keys at once.
- Generates an interrupt when a new stable key is determined.
- Also generates a 3-key reset interrupt.

Table H. 64-Key Keypad Interface Pin Assignments

Pin Mnemonic	Pin Description	Alternative Usage
COL[7:0]	Key Matrix Column Inputs	General Purpose I/O
ROW[7:0]	Key Matrix Row Inputs	General Purpose I/O

Table P. General Purpose Input/Output Pin Assignment

Pin Mnemonic	Pin Name - Description
EGPIO[15:0]	Expanded General Purpose Input / Output Pins with Interrupts
FGPIO[7:0]	Expanded General Purpose Input / Output Pins with Interrupts

Note: Port F defaults as PCMCIA pins. Port F must be configured by software to be used as GPIO.

Reset and Power Management

The chip may be reset through the PRSTn pin or through the open drain common reset pin, RSTOn.

Clocks are managed on a peripheral-by-peripheral basis and may be turned off to conserve power.

The processor clock is dynamically adjustable from 0 to 200 MHz (184 MHz for industrial conditions).

Table Q. Reset and Power Management Pin Assignments

Pin Mnemonic	Pin Name - Description
PRSTn	Power On Reset
RSTOn	User Reset In/Out – Open Drain – Preserves Real Time Clock value

Hardware Debug Interface

The JTAG interface allows use of ARM's Multi-ICE or other in-circuit emulators.

Note: The JTAG interface does not support boundary scan.

Table R. Hardware Debug Interface

Pin Mnemonic	Pin Name - Description
TCK	JTAG Clock
TDI	JTAG Data In
TDO	JTAG Data Out
TMS	JTAG Test Mode Select
TRSTn	JTAG Port Reset

Internal Boot ROM

The Internal 16-kbyte ROM allows booting from FLASH memory, SPI or UART. Consult the EP93xx User's Manual for operational details

12-channel DMA Controller

The DMA module contains 12 separate DMA channels. Ten of these may be used for peripheral-to-memory or memory-to-peripheral access. Two of these are dedicated to memory-to-memory transfers. Each DMA channel is connected to the 16-bit DMA request bus.

The request bus is a collection of requests, Serial Audio, and UARTs. Each DMA channel can be used independently or dedicated to any request signal. For each DMA channel, source and destination addressing can be independently programmed to increment, decrement, or stay at the same value. All DMA addresses are physical, not virtual addresses.

PCMCIA Interface

The EP9315 has a single PCMCIA port which can be used to access either 8 or 16-bit devices.

Table S. PCMCIA Interface

Pin Mnemonic	Pin Name - Description
VS1	Voltage sense
VS2	Voltage sense
MCD1	Card detect
MCD2	Card detect
MCBVD1	Voltage detection / status change
MCBVD2	Voltage detection
MCDIR	Data transceiver direction control
MCDAENn	Data bus transceiver enable
MCADENn	Address bus transceiver enable
MCREGn	Memory card register
MCEHn	Memory card high byte select
MCELn	Memory card low byte select
IORDn	I/O card read
IOWRn	I/O card write
MCRDn	Memory card read
MCWRn	Memory card write
READY	Ready / interrupt
WP	Write protect
MCWAITn	Wait Input
MCRESETn	Card reset

Memory Interface

Figure 2 through Figure 5 define the timings associated with all phases of the SDRAM. The following table contains the values for the timings of each of the SDRAM modes.

Parameter	Symbol	Min	Typ	Max	Unit
SDCLK high time	t_{clk_high}	-	$(t_{HCLK}) / 2$	-	ns
SDCLK low time	t_{clk_low}	-	$(t_{HCLK}) / 2$	-	ns
SDCLK rise/fall time	t_{clkrf}	-	2	4	ns
Signal delay from SDCLK rising edge time	t_d	-	-	8	ns
Signal hold from SDCLK rising edge time	t_h	1	-	-	ns
DQMn delay from SDCLK rising edge time	t_{DQd}	-	-	8	ns
DQMn hold from SDCLK rising edge time	t_{DQh}	1	-	-	ns
DA valid setup to SDCLK rising edge time	t_{DAs}	2	-	-	ns
DA valid hold from SDCLK rising edge time	t_{DAh}	3	-	-	ns

SDRAM Load Mode Register Cycle

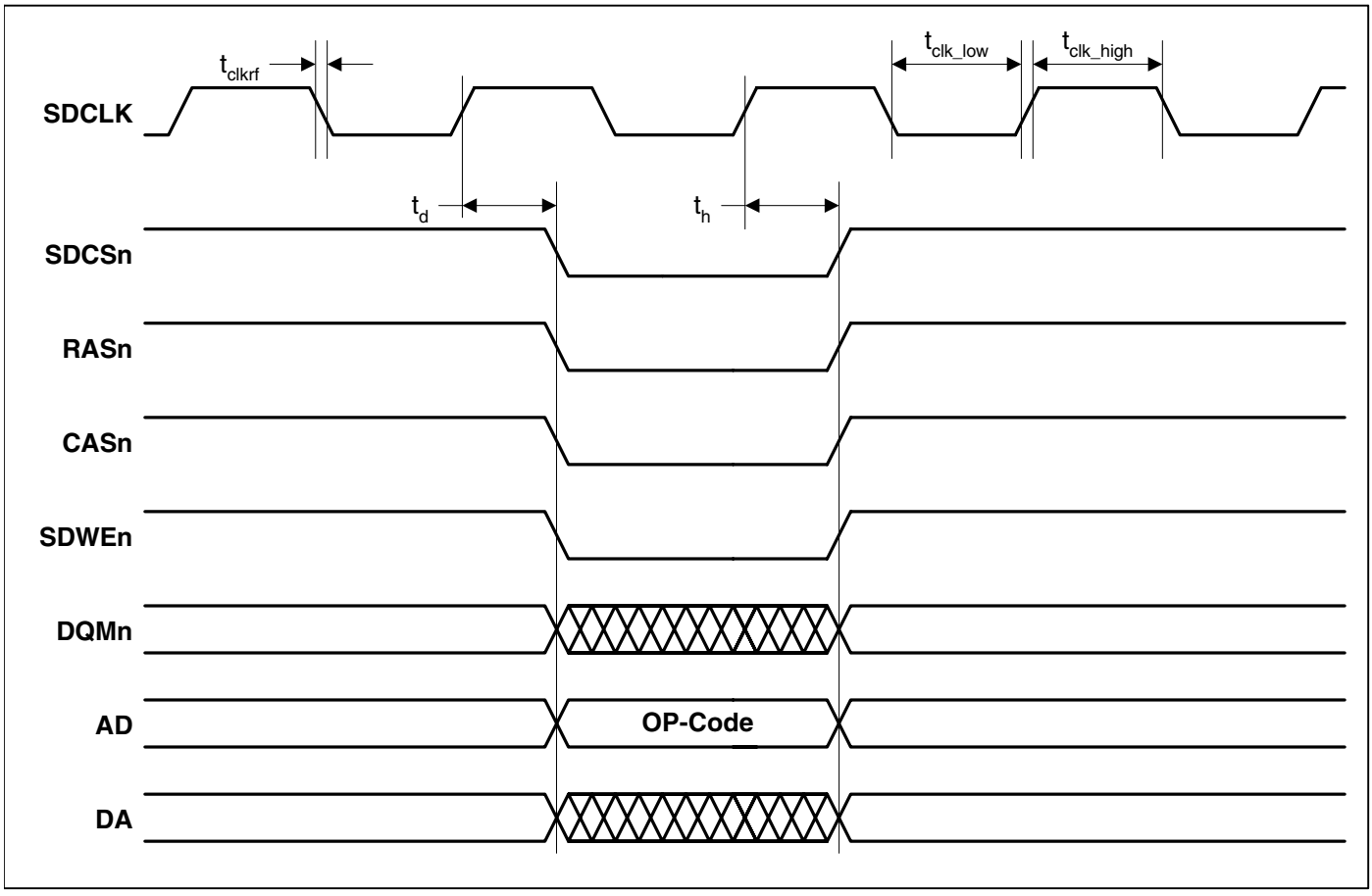


Figure 2. SDRAM Load Mode Register Cycle Timing Measurement

SDRAM Burst Write Cycle

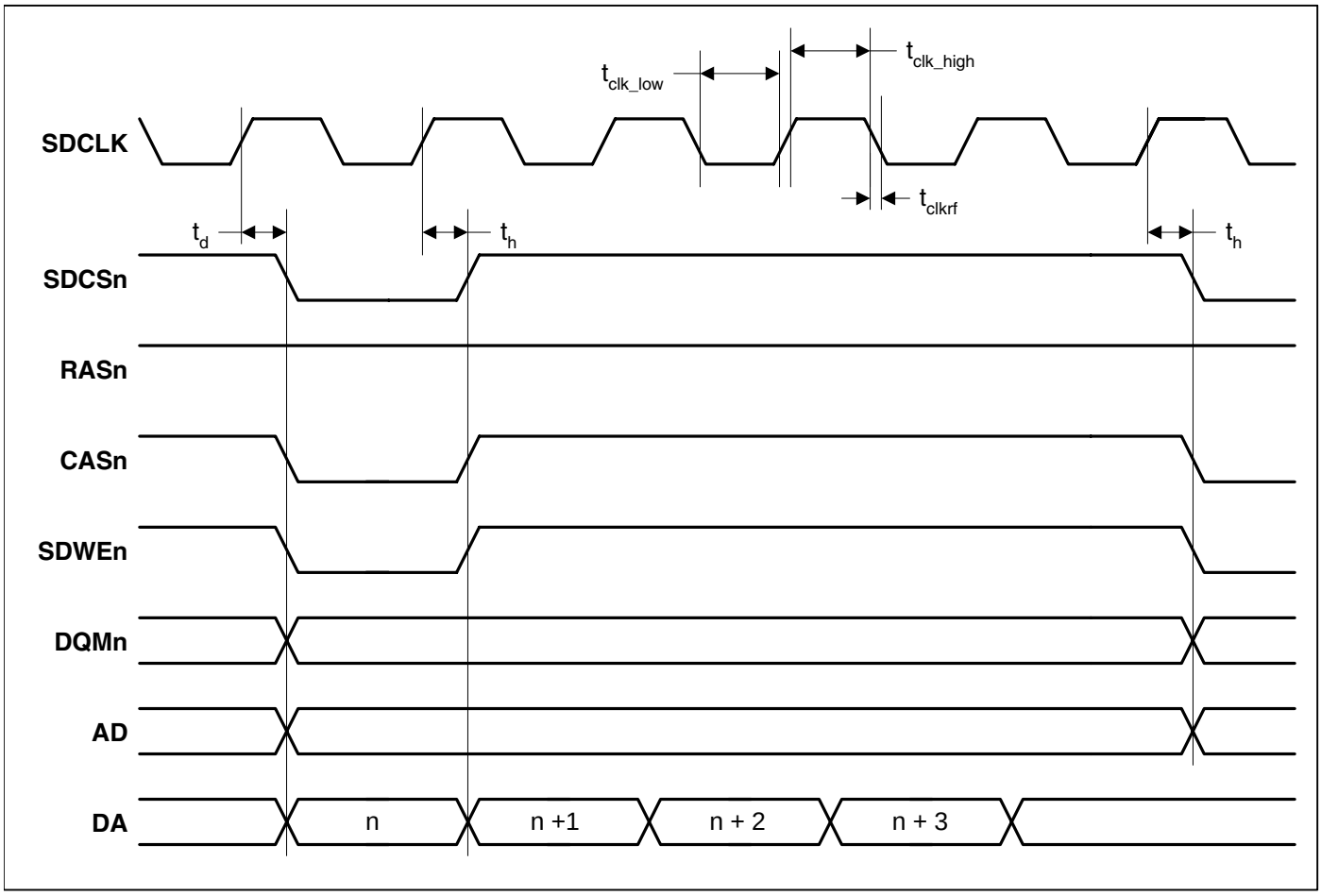


Figure 4. SDRAM Burst Write Cycle Timing Measurement

Static Memory Single Word Read Cycle

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to CSn assert time	t_{ADs}	0	-	-	ns
AD hold from CSn deassert time	t_{ADh}	t_{HCLK}	-	-	ns
RDn assert time	t_{RDpw}	-	$t_{HCLK} \times (WST1 + 2)$	-	ns
CSn to RDn delay time	t_{RDd}	-	-	3	ns
CSn assert to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DA setup to RDn deassert time	t_{DAs}	$t_{HCLK} + 12$	-	-	ns
DA hold from RDn deassert time	t_{DAh}	0	-	-	ns

See “Timing Conditions” on page 14 for definition of HCLK.

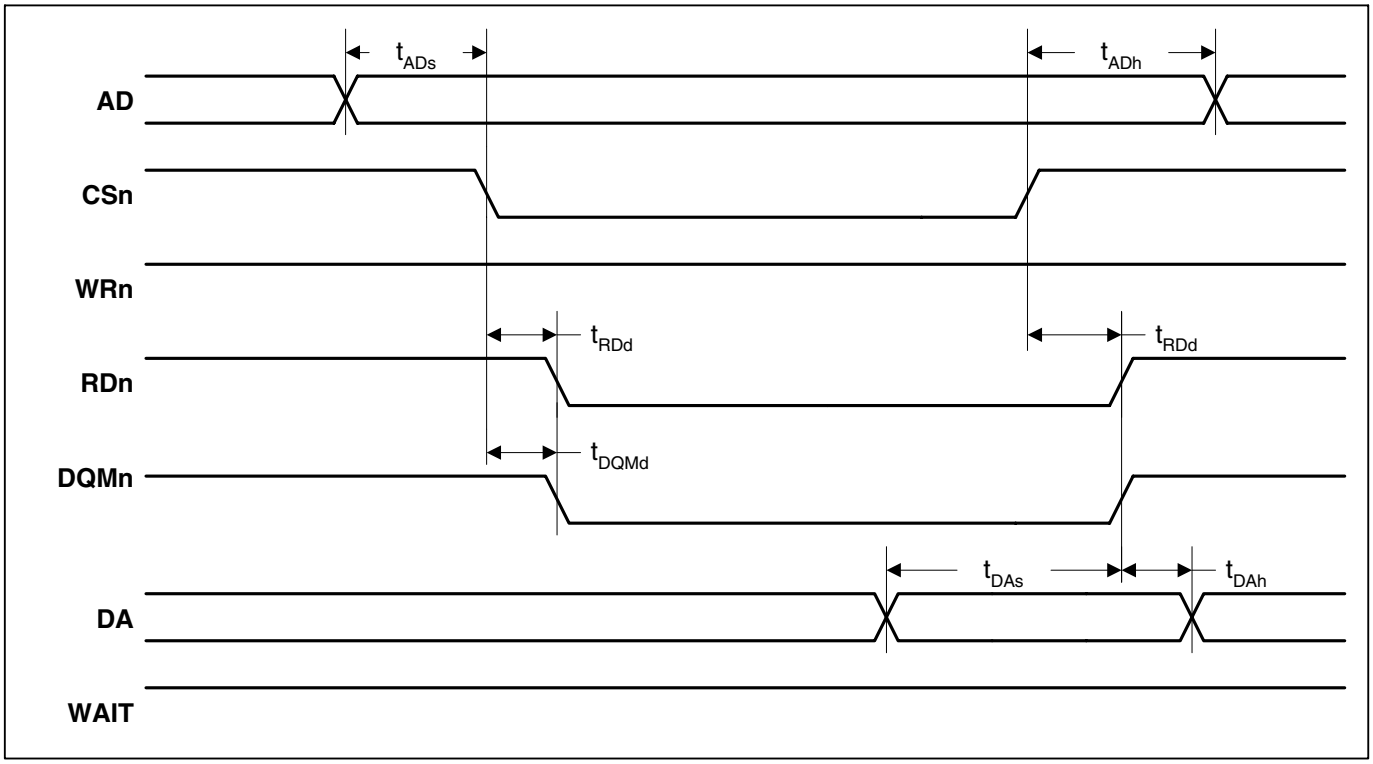


Figure 6. Static Memory Single Word Read Cycle Timing Measurement

Static Memory Single Word Write Cycle

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	t_{HCLK} - 3	-	-	ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$	-	-	ns
WRn deassert to CSn deassert time	t_{CSh}	7	-	-	ns
CSn to WRn assert delay time	t_{WRd}	-	-	2	ns
WRn assert time	t_{WRpw}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
WRn deassert to DA transition time	t_{DAh}	t_{HCLK}	-	-	ns
WRn assert to DA valid	t_{DAV}	-	-	8	ns

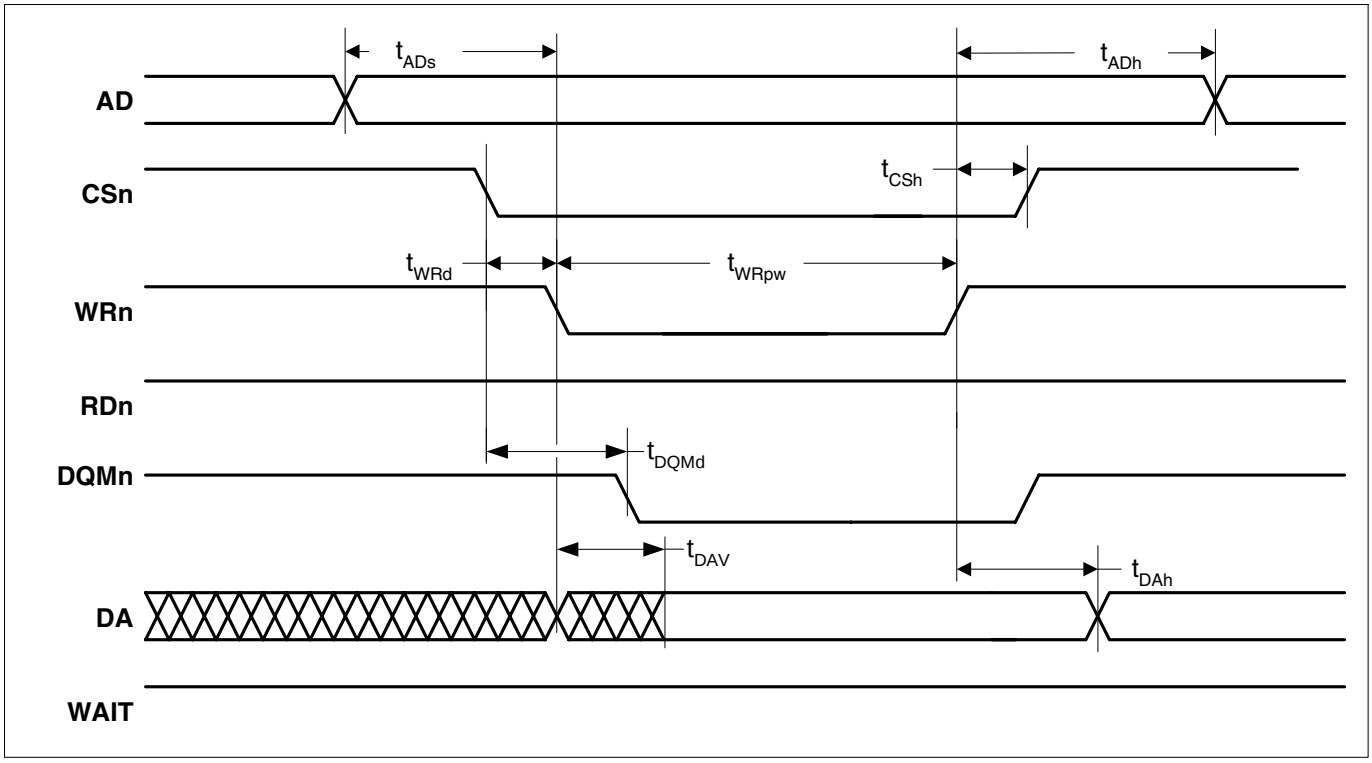


Figure 7. Static Memory Single Word Write Cycle Timing Measurement

Static Memory Burst Write Cycle

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	$t_{HCLK} - 3$			ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$			ns
WRN/DQMn deassert to AD transition time	t_{ADd}			$t_{HCLK} + 6$	ns
CSn hold from WRn deassert time	t_{CSh}	7			ns
CSn to WRn assert delay time	t_{WRd}			2	ns
CSn to DQMn assert delay time	t_{DQMd}			1	ns
DQMn assert time	t_{DQpwL}		$t_{HCLK} \times (WST1 + 1)$		ns
DQMn deassert time	t_{DQpwH}			$(t_{HCLK} \times 2) + 14$	ns
WRn assert time	t_{WRpwL}		$t_{HCLK} \times (WST1 + 11)$		ns
WRn deassert time	t_{WRpwH}			$(t_{HCLK} \times 2) + 7$	ns
WRn/DQMn deassert to DA transition time	t_{DAh}	t_{HCLK}			ns
WRn/DQMn assert to DA valid time	t_{DAv}			8	ns

Note: These characteristics are valid when the Page Mode Enable (Burst Mode) bit is set. See the User's Guide for details.

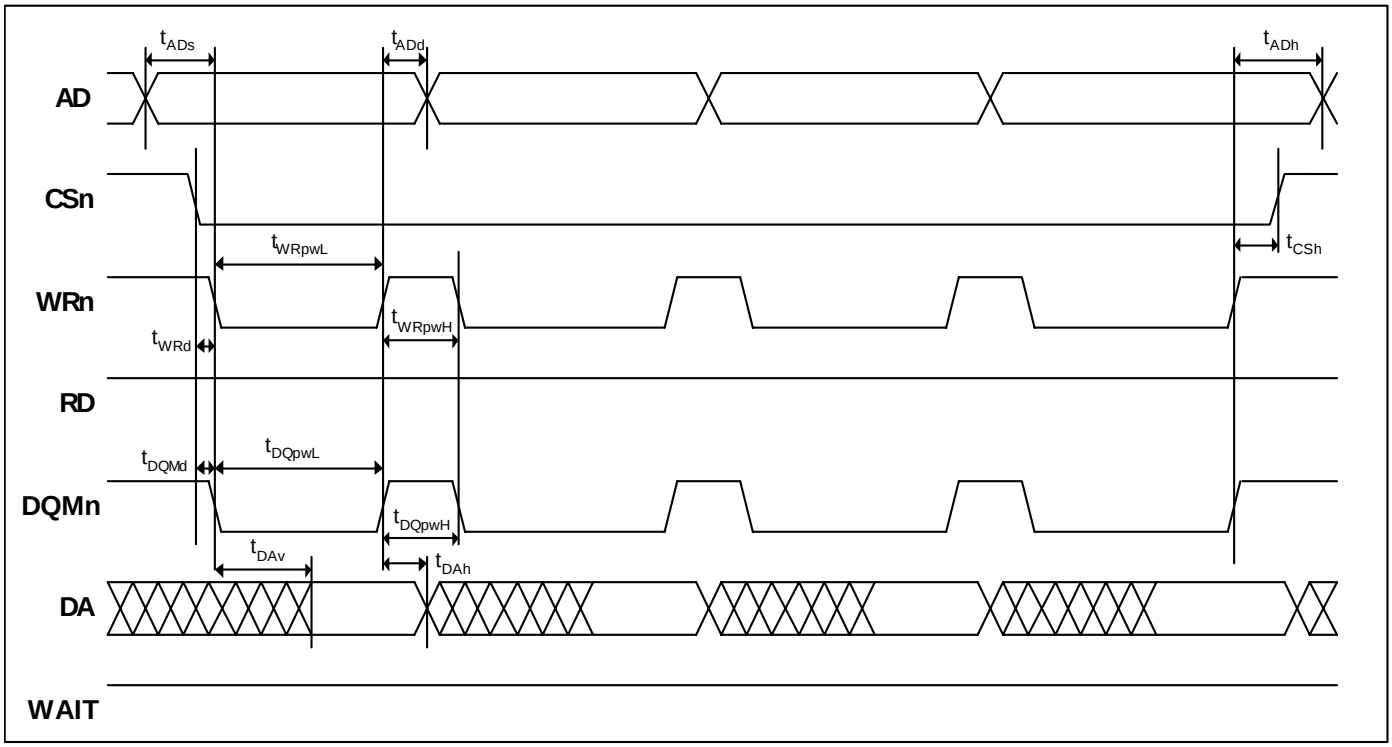


Figure 13. Static Memory Burst Write Cycle Timing Measurement

Static Memory Single Read Wait Cycle

Parameter	Symbol	Min	Typ	Max	Unit
CSn assert to WAIT time	t_{WAITd}	-	-	$t_{HCLK} \times (WST1-2)$	ns
WAIT assert time	t_{WAITpw}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 510$	ns
WAIT to CSn deassert delay time	t_{CSnd}	$t_{HCLK} \times 3$	-	$t_{HCLK} \times 5$	ns

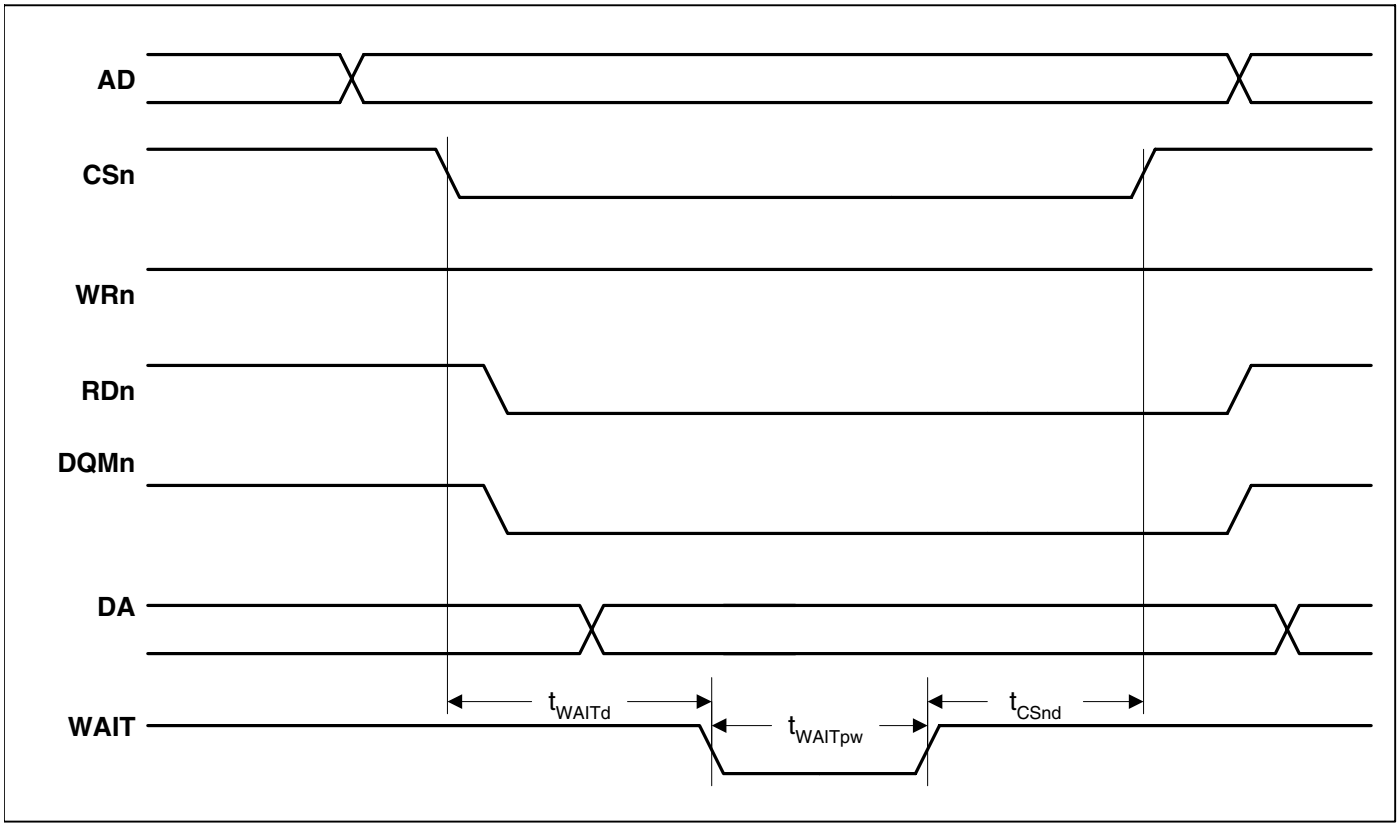


Figure 14. Static Memory Single Read Wait Cycle Timing Measurement

PCMCIA Interface

PCMCIA Read Cycle

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to signal transition time	t_{ADs}	0	-	-	ns
Attribute access time	t_A	$[(AA + 1) \times t_{HCLK}] - 14$	$(AA + 1) \times t_{HCLK}$	-	ns
Attribute hold time	t_H	$[(HA + 1) \times t_{HCLK}] - 3$	$(HA + 1) \times t_{HCLK}$	-	ns
Attribute space pre-charge delay time	t_p	$(PA + 1) \times t_{HCLK}$	$(PA + 1) \times t_{HCLK}$	-	ns
Common access time	t_A	$[(AC + 1) \times t_{HCLK}] - 14$	$(AC + 1) \times t_{HCLK}$	-	ns
Common hold time	t_H	$[(HC + 1) \times t_{HCLK}] - 3$	$(HC + 1) \times t_{HCLK}$	-	ns
Common space pre-charge delay time	t_p	$(PC + 1) \times t_{HCLK}$	$(PC + 1) \times t_{HCLK}$	-	ns
I/O access time	t_A	$[(AI + 1) \times t_{HCLK}] - 14$	$(AI + 1) \times t_{HCLK}$	-	ns
I/O hold time	t_H	$[(HI + 1) \times t_{HCLK}] - 3$	$(HI + 1) \times t_{HCLK}$	-	ns
I/O space pre-charge delay time	t_p	$(PI + 1) \times t_{HCLK}$	$(PI + 1) \times t_{HCLK}$	-	ns
MCDIR hold time	t_{MCDh}	0	-	-	ns
DA setup to MCRDn / IORDn rising edge	t_s	10	-	-	ns
DA hold from MCRDn / IORDn rising edge	t_h	0	-	-	ns

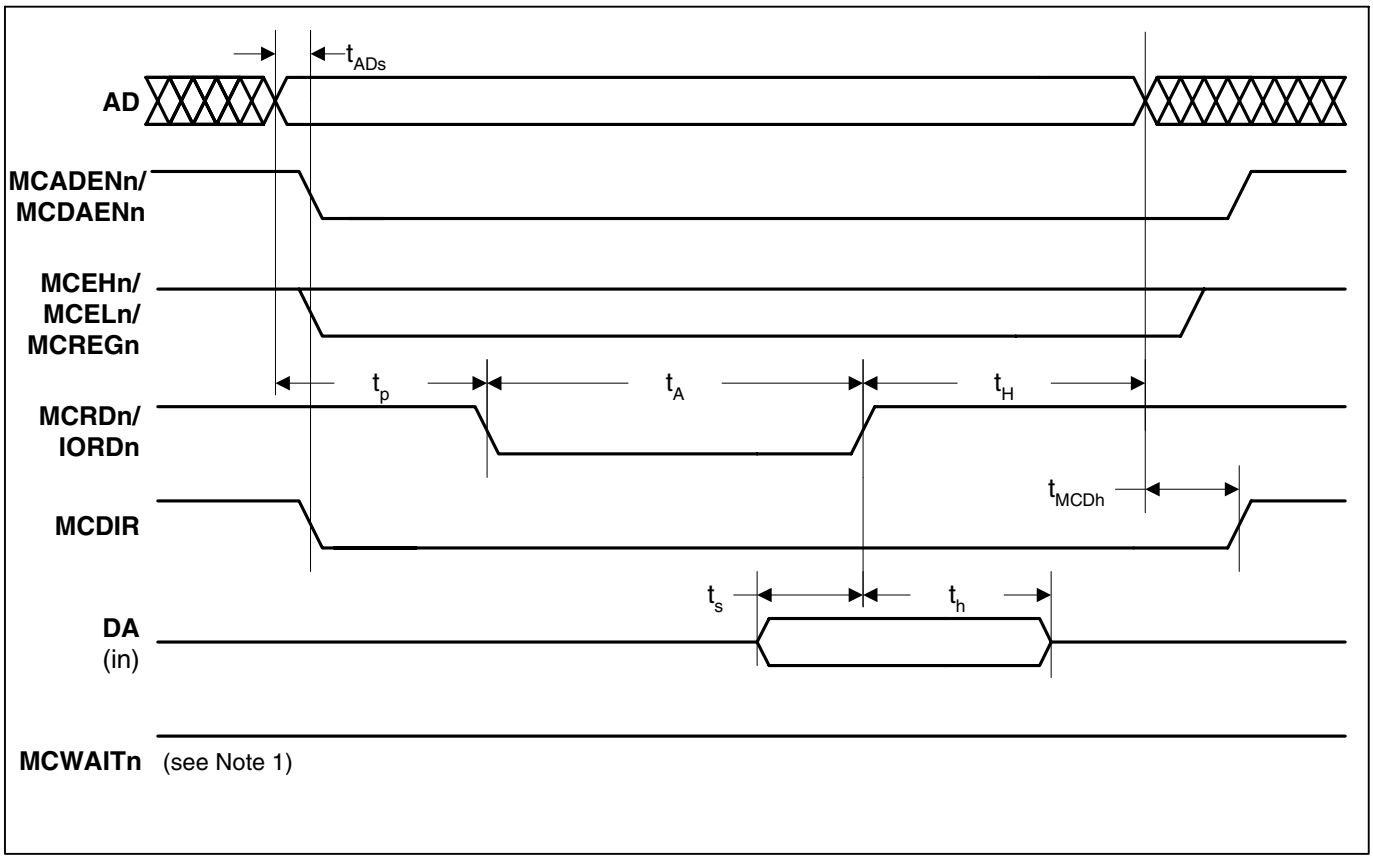


Figure 17. PCMCIA Read Cycle Timing Measurement

Note: 1 - MCWAITn asserted will extend the MCRD / IORD strobe time.

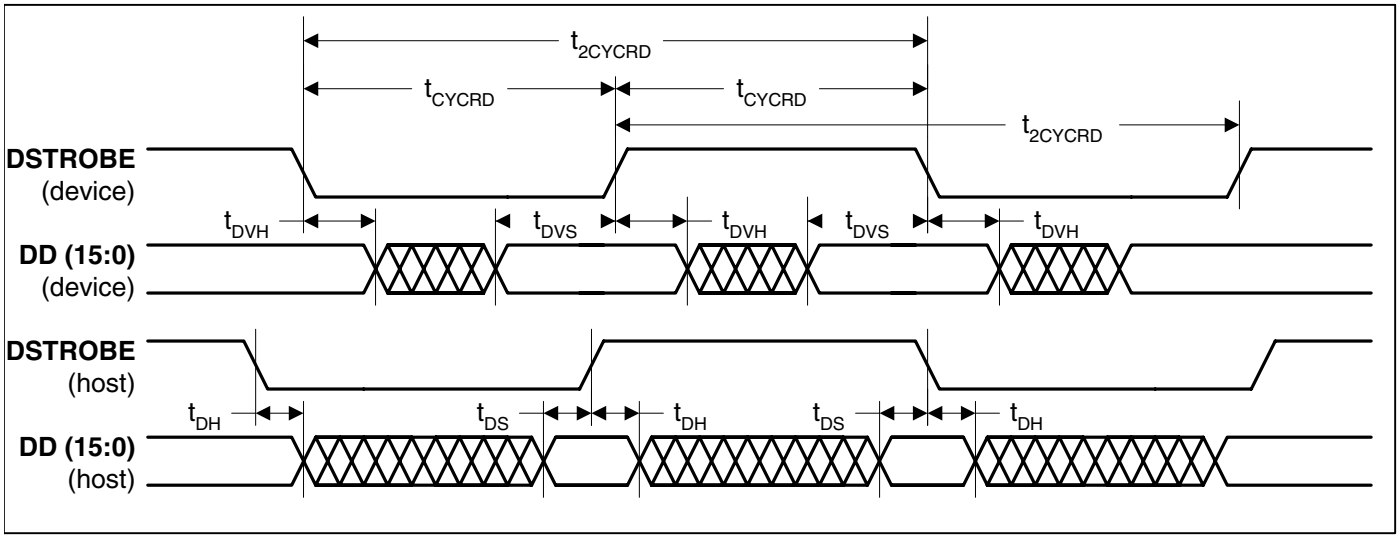
Ultra DMA Data Transfer

Figure 21 through Figure 30 define the timings associated with all phases of Ultra DMA bursts. The following table contains the values for the timings for each of the Ultra DMA modes.

Timing reference levels = 1.5 V

Parameter	Symbol	Mode 0 (in ns)		Mode 1 (in ns)		Mode 2 (in ns)		Mode 3 (in ns)	
		min	max	min	max	min	max	min	max
Cycle time allowing for asymmetry and clock variations (from DSTROBE edge to DSTROBE edge)	t_{CYCRD}	112	-	73	-	54	-	39	-
Two-cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of DSTROBE)	t_{2CYCRD}	230	-	154	-	115	-	86	-
Cycle time allowing for asymmetry and clock variations (from HSTROBE edge to HSTROBE edge)	t_{CYCWR}	230	-	170	-	130	-	100	-
Two-cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of HSTROBE)	t_{2CYCWR}	460	-	340	-	260	-	200	-
Data setup time at recipient (Read)	t_{DS}	15	-	10	-	7	-	7	-
Data hold time at recipient (Read)	t_{DH}	8	-	8	-	8	-	8	-
Data valid setup time at sender (Write) (Note 2) (from data valid until STROBE edge)	t_{DVS}	70	-	48	-	30	-	20	-
Data valid hold time at sender (Write) (Note 2) (from STROBE edge until data may become invalid)	t_{DVH}	6	-	6	-	6	-	6	-
First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	t_{FS}	0	230	0	200	0	170	0	130
Limited interlock time (Note 3)	t_{LI}	0	150	0	150	0	150	0	100
Interlock time with minimum (Note 3)	t_{MLI}	20	-	20	-	20	-	20	-
Unlimited interlock time (Note 3)	t_{UI}	0	-	0	-	0	-	0	-
Maximum time allowed for output drivers to release (from asserted or negated)	t_{AZ}	-	10	-	10	-	10	-	10
Minimum delay time required for output	t_{ZAH}	20	-	20	-	20	-	20	-
Drivers to assert or negate (from released)	t_{ZAD}	0	-	0	-	0	-	0	-
Envelope time (from DMACKn to STOP and HDMARDYn during data in burst initiation and from DMACKn to STOP during data out burst initiation)	t_{ENV}	20	70	20	70	20	70	20	55
Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDYn)	t_{RFS}	-	75	-	70	-	60	-	60
Ready-to-pause time (that recipient shall wait to pause after negating DMARDYn)	t_{RP}	160	-	125	-	100	-	100	-
Maximum time before releasing IORDY	t_{IORDYZ}	-	20	-	20	-	20	-	20
Minimum time before driving STROBE (Note 4)	t_{ZIORDY}	0	-	0	-	0	-	0	-
Setup and hold times for DMACKn (before assertion or negation)	t_{ACK}	20	-	20	-	20	-	20	-
Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	t_{SS}	50	-	50	-	50	-	50	-

Note: 1. Timing parameters shall be measured at the connector of the sender or receiver to which the parameter applies.
2. The test load for t_{DVS} and t_{DVH} shall be a lumped capacitor load with no cable or receivers. Timing for t_{DVS} and t_{DVH} shall be met for all capacitive loads from 15 to 40 pf where all signals have the same capacitive load value.
3. t_{UI}, t_{MLI} and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks, i.e., either sender or recipient is waiting for the other to respond with a signal before proceeding. t_{UI} is an unlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.
4. t_{ZIORDY} may be greater than t_{ENV} since the device has a pull up on IORDYn giving it a known state when released.
5. All IDE timing is based upon HCLK = 100 MHz.



Note: DD (15:0) and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

Figure 22. Sustained Ultra DMA data-in Burst

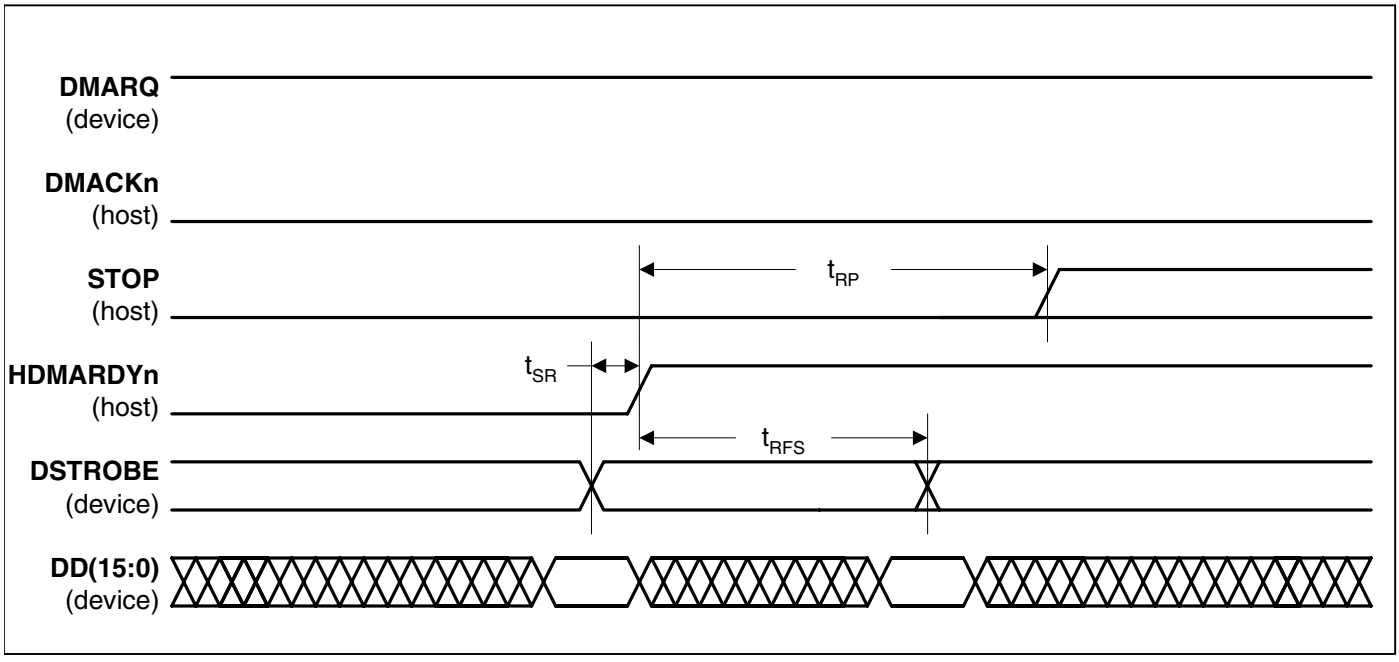
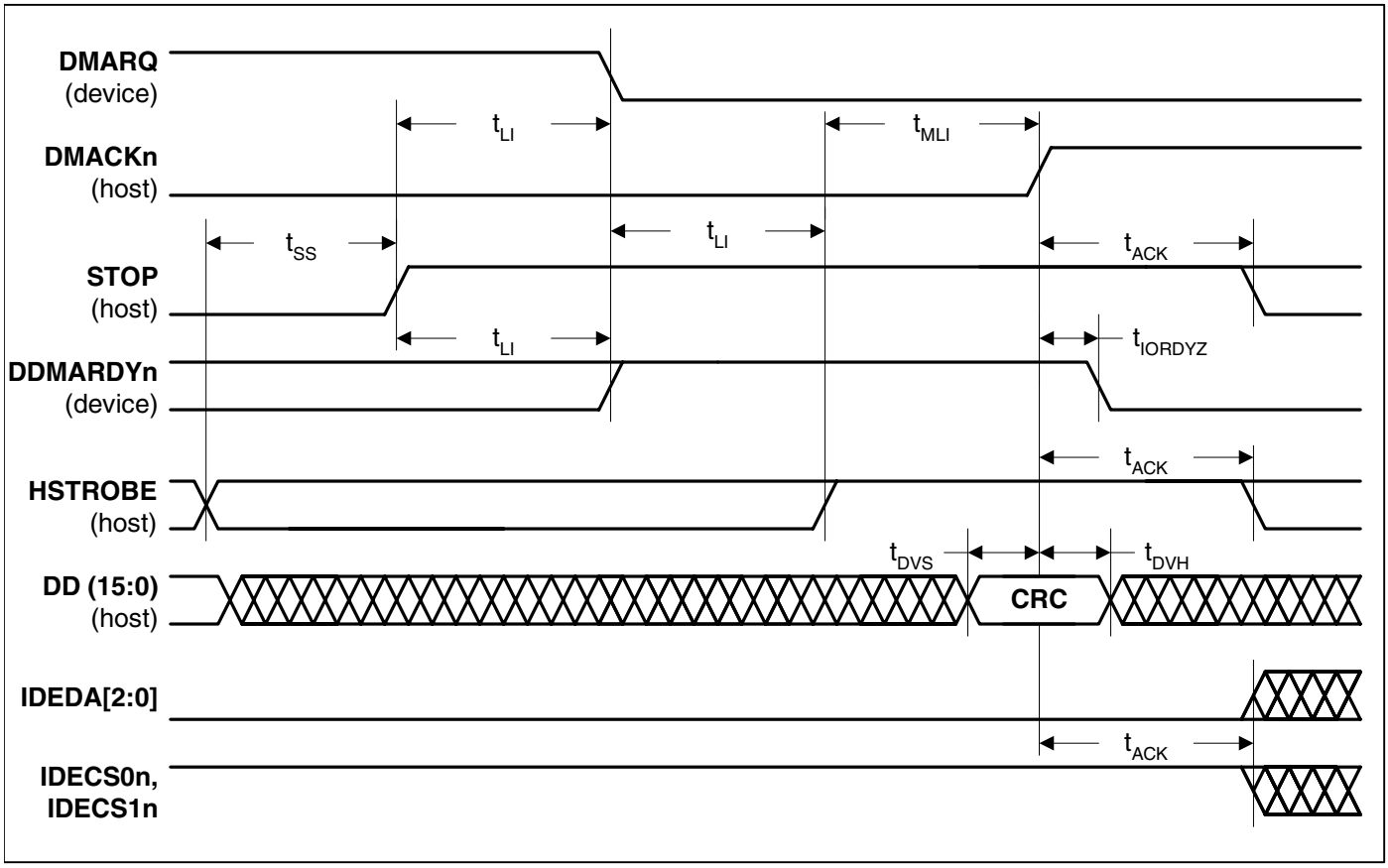


Figure 23. Host Pausing an Ultra DMA data-in Burst



Note: The definitions for the DIOWn:STOP, IORDY:DDMARDYn:DSTROBE and DIORn:HDMARDYn:HSTROBE signal lines are no longer in effect after DMARQ and DMACKn are negated.

Figure 29. Host Terminating an Ultra DMA data-out Burst

LCD Interface

Parameter	Symbol	Min	Typ	Max	Unit
SPCLK rise/fall time	t_{clkr}	2	-	8	ns
SPCLK rising edge to control signal transition time	t_{CD}	-	-	3	ns
SPCLK rising edge to data transition time	t_{DD}	-	-	10	ns
Data valid time	t_{Dv}	t_{SPCLK}	-	-	ns

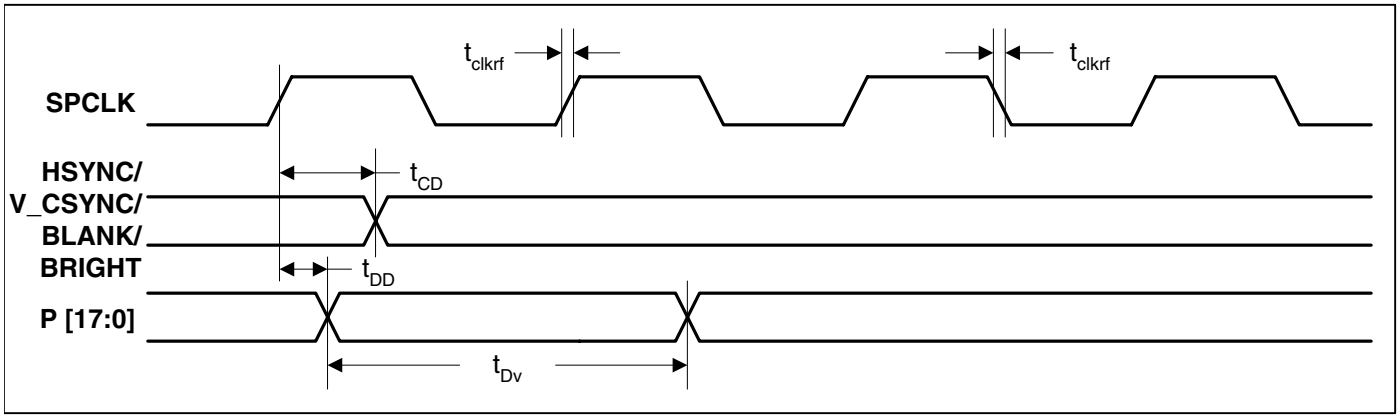
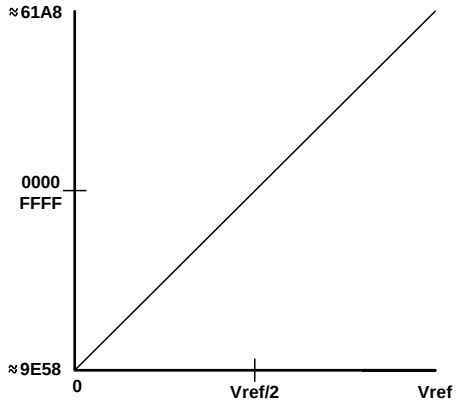


Figure 37. LCD Timing Measurement

ADC

Parameter	Comment	Value	Units
Resolution	No missing codes Range of 0 to 3.3 V	50K counts (approximate)	
Integral non-linearity		0.01%	
Offset error		±15	mV
Full scale error		0.2%	
Maximum sample rate	ADIV = 0 ADIV = 1	3750 925	Samples per second Samples per second
Channel switch settling time	ADIV = 0 ADIV = 1	500 2	µs ms
Noise (RMS) - typical		120	µV

Note: ADIV refers to bit 16 in the KeyTchClkDiv register.
ADIV = 0 means the input clock to the ADC module is equal to the external 14.7456 MHz clock divided by 4.
ADIV = 1 means the input clock to the ADC module is equal to the external 14.7456 MHz clock divided by 16.



A/D Converter Transfer Function
(approximately ±25,000 counts)

Figure 38. ADC Transfer Function

Using the ADC:

This ADC has a state-machine based conversion engine that automates the conversion process. The initiator for a conversion is the read access of the TSXYResult register by the CPU. The data returned from reading this register contains the result as well as the status bit indicating the state of the ADC. However, this peripheral requires a delay between each successful conversion and the issue of the next conversion command, or else the returned value of successive samples may not reflect the analog input. Since the state of the ADC state machine is returned through the same channel used to initiate the conversion process, there must be a delay inserted after every complete conversion. Note that reading TSXYResult during a conversion will not affect the result of the ongoing process.

The following is a recommended procedure for safely polling the ADC from software:

1. Read the TSXYResult register into a local variable to initiate a conversion.
2. If the value of bit 31 of the local variable is '0' then repeat step 1.
3. Delay long enough to meet the maximum sample rate as shown above.
4. Mask the local variable with 0xFFFF to remove extraneous data.
5. If signed mode is used, do a sign extend of the lower halfword.
6. Return the sampled value.

JTAG

Parameter	Symbol	Min	Max	Units
TCK clock period	t_{clk_per}	100	-	ns
TCK clock high time	t_{clk_high}	50	-	ns
TCK clock low time	t_{clk_low}	50	-	ns
TMS / TDI to clock rising setup time	t_{JPs}	20	-	ns
Clock rising to TMS / TDI hold time	t_{JPh}	45	-	ns
JTAG port clock to output	t_{JPco}	-	30	ns
JTAG port high impedance to valid output	t_{JPzx}	-	30	ns
JTAG port valid output to high impedance	t_{JPxz}	-	30	ns

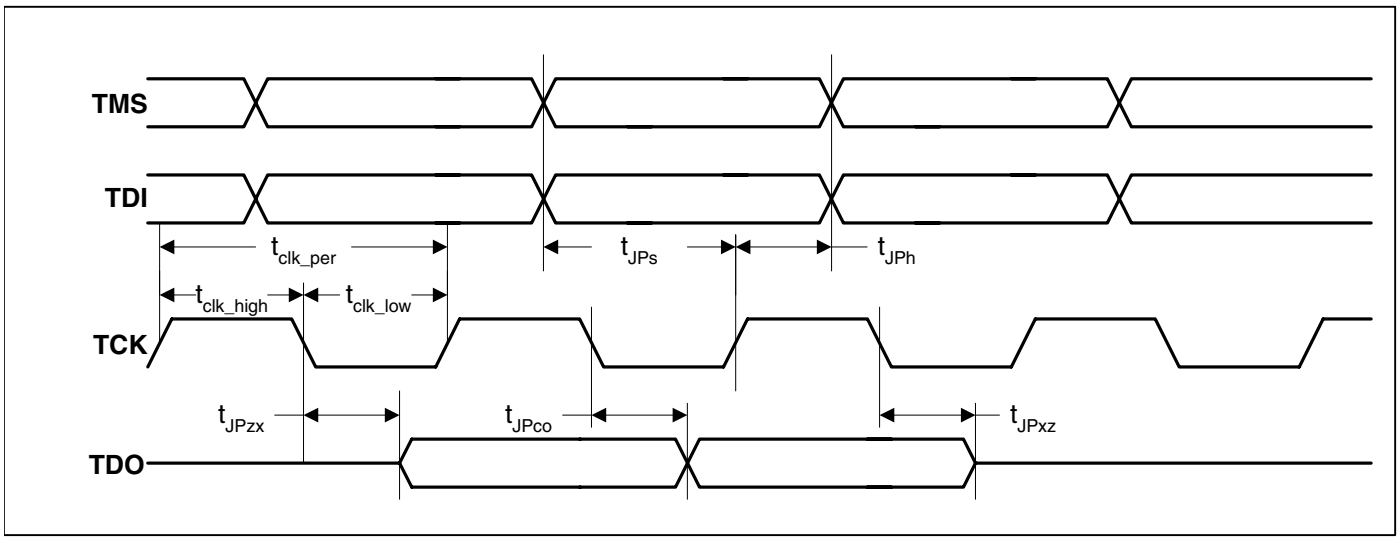


Figure 39. JTAG Timing Measurement

352 Pin BGA Package Outline

352-Ball PBGA Diagram

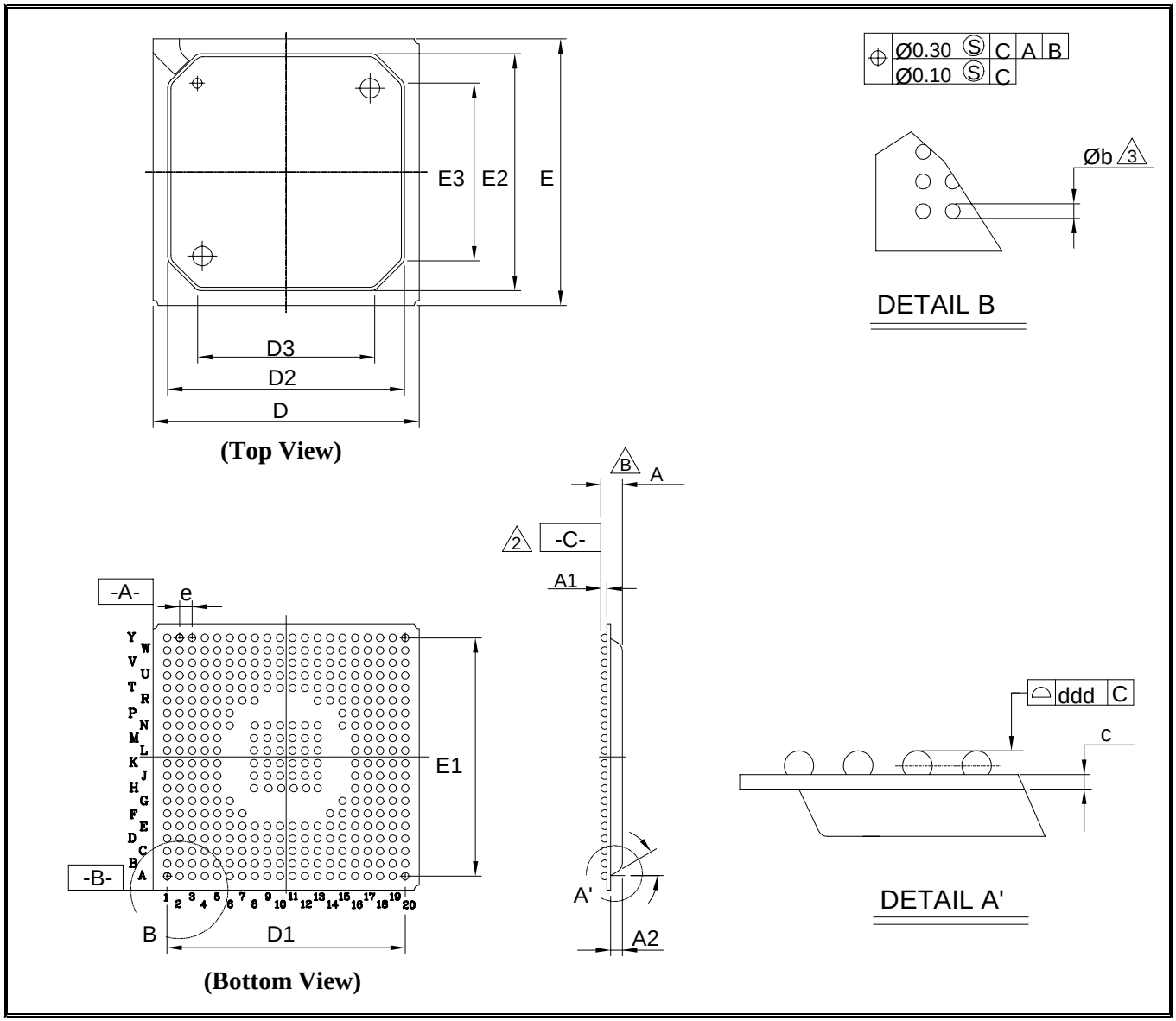


Figure 40. 352 Pin PBGA Pin Diagram

Pin List

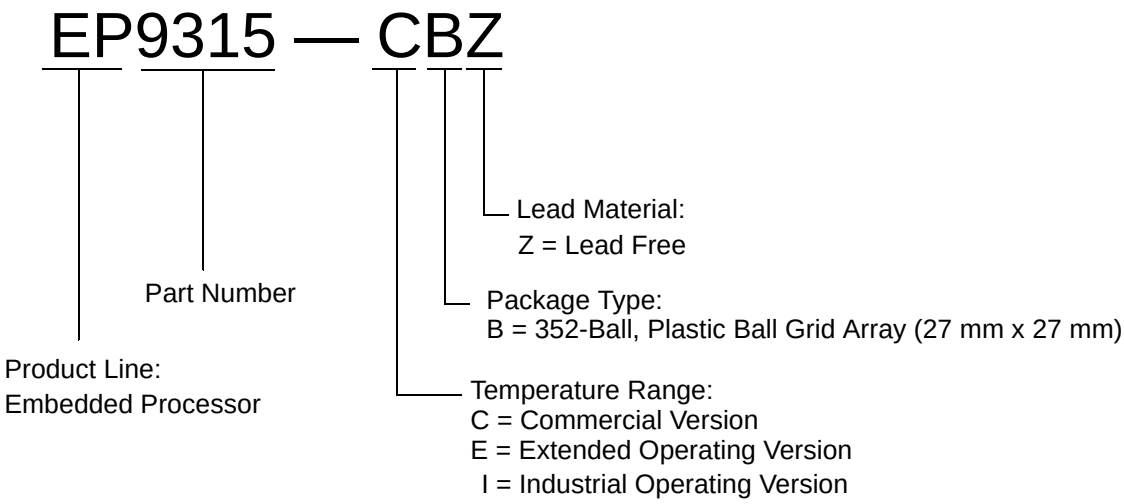
The following Plastic Ball Grid Array (PBGA) ball assignment table is sorted in order of ball.

Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal
A1	CSN[7]	E9	RVDD	L3	DA[16]	T13	CVDD
A2	DA[28]	E10	GND	L4	DA[15]	T14	GND
A3	AD[18]	E11	GND	L5	GND	T15	INT[0]
A4	DD[8]	E12	RVDD	L8	GND	T16	USBM[1]
A5	DD[4]	E13	CVDD	L9	GND	T17	RXD[0]
A6	AD[17]	E14	CVDD	L10	GND	T18	TXD[2]
A7	RDN	E15	GND	L11	GND	T19	ROW[2]
A8	RXCLK	E16	ASDI	L12	GND	T20	ROW[4]
A9	MIIRXD[0]	E17	DIOWN	L13	GND	U1	AD[0]
A10	RXDVAL	E18	EGPIO[0]	L16	CVDD	U2	P[15]
A11	MIITXD[2]	E19	EGPIO[3]	L17	COL[5]	U3	P[10]
A12	TXERR	E20	EGPIO[5]	L18	COL[7]	U4	P[7]
A13	CLD	F1	SDCSN[3]	L19	RSTON	U5	P[6]
A14	VS2	F2	DA[22]	L20	PRSTN	U6	P[4]
A15	MCBVD1	F3	DA[24]	M1	AD[7]	U7	P[0]
A16	MCREGN	F4	AD[25]	M2	DA[14]	U8	AD[13]
A17	EGPIO[12]	F5	RVDD	M3	AD[6]	U9	DA[3]
A18	EGPIO[15]	F6	GND	M4	AD[5]	U10	DA[0]
A19	IOWRN	F7	CVDD	M5	CVDD	U11	DSRN
A20	MCRESETN	F14	CVDD	M8	GND	U12	BOOT[1]
B1	CSN[2]	F15	GND	M9	GND	U13	NC
B2	DA[31]	F16	GND	M10	GND	U14	SSPRX1
B3	DA[30]	F17	EGPIO[2]	M11	GND	U15	INT[1]
B4	DA[27]	F18	EGPIO[4]	M12	GND	U16	PWMOUT
B5	DD[7]	F19	EGPIO[6]	M13	GND	U17	USBM[0]
B6	DD[3]	F20	EGPIO[8]	M16	GND	U18	RXD[1]
B7	WRN	G1	SDCSN[0]	M17	COL[4]	U19	TXD[1]
B8	MDIO	G2	SDCSN[1]	M18	COL[3]	U20	ROW[1]
B9	MIIRXD[1]	G3	SDWEN	M19	COL[6]	V1	P[16]
B10	RXERR	G4	SDCLK	M20	CSN[0]	V2	P[11]
B11	MIITXD[1]	G5	RVDD	N1	DA[13]	V3	P[8]
B12	CRS	G6	RVDD	N2	DA[12]	V4	DD[15]
B13	VS1	G15	RVDD	N3	DA[11]	V5	DD[13]
B14	MCD1	G16	RVDD	N4	AD[3]	V6	P[1]
B15	MCBVD2	G17	EGPIO[7]	N5	CVDD	V7	AD[14]
B16	MCEHN	G18	EGPIO[9]	N6	CVDD	V8	AD[12]
B17	EGPIO[13]	G19	EGPIO[10]	N8	GND	V9	DA[2]
B18	MCRDN	G20	EGPIO[11]	N9	GND	V10	IDECS0N
B19	WAITN	H1	DQMN[3]	N10	GND	V11	IDEDA[2]
B20	TRSTN	H2	CASN	N11	GND	V12	TDI
C1	CSN[1]	H3	RASN	N12	GND	V13	GND
C2	CSN[3]	H4	SDCSN[2]	N13	GND	V14	ASYNC

Ordering Information

The order numbers for the device are:

EP9315-CB	0°C to +70°C	352-pin PBGA	
EP9315-CBZ	0°C to +70°C	352-pin PBGA	Lead Free
EP9315-IB	-40°C to +85°C	352-pin PBGA	
EP9315-IBZ	-40°C to +85°C	352-pin PBGA	Lead Free



Note: Go to the Cirrus Logic Internet site at http://www.cirrus.com to find contact information for your local sales representative.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **www.cirrus.com**