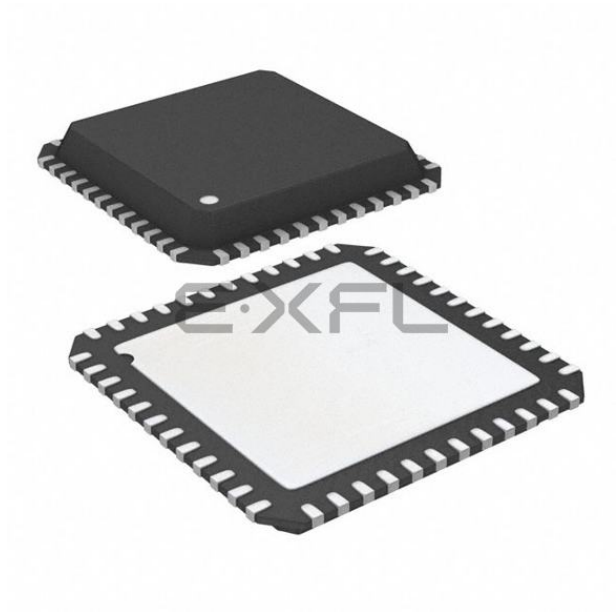

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TFQFN Exposed Pad
Supplier Device Package	48-QFN-EP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12p96j0cft

3.2 External Signal Description . . . 109
3.3 Memory Map and Registers . . . 109
3.3.1 Module Memory Map . . . 109
3.3.2 Register Descriptions . . . 110
3.4 Functional Description . . . 113
3.4.1 MCU Operating Modes . . . 113
3.4.2 Memory Map Scheme . . . 114
3.5 Implemented Memory in the System Memory Architecture . . . 117
3.5.1 Chip Bus Control . . . 119
3.5.2 Interrupts . . . 119
3.6 Initialization/Application Information . . . 120
3.6.1 CALL and RTC Instructions . . . 120

Chapter 4
Interrupt Module (S12SINTV1)

4.1 Introduction . . . 123
4.1.1 Glossary . . . 123
4.1.2 Features . . . 123
4.1.3 Modes of Operation . . . 124
4.1.4 Block Diagram . . . 124
4.2 External Signal Description . . . 125
4.3 Memory Map and Register Definition . . . 125
4.3.1 Register Descriptions . . . 125
4.4 Functional Description . . . 126
4.4.1 S12S Exception Requests . . . 126
4.4.2 Interrupt Prioritization . . . 126
4.4.3 Reset Exception Requests . . . 127
4.4.4 Exception Priority . . . 127
4.5 Initialization/Application Information . . . 128
4.5.1 Initialization . . . 128
4.5.2 Interrupt Nesting . . . 128
4.5.3 Wake Up from Stop or Wait Mode . . . 128

Chapter 5
Background Debug Module (S12SBDMV1)

5.1 Introduction . . . 131
5.1.1 Features . . . 132
5.1.2 Modes of Operation . . . 132
5.1.3 Block Diagram . . . 133
5.2 External Signal Description . . . 133
5.3 Memory Map and Register Definition . . . 134
5.3.1 Module Memory Map . . . 134
5.3.2 Register Descriptions . . . 134
5.3.3 Family ID Assignment . . . 138

Table 2-2. Block Memory Map (continued)

Port	Offset or Address	Register	Access	Reset Value	Section/Page
S	0x0248	PTS—Port S Data Register	R/W	0x00	2.3.24/2-77
	0x0249	PTIS—Port S Input Register	R	[4]	2.3.25/2-77
	0x024A	DDRS—Port S Data Direction Register	R/W	0x00	2.3.26/2-78
	0x024B	RDRS—Port S Reduced Drive Register	R/W	0x00	2.3.27/2-79
	0x024C	PERS—Port S Pull Device Enable Register	R/W	0xFF	2.3.28/2-79
	0x024D	PTPS—Port S Polarity Select Register	R/W	0x00	2.3.29/2-80
	0x024E	WOMS—Port S Wired-Or Mode Register	R/W	0x00	2.3.30/2-80
	0x024F	PIM Reserved	R	0x00	2.3.39/2-86
M	0x0250	PTM—Port M Data Register	R/W	0x00	2.3.32/2-81
	0x0251	PTIM—Port M Input Register	R	[4]	2.3.33/2-82
	0x0252	DDRM—Port M Data Direction Register	R/W	0x00	2.3.34/2-83
	0x0253	RDRM—Port M Reduced Drive Register	R/W	0x00	2.3.35/2-84
	0x0254	PERM—Port M Pull Device Enable Register	R/W	0x00	2.3.36/2-85
	0x0255	PPSM—Port M Polarity Select Register	R/W	0x00	2.3.37/2-85
	0x0256	WOMM—Port M Wired-Or Mode Register	R/W	0x00	2.3.38/2-86
	0x0257	PIM Reserved	R	0x00	2.3.39/2-86
P	0x0258	PTP—Port P Data Register	R/W	0x00	2.3.40/2-87
	0x0259	PTIP—Port P Input Register	R	[4]	2.3.41/2-88
	0x025A	DDRP—Port P Data Direction Register	R/W	0x00	2.3.42/2-88
	0x025B	RDRP—Port P Reduced Drive Register	R/W	0x00	2.3.43/2-89
	0x025C	PERP—Port P Pull Device Enable Register	R/W	0x00	2.3.44/2-90
	0x025D	PTPP—Port P Polarity Select Register	R/W	0x00	2.3.45/2-90
	0x025E	PIEP—Port P Interrupt Enable Register	R/W	0x00	2.3.46/2-91
	0x025F	PIFP—Port P Interrupt Flag Register	R/W	0x00	2.3.47/2-91
	0x0260 : 0x0267	PIM Reserved	R	0x00	2.3.48/2-92

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x027C Reserved	R	0	0	0	0	0	0	0	0
	W								
0x027D Reserved	R	0	0	0	0	0	0	0	0
	W								
0x027E Reserved	R	0	0	0	0	0	0	0	0
	W								
0x027F Reserved	R	0	0	0	0	0	0	0	0
	W								

= Unimplemented or Reserved

2.3.2 Register Descriptions

The following table summarizes the effect of the various configuration bits, i.e. data direction (DDR), output level (IO), reduced drive (RDR), pull enable (PE), pull select (PS) on the pin function and pull device activity.

The configuration bit PS is used for two purposes:

1. Configure the sensitive interrupt edge (rising or falling), if interrupt is enabled.
2. Select either a pull-up or pull-down device if PE is active.

2.3.12 ECLK Control Register (ECLKCTL)

Address 0x001C Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	NECLK	NCLKX2	DIV16	EDIV4	EDIV3	EDIV2	EDIV1	EDIV0
Reset:	Mode Depen-dent	1	0	0	0	0	0	0
Special single-chip	0	1	0	0	0	0	0	0
Normal single-chip	1	1	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-10. ECLK Control Register (ECLKCTL)

1. Read: Anytime
   Write: Anytime

Table 2-12. ECLKCTL Register Field Descriptions

Field	Description
7 NECLK	**No ECLK**—Disable ECLK output This bit controls the availability of a free-running clock on the ECLK pin. This clock has a fixed rate of equivalent to the internal bus clock. 1 ECLK disabled 0 ECLK enabled
6 NCLKX2	**No ECLKX2**—Disable ECLKX2 output This bit controls the availability of a free-running clock on the ECLKX2 pin. This clock has a fixed rate of twice the internal bus clock. 1 ECLKX2 disabled 0 ECLKX2 enabled
5 DIV16	**Free-running ECLK pre-divider**—Divide by 16 This bit enables a divide-by-16 stage on the selected EDIV rate. 1 Divider enabled: ECLK rate = EDIV rate divided by 16 0 Divider disabled: ECLK rate = EDIV rate
4-0 EDIV	**Free-running ECLK Divider**—Configure ECLK rate These bits determine the rate of the free-running clock on the ECLK pin. 00000 ECLK rate = bus clock rate 00001 ECLK rate = bus clock rate divided by 2 00010 ECLK rate = bus clock rate divided by 3,... 11111 ECLK rate = bus clock rate divided by 32

2.3.13 PIM Reserved Register

Port E pin PE[0] can be used for either general purpose input or as the level-sensitive $\overline{\text{XIRQ}}$ interrupt. $\overline{\text{XIRQ}}$ can be enabled by clearing the X-bit in the CPU condition code register. It is inhibited at reset so this pin is initially configured as a high-impedance input with a pull-up.

2.4.3.4 Port T

This port is associated with TIM and PWM.

Port T pins PT[5:4,0] can be used for either general purpose I/O, or with the routed PWM or with the channels of the standard Timer subsystem.

Port T pins PT[7:6,3:1] can be used for either general purpose I/O, or with the channels of the standard Timer subsystem.

2.4.3.5 Port S

This port is associated with SCI.

Port S pins PS[1:0] can be used either for general purpose I/O, or with the SCI subsystem.

Port S pins PS[3:2] can be used for general purpose I/O.

2.4.3.6 Port M

This port is associated with CAN and SPI.

Port M pins PM[1:0] can be used for either general purpose I/O, or with the CAN subsystem.

Port M pins PM[5:2] can be used for general purpose I/O, or with the SPI subsystem.

2.4.3.7 Port P

This port is associated with the PWM.

Port P pins PP[7,5:0] can be used for either general purpose I/O with pin interrupt capability, or with the PWM subsystem.

2.4.3.8 Port J

Port J pins PJ[7:6,2:0] can be used for general purpose I/O with pin-interrupt capability.

2.4.3.9 Port AD

This port is associated with the ATD.

Port AD pins PAD[9:0] can be used for either general purpose I/O, or with the ATD subsystem.

a forced match, a state sequencer transition can occur immediately on a successful match of system busses and comparator registers. Whilst tagging, at a comparator match, the instruction opcode is tagged and only if the instruction reaches the execution stage of the instruction queue can a state sequencer transition occur. In the case of a transition to Final State, bus tracing is triggered and/or a breakpoint can be generated.

A state sequencer transition to final state (with associated breakpoint, if enabled) can be initiated by writing to the TRIG bit in the DBGC1 control register.

The trace buffer is visible through a 2-byte window in the register address map and must be read out using standard 16-bit word reads.

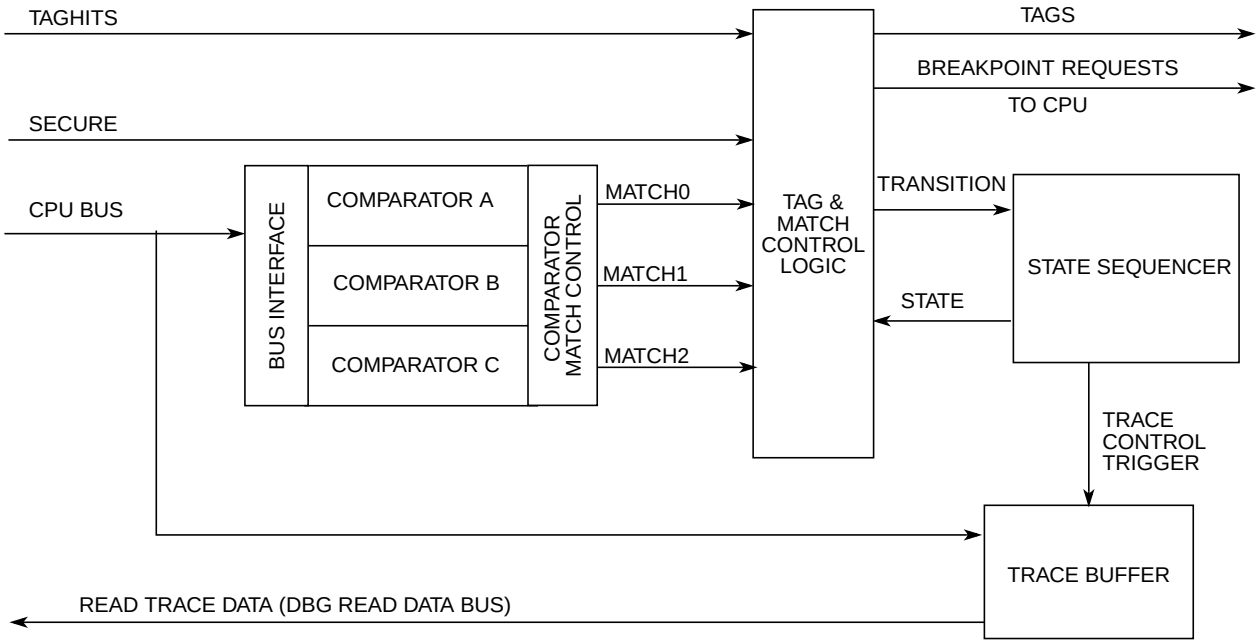


Figure 6-23. DBG Overview

6.4.2 Comparator Modes

The DBG contains three comparators, A, B and C. Each comparator compares the system address bus with the address stored in DBGXAH, DBGXAM, and DBGXAL. Furthermore, comparator A also compares the data buses to the data stored in DBGADH, DBGADL and allows masking of individual data bus bits.

All comparators are disabled in BDM and during BDM accesses.

The comparator match control logic (see Figure 6-23) configures comparators to monitor the buses for an exact address or an address range, whereby either an access inside or outside the specified range generates a match condition. The comparator configuration is controlled by the control register contents and the range control by the DBGC2 contents.

A match can initiate a transition to another state sequencer state (see 6.4.4”). The comparator control register also allows the type of access to be included in the comparison through the use of the RWE, RW, SZE, and SZ bits. The RWE bit controls whether read or write comparison is enabled for the associated comparator and the RW bit selects either a read or write access for a valid match. Similarly the SZE and

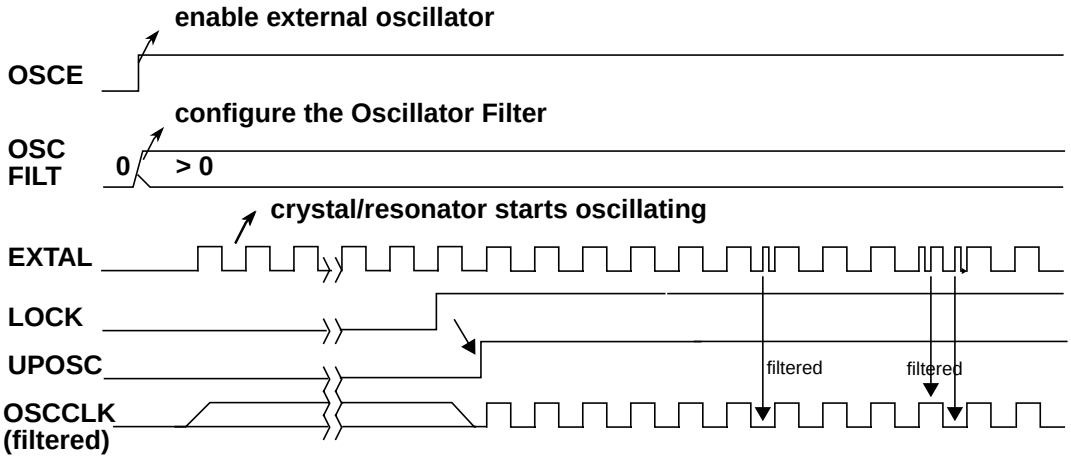
7.4.5.2 The Adaptive Oscillator Filter

A spike in the oscillator clock can disturb the function of the modules driven by this clock.

The adaptive Oscillator Filter includes two features:

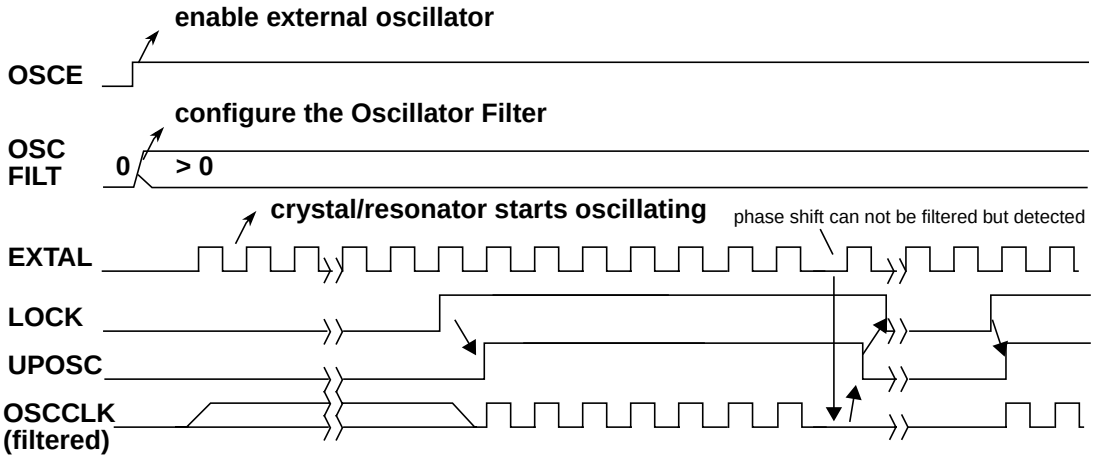
1. Filter noise (spikes) from the incoming external oscillator clock. The filter function is illustrated in Figure 7-35.

Figure 7-35. Noise filtered by the Adaptive Oscillator Filter



2. Detect severe noise disturbances on the external oscillator clock, which can not be filtered and indicate the critical situation to the software by clearing the UPOSC and LOCK status bit and setting the OSCIF and LOCKIF flag. An example for the detection of critical noise is illustrated in Figure 7-36.

Figure 7-36. Critical noise detected by the Adaptive Oscillator Filter

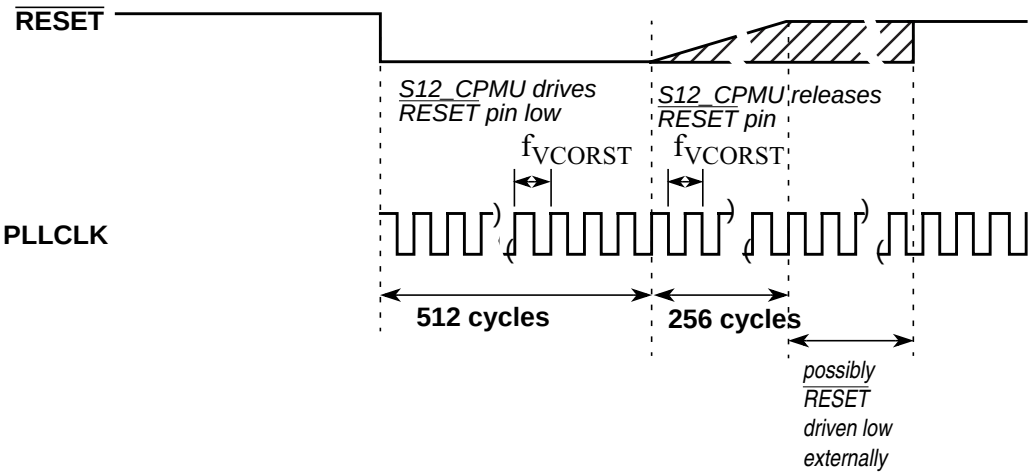


NOTE

If the LOCK bit is clear due to severe noise disturbance on the external oscillator clock the PLLCLK is derived from the VCO clock (with its actual frequency) divided by four (see also Section 7.3.2.3, “S12CPMU Post Divider Register (CPMUPOSTDIV))

The internal reset of the MCU remains asserted while the reset generator completes the 768 PLLCLK cycles long reset sequence. In case the RESET pin is externally driven low for more than these 768 PLLCLK cycles (External Reset), the internal reset remains asserted longer.

Figure 7-37. RESET Timing



7.5.2.1 Clock Monitor Reset

If the external oscillator is enabled (OSCE=1) in case of loss of oscillation or the oscillator frequency is below the failure assert frequency f_{CMFA} (see device electrical characteristics for values), the S12CPMU generates a Clock Monitor Reset.In Full Stop Mode the external oscillator and the clock monitor are disabled.

7.5.2.2 Computer Operating Properly Watchdog (COP) Reset

The COP (free running watchdog timer) enables the user to check that a program is running and sequencing properly. When the COP is being used, software is responsible for keeping the COP from timing out. If the COP times out it is an indication that the software is no longer being executed in the intended sequence; thus COP reset is generated.

The clock source for the COP is either IRCCLK or OSCCLK depending on the setting of the COPOSCSEL bit. In Stop Mode with PSTP=1 (Pseudo Stop Mode), COPOSCSEL=1 and PCE=1 the COP continues to run, else the COP counter halts in Stop Mode.

Three control bits in the CPMUCOP register allow selection of seven COP time-out periods.

When COP is enabled, the program must write $55 and $AA (in this order) to the CPMUARMCOP register during the selected time-out period. Once this is done, the COP time-out period is restarted. If the program fails to do this and the COP times out, a COP reset is generated. Also, if any value other than $55 or $AA is written, a COP reset generated.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x000E CANRXERR	R	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
	W								
0x000F CANTXERR	R	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
	W								
0x0010–0x0013 CANIDAR0–3	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
	W								
0x0014–0x0017 CANIDMRx	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
	W								
0x0018–0x001B CANIDAR4–7	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
	W								
0x001C–0x001F CANIDMR4–7	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
	W								
0x0020–0x002F CANRXFG	R	See Section 8.3.3, "Programmer's Model of Message Storage"							
	W								
0x0030–0x003F CANTXFG	R	See Section 8.3.3, "Programmer's Model of Message Storage"							
	W								

= Unimplemented or Reserved

Figure 8-3. MSCAN Register Summary (continued)

8.3.2 Register Descriptions

This section describes in detail all the registers and register bits in the MSCAN module. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order. All bits of all registers in this module are completely synchronous to internal clocks during a register read.

8.3.2.1 MSCAN Control Register 0 (CANCTL0)

The CANCTL0 register provides various control bits of the MSCAN module as described below.

Table 8-6. Synchronization Jump Width (continued)

SJW1	SJW0	Synchronization Jump Width
0	1	2 Tq clock cycles
1	0	3 Tq clock cycles
1	1	4 Tq clock cycles

Table 8-7. Baud Rate Prescaler

BRP5	BRP4	BRP3	BRP2	BRP1	BRP0	Prescaler value (P)
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
:	:	:	:	:	:	:
1	1	1	1	1	1	64

8.3.2.4 MSCAN Bus Timing Register 1 (CANBTR1)

The CANBTR1 register configures various CAN bus timing parameters of the MSCAN module.

Module Base + 0x0003 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
Reset:	0	0	0	0	0	0	0	0

Figure 8-7. MSCAN Bus Timing Register 1 (CANBTR1)

1. Read: Anytime
   Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 8-8. CANBTR1 Register Field Descriptions

Field	Description
7 SAMP	**Sampling** — This bit determines the number of CAN bus samples taken per bit time. 0 One sample per bit. 1 Three samples per bit(1). If SAMP = 0, the resulting bit value is equal to the value of the single bit positioned at the sample point. If SAMP = 1, the resulting bit value is determined by using majority rule on the three total samples. For higher bit rates, it is recommended that only one sample is taken per bit time (SAMP = 0).
6-4 TSEG2[2:0]	**Time Segment 2** — Time segments within the bit time fix the number of clock cycles per bit time and the location of the sample point (see Figure 8-44). Time segment 2 (TSEG2) values are programmable as shown in Table 8-9.
3-0 TSEG1[3:0]	**Time Segment 1** — Time segments within the bit time fix the number of clock cycles per bit time and the location of the sample point (see Figure 8-44). Time segment 1 (TSEG1) values are programmable as shown in Table 8-10.

8.3.3.3 Data Length Register (DLR)

This register keeps the data length field of the CAN frame.

Module Base + 0x00XC

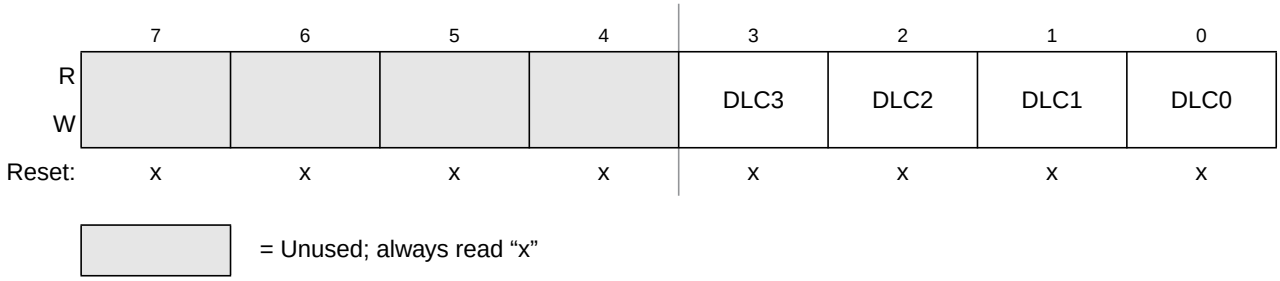


Figure 8-35. Data Length Register (DLR) — Extended Identifier Mapping

Table 8-34. DLR Register Field Descriptions

Field	Description
3-0 DLC[3:0]	**Data Length Code Bits** — The data length code contains the number of bytes (data byte count) of the respective message. During the transmission of a remote frame, the data length code is transmitted as programmed while the number of transmitted data bytes is always 0. The data byte count ranges from 0 to 8 for a data frame. Table 8-35 shows the effect of setting the DLC bits.

Table 8-35. Data Length Codes

Data Length Code				Data Byte Count
DLC3	DLC2	DLC1	DLC0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

8.3.3.4 Transmit Buffer Priority Register (TBPR)

This register defines the local priority of the associated message buffer. The local priority is used for the internal prioritization process of the MSCAN and is defined to be highest for the smallest binary number. The MSCAN implements the following internal prioritization mechanisms:

- All transmission buffers with a cleared TXEx flag participate in the prioritization immediately before the SOF (start of frame) is sent.
- The transmission buffer with the lowest local priority field wins the prioritization.

9.2 Signal Description

This section lists all inputs to the ADC12B10C block.

9.2.1 Detailed Signal Descriptions

9.2.1.1 AN*x* (*x* = 9, 8, 7, 6, 5, 4, 3, 2, 1, 0)

This pin serves as the analog input Channel *x*. It can also be configured as digital port or external trigger for the ATD conversion.

9.2.1.2 ETRIG3, ETRIG2, ETRIG1, ETRIG0

These inputs can be configured to serve as an external trigger for the ATD conversion.

Refer to device specification for availability and connection of these inputs!

9.2.1.3 V_{RH}, V_{RL}

V_{RH} is the high reference voltage, V_{RL} is the low reference voltage for ATD conversion.

9.2.1.4 V_{DDA}, V_{SSA}

These pins are the power supplies for the analog circuitry of the ADC12B10C block.

9.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the ADC12B10C.

9.3.1 Module Memory Map

Figure 9-2 gives an overview on all ADC12B10C registers.

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	ATDCTL0	R W	Reserved	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
0x0001	ATDCTL1	R W	ETRIGSEL	SRES1	SRES0	SMP_DIS	ETRIGCH3	ETRIGCH2	ETRIGCH1	ETRIGCH0
0x0002	ATDCTL2	R W	0	AFFC	ICLKSTP	ETRIGLE	ETRIGP	ETRIGE	ASCIE	ACMPIE

= Unimplemented or Reserved

Figure 9-2. ADC12B10C Register Summary (Sheet 1 of 3)

Read: always read 0x0000 in normal modes

Write: unimplemented in normal modes

NOTE

Writing to this register when in special modes can alter the PWM functionality.

10.3.2.8 Reserved Register (PWMPRSC)

This register is reserved for factory testing of the PWM module and is not available in normal modes.

Module Base + 0x0007

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-10. Reserved Register (PWMPRSC)

Read: always read 0x0000 in normal modes

Write: unimplemented in normal modes

NOTE

Writing to this register when in special modes can alter the PWM functionality.

10.3.2.9 PWM Scale A Register (PWMSCLA)

PWMSCLA is the programmable scale value used in scaling clock A to generate clock SA. Clock SA is generated by taking clock A, dividing it by the value in the PWMSCLA register and dividing that by two.

Clock SA = Clock A / (2 * PWMSCLA)

NOTE

When PWMSCLA = 0x0000, PWMSCLA value is considered a full scale value of 256. Clock A is thus divided by 512.

Any value written to this register will cause the scale counter to load the new scale value (PWMSCLA).

Module Base + 0x0008

	7	6	5	4	3	2	1	0
R	Bit 7	6	5	4	3	2	1	Bit 0
W								
Reset	0	0	0	0	0	0	0	0

Figure 10-11. PWM Scale A Register (PWMSCLA)

due to the synchronization of PWMEx and the clock source. An exception to this is when channels are concatenated. Refer to Section 10.4.2.7, “PWM 16-Bit Functions,” for more detail.

NOTE

The first PWM cycle after enabling the channel can be irregular.

On the front end of the PWM timer, the clock is enabled to the PWM circuit by the PWMEx bit being high. There is an edge-synchronizing circuit to guarantee that the clock will only be enabled or disabled at an edge. When the channel is disabled (PWMEx = 0), the counter for the channel does not count.

10.4.2.2 PWM Polarity

Each channel has a polarity bit to allow starting a waveform cycle with a high or low signal. This is shown on the block diagram as a mux select of either the Q output or the $\overline{Q}$ output of the PWM output flip-flop. When one of the bits in the PWMPOL register is set, the associated PWM channel output is high at the beginning of the waveform, then goes low when the duty count is reached. Conversely, if the polarity bit is 0, the output starts low and then goes high when the duty count is reached.

10.4.2.3 PWM Period and Duty

Dedicated period and duty registers exist for each channel and are double buffered so that if they change while the channel is enabled, the change will NOT take effect until one of the following occurs:

- The effective period ends
- The counter is written (counter resets to 0x0000)
- The channel is disabled

In this way, the output of the PWM will always be either the old waveform or the new waveform, not some variation in between. If the channel is not enabled, then writes to the period and duty registers will go directly to the latches as well as the buffer.

A change in duty or period can be forced into effect “immediately” by writing the new value to the duty and/or period registers and then writing to the counter. This forces the counter to reset and the new duty and/or period values to be latched. In addition, because the counter is readable it is possible to know where the count is with respect to the duty value and software can be used to make adjustments.

NOTE

When forcing a new period or duty into effect immediately, an irregular PWM cycle can occur.

Depending on the polarity bit, the duty registers will contain the count of either the high time or the low time.

10.4.2.4 PWM Timer Counters

Each channel has a dedicated 8-bit up/down counter which runs at the rate of the selected clock source (reference Figure 10-34 for the available clock sources and rates). The counter compares to two registers, a duty register and a period register as shown in Figure 10-35. When the PWM counter matches the duty register the output flip-flop changes state causing the PWM waveform to also change state. A match

Table 13-39. Program P-Flash Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters
011	Word 1 program value
100	Word 2 program value
101	Word 3 program value

1. Global address [2:0] must be 000

Upon clearing CCIF to launch the Program P-Flash command, the Memory Controller will program the data words to the supplied global address and will then proceed to verify the data words read back as expected. The CCIF flag will set after the Program P-Flash operation has completed.

Table 13-40. Program P-Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 101 at command launch
		Set if command not available in current mode (see Table 13-27)
		Set if an invalid global address [17:0] is supplied
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the global address [17:0] points to a protected area
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

13.4.5.6 Program Once Command

The Program Once command restricts programming to a reserved 64 byte field (8 phrases) in the nonvolatile information register located in P-Flash. The Program Once reserved field can be read using the Read Once command as described in Section 13.4.5.4. The Program Once command must only be issued once since the nonvolatile information register in P-Flash cannot be erased. The Program Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 13-41. Program Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x07	Not Required
001	Program Once phrase index (0x0000 - 0x0007)	
010	Program Once word 0 value	
011	Program Once word 1 value	
100	Program Once word 2 value	
101	Program Once word 3 value	

Table 13-55. Set User Margin Level Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 13-27)
		Set if an invalid global address [17:16] is supplied
		Set if an invalid margin level setting is supplied
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

NOTE

User margin levels can be used to check that Flash memory contents have adequate margin for normal level read operations. If unexpected results are encountered when checking Flash memory contents at user margin levels, a potential loss of information has been detected.

13.4.5.13 Set Field Margin Level Command

The Set Field Margin Level command, valid in special modes only, causes the Memory Controller to set the margin level specified for future read operations of the P-Flash or D-Flash block.

Table 13-56. Set Field Margin Level Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0E	Global address [17:16] to identify the Flash block
001	Margin level setting	

Upon clearing CCIF to launch the Set Field Margin Level command, the Memory Controller will set the field margin level for the targeted block and then set the CCIF flag.

NOTE

When the D-Flash block is targeted, the D-Flash field margin levels are applied only to the D-Flash reads. However, when the P-Flash block is targeted, the P-Flash field margin levels are applied to both P-Flash and D-Flash reads. It is not possible to apply field margin levels to the P-Flash block only.

Valid margin level settings for the Set Field Margin Level command are defined in Table 13-57.

14.4.3.1 OC Channel Initialization

Internal register whose output drives OCx can be programmed before timer drives OCx. The desired state can be programmed to this Internal register by writing a one to CFORCx bit with TIOSx, OCPDx and TEN bits set to one. Setting OCPDx to zero allows Interal register to drive the programmed state to OCx. This allows a glitch free switch over of port from general purpose I/O to timer output once the OCPDx bit is set to zero.

14.4.4 Pulse Accumulator

The pulse accumulator (PACNT) is a 16-bit counter that can operate in two modes:

Event counter mode — Counting edges of selected polarity on the pulse accumulator input pin, PAI.

Gated time accumulation mode — Counting pulses from a divide-by-64 clock. The PAMOD bit selects the mode of operation.

The minimum pulse width for the PAI input is greater than two bus clocks.

14.4.5 Event Counter Mode

Clearing the PAMOD bit configures the PACNT for event counter operation. An active edge on the IOC7 pin increments the pulse accumulator counter. The PEDGE bit selects falling edges or rising edges to increment the count.

NOTE

The PACNT input and timer channel 7 use the same pin IOC7. To use the IOC7, disconnect it from the output logic by clearing the channel 7 output mode and output level bits, OM7 and OL7. Also clear the channel 7 output compare 7 mask bit, OC7M7.

The Pulse Accumulator counter register reflect the number of active input edges on the PACNT input pin since the last reset.

The PAOVF bit is set when the accumulator rolls over from 0xFFFF to 0x0000. The pulse accumulator overflow interrupt enable bit, PAOVI, enables the PAOVF flag to generate interrupt requests.

NOTE

The pulse accumulator counter can operate in event counter mode even when the timer enable bit, TEN, is clear.

14.4.6 Gated Time Accumulation Mode

Setting the PAMOD bit configures the pulse accumulator for gated time accumulation operation. An active level on the PACNT input pin enables a divided-by-64 clock to drive the pulse accumulator. The PEDGE bit selects low levels or high levels to enable the divided-by-64 clock.

The trailing edge of the active level at the IOC7 pin sets the PAIF. The PAI bit enables the PAIF flag to generate interrupt requests.

Table A-10. Peripheral Configurations for Run & Wait Current Measurement

Peripheral	Configuration
MSCAN	configured to loop-back mode using a bit rate of 1Mbit/s
SPI	configured to master mode, continously transmit data (0x55 or 0xAA) at 1Mbit/s
SCI	configured into loop mode, continously transmit data (0x55) at speed of 57600 baud
PWM	configured to toggle its pins at the rate of 40kHz
ATD	the peripheral is configured to operate at its maximum specified frequency and to continuously convert voltages on all input channels in sequence.
DBG	the module is enabled and the comparators are configured to trigger in outside range.The range covers all the code executed by the core.
TIM	the peripheral shall be configured to output compare mode, pulse accumulator and modulus counter enabled.
COP & RTI	enabled

Table A-11. Run and Wait Current Characteristics

Conditions are: V_{DDR}=5.5V, T_A=125°C, see Table A-9. and Table A-10.							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	IDD Run Current	I_{DDR}		18	20	mA
2	P	IDD Wait Current	I_{DDW}		11	12	mA

Table A-12. Full Stop Current Characteristics

Conditions are: VDDR=5.5V, API see Table A-9.							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Stop Current API disabled							
1	P	150°C	I_{DDS}		250	1100	µA
2	P	-40°C	I_{DDS}		15	35	µA
3	P	25°C,	I_{DDS}		25	50	µA
Stop Current API enabled							
4	C	150°C,	I_{DDS}		270		µA
5	C	-40°C	I_{DDS}		20		µA
6	C	25°C	I_{DDS}		40		µA

A.2.2 Factors Influencing Accuracy

Source resistance, source capacitance and current injection have an influence on the accuracy of the ATD. A further factor is that PortAD pins that are configured as output drivers switching.

A.2.2.1 Port AD Output Drivers Switching

PortAD output drivers switching can adversely affect the ATD accuracy whilst converting the analog voltage on other PortAD pins because the output drivers are supplied from the VDDA/VSSA ATD supply pins. Although internal design measures are implemented to minimize the affect of output driver noise, it is recommended to configure PortAD pins as outputs only for low frequency, low load outputs. The impact on ATD accuracy is load dependent and not specified. The values specified are valid under condition that no PortAD output drivers switch during conversion.

A.2.2.2 Source Resistance

Due to the input pin leakage current as specified in Table A-6 and Table A-7 in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum source resistance R_S specifies results in an error (10-bit resolution) of less than 1/2 LSB (2.5 mV) at the maximum leakage current. If device or operating conditions are less than worst case or leakage-induced error is acceptable, larger values of source resistance of up to 10Kohm are allowed.

A.2.2.3 Source Capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external and the pin capacitance. For a maximum sampling error of the input voltage ≤ 1LSB (10-bit resilution), then the external filter capacitor, $C_f \geq 1024 * (C_{INS}–C_{INN})$.

A.2.2.4 Current Injection

There are two cases to consider.

1. A current is injected into the channel being converted. The channel being stressed has conversion values of $3FF (in 10-bit mode) for analog inputs greater than V_{RH} and $000 for values less than V_{RL} unless the current is higher than specified as disruptive condition.
2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance.

   The additional input voltage error on the converted channel can be calculated as:

   $$V_{ERR} = K * R_S * I_{INJ}$$

   with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

A.10 MSCAN

Table A-25. MSCAN Wake-up Pulse Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	MSCAN wakeup dominant pulse filtered	t_{WUP}	—	—	1.5	µs
2	P	MSCAN wakeup dominant pulse pass	t_{WUP}	5	—	—	µs

A.11 SPI Timing

This section provides electrical parametrics and ratings for the SPI. In Table A-26 the measurement conditions are listed.

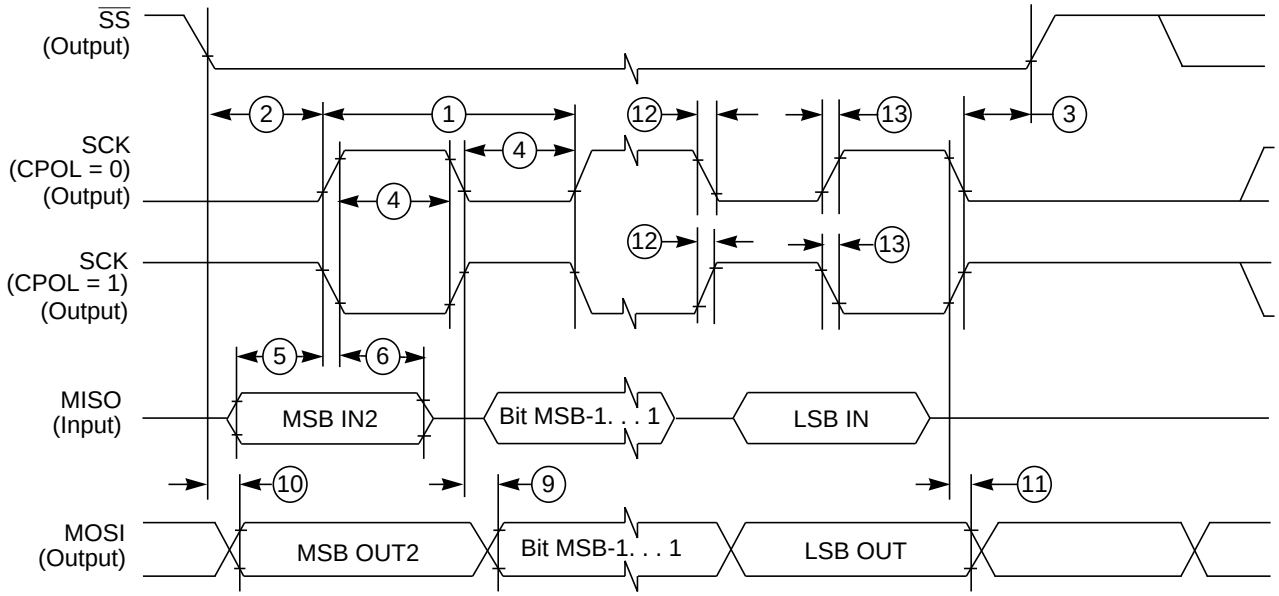
Table A-26. Measurement Conditions

Description	Value	Unit
Drive mode	Full drive mode	—
Load capacitance C_{LOAD}[(1)], on all outputs	50	pF
Thresholds for delay measurement points	(20% / 80%) V_{DDX}	V

1. Timing specified for equal load on all SPI output pins. Avoid asymmetric load.

A.11.1 Master Mode

In Figure A-5 the timing diagram for master mode with transmission format CPHA = 0 is depicted.



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, bit 2... MSB.

Figure A-5. SPI Master Timing (CPHA = 0)