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Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	49
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12p96j0clh

1.9.2 Low Power Operation

The MC9S12P has two static low-power modes Pseudo Stop and Stop Mode. For a detailed description refer to S12CPMU section.

1.10 Security

The MCU security mechanism prevents unauthorized access to the Flash memory. Refer to **Section 5.4.1 Security** and **Section 13.5 Security**

1.11 Resets and Interrupts

Consult the S12 CPU manual and the S12SINT section for information on exception processing.

1.11.1 Resets

Table 1-11. lists all Reset sources and the vector locations. Resets are explained in detail in the **Section Chapter 7 S12 Clock, Reset and Power Management Unit (S12CPMU)**

Table 1-11. Reset Sources and Vector Locations

Vector Address	Reset Source	CCR Mask	Local Enable
$FFFE	Power-On Reset (POR)	None	None
$FFFE	Low Voltage Reset (LVR)	None	None
$FFFE	External pin $\overline{\text{RESET}}$	None	None
$FFFE	Illegal Address Reset	None	None
$FFFC	Clock monitor reset	None	OSCE Bit in CPMUOSC register
$FFFA	COP watchdog reset	None	CR[2:0] in CPMUCOP register

1.11.2 Interrupt Vectors

Table 1-12 lists all interrupt sources and vectors in the default order of priority. The interrupt module (see **Section Chapter 4 Interrupt Module (S12SINTV1)**) provides an interrupt vector base register (IVBR) to relocate the vectors.

Table 1-12. Interrupt Vector Locations (Sheet 1 of 3)

Vector Address[1]	Interrupt Source	CCR Mask	Local Enable	Wake up from STOP	Wakeup from WAIT
Vector base + $F8	Unimplemented instruction trap	None	None	-	-
Vector base+ $F6	SWI	None	None	-	-
Vector base+ $F4	$\overline{\text{XIRQ}}$	X Bit	None	Yes	Yes
Vector base+ $F2	$\overline{\text{IRQ}}$	I bit	IRQCR (IRQEN)	Yes	Yes

2.3.3 Port A Data Register (PORTA)

Address 0x0000 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Reset	0	0	0	0	0	0	0	0

Figure 2-1. Port A Data Register (PORTA)

1. Read: Anytime. The data source is depending on the data direction value.
   Write: Anytime

Table 2-4. PORTA Register Field Descriptions

Field	Description
7-0 PA	**Port A general purpose input/output data**—Data Register The associated pin can be used as general purpose I/O. In general purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the buffered pin input state is read.

2.3.4 Port B Data Register (PORTB)

Address 0x0001 Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Reset	0	0	0	0	0	0	0	0

Figure 2-2. Port B Data Register (PORTB)

1. Read: Anytime. The data source is depending on the data direction value.
   Write: Anytime

Table 2-5. PORTB Register Field Descriptions

Field	Description
7-0 PB	**Port B general purpose input/output data**—Data Register The associated pin can be used as general purpose I/O. In general purpose output mode the register bit value is driven to the pin. If the associated data direction bit is set to 1, a read returns the value of the port register bit, otherwise the buffered pin input state is read.

Address 0x001D Access: User read(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-11. PIM Reserved Register

1. Read: Always reads 0x00
   Write: Unimplemented

2.3.14 IRQ Control Register (IRQCR)

Address 0x001E Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	IRQE	IRQEN	0	0	0	0	0	0
W								
Reset	0	1	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-12. IRQ Control Register (IRQCR)

1. Read: See individual bit descriptions below.
   Write: See individual bit descriptions below.

Table 2-13. IRQCR Register Field Descriptions

Field	Description
7 IRQE	**IRQ select edge sensitive only**— Special mode: Read or write anytime. Normal mode: Read anytime, write once. 1 $\overline{\text{IRQ}}$ pin configured to respond only to falling edges. Falling edges on the $\overline{\text{IRQ}}$ pin will be detected anytime IRQE=1 and will be cleared only upon a reset or the servicing of the $\overline{\text{IRQ}}$ interrupt. 0 $\overline{\text{IRQ}}$ pin configured for low level recognition
6 IRQEN	**IRQ enable**— Read or write anytime. 1 $\overline{\text{IRQ}}$ pin is connected to interrupt logic 0 $\overline{\text{IRQ}}$ pin is disconnected from interrupt logic

2.3.15 PIM Reserved Register

This register is reserved for factory testing of the PIM module and is not available in normal operation. Writing to this register when in special modes can alter the pin functionality.

Chapter 3
Memory Map Control (S12PMMCV1)

Table 3-1. Revision History Table

Table 3-2.

Rev. No. (Item No.)	Date (Submitted By)	Sections Affected	Substantial Change(s)
01.03	10.JAN.2008	General	Minor Changes
01.04	13.JAN.2010	Figure 3-2	Added reserved registers
01.05	22.APR.2010	General	Removed references to the MMCCTL1 register

3.1 Introduction

The S12PMMC module controls the access to all internal memories and peripherals for the CPU12 and S12SBDM module. It regulates access priorities and determines the address mapping of the on-chip ressources. Figure 3-1 shows a block diagram of the S12PMMC module.

3.1.1 Glossary

Table 3-3. Glossary Of Terms

Term	Definition
Local Addresses	Address within the CPU12's Local Address Map (Figure 3-10)
Global Addresse	Address within the Global Address Map (Figure 3-10)
Aligned Bus Access	Bus access to an even address.
Misaligned Bus Access	Bus access to an odd address.
NS	Normal Single-Chip Mode
SS	Special Single-Chip Mode
Unimplemented Address Ranges	Address ranges which are not mapped to any on-chip ressource.
P-Flash	Program Flash
D-Plash	Data Flash
NVM	Non-volatile Memory; P-Flash or D-Flash
IFR	NVM Information Row. Refer to FTMRC Block Guide

Table 3-6. DIRECT Field Descriptions

Field	Description
7–0 DP[15:8]	**Direct Page Index Bits 15–8** — These bits are used by the CPU when performing accesses using the direct addressing mode. These register bits form bits [15:8] of the local address (see Figure 3-6).

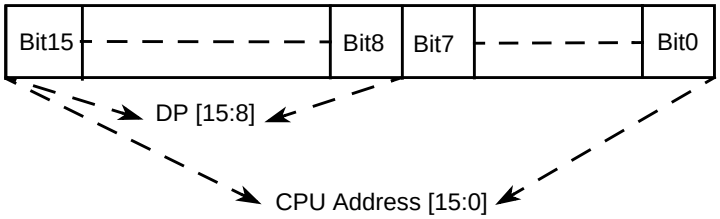

Figure 3-6. DIRECT Address Mapping

Example 3-1. This example demonstrates usage of the Direct Addressing Mode

```
MOVB      #$80,DIRECT       ;Set DIRECT register to 0x80. Write once only.
                            ;Global data accesses to the range 0xXX_80XX can be direct.
                            ;Logical data accesses to the range 0x80XX are direct.

LDY       <$00              ;Load the Y index register from 0x8000 (direct access).
                            ;< operator forces direct access on some assemblers but in
                            ;many cases assemblers are "direct page aware" and can
                            ;automatically select direct mode.
```

3.3.2.3 Program Page Index Register (PPAGE)

Address: 0x0030

	7	6	5	4	3	2	1	0
R	0	0	0	0	PIX3	PIX2	PIX1	PIX0
W								
Reset	0	0	0	0	1	1	1	0

Figure 3-7. Program Page Index Register (PPAGE)

Read: Anytime

Write: Anytime

These four index bits are used to map 16KB blocks into the Flash page window located in the local (CPU or BDM) memory map from address 0x8000 to address 0xBFFF (see Figure 3-8). This supports accessing up to 256 KB of Flash (in the Global map) within the 64KB Local map. The PPAGE index register is effectively used to construct paged Flash addresses in the Local map format. The CPU has special access to read and write this register directly during execution of CALL and RTC instructions.

access causes a match. Thus if configured for a byte access of a particular address, a word access covering the same address does not lead to match.

Assuming the access direction is not qualified (RWE=0), for simplicity, the size access considerations are shown in Table 6-33.

Table 6-33. Comparator B Access Size Considerations

Condition For Valid Match	Comp B Address	RWE	SZE	SZ8	Examples
Word and byte accesses of ADDR[n]	ADDR[n](1)	0	0	X	MOVB #$BYTE ADDR[n] MOVW #$WORD ADDR[n]
Word accesses of ADDR[n] only	ADDR[n]	0	1	0	MOVW #$WORD ADDR[n] LDD ADDR[n]
Byte accesses of ADDR[n] only	ADDR[n]	0	1	1	MOVB #$BYTE ADDR[n] LDAB ADDR[n]

1. A word access of ADDR[n-1] also accesses ADDR[n] but does not generate a match.
The comparator address register must contain the exact address from the code.

Access direction can also be used to qualify a match for Comparator B in the same way as described for Comparator C in Table 6-32.

6.4.2.1.3 Comparator A

Comparator A offers address, direction (R/W), access size (word/byte) and data bus comparison.

Table 6-34 lists access considerations with data bus comparison. On word accesses the data byte of the lower address is mapped to DBGADH. Access direction can also be used to qualify a match for Comparator A in the same way as described for Comparator C in Table 6-32.

Table 6-34. Comparator A Matches When Accessing ADDR[n]

SZE	SZ	DBGADHM, DBGADLM	Access DH=DBGADH, DL=DBGADL	Comment
0	X	$0000	Byte Word	No databus comparison
0	X	$FF00	Byte, data(ADDR[n])=DH Word, data(ADDR[n])=DH, data(ADDR[n+1])=X	Match data(ADDR[n])
0	X	$00FF	Word, data(ADDR[n])=X, data(ADDR[n+1])=DL	Match data(ADDR[n+1])
0	X	$00FF	Byte, data(ADDR[n])=X, data(ADDR[n+1])=DL	Possible unintended match
0	X	$FFFF	Word, data(ADDR[n])=DH, data(ADDR[n+1])=DL	Match data(ADDR[n], ADDR[n+1])
0	X	$FFFF	Byte, data(ADDR[n])=DH, data(ADDR[n+1])=DL	Possible unintended match
1	0	$0000	Word	No databus comparison
1	0	$00FF	Word, data(ADDR[n])=X, data(ADDR[n+1])=DL	Match only data at ADDR[n+1]
1	0	$FF00	Word, data(ADDR[n])=DH, data(ADDR[n+1])=X	Match only data at ADDR[n]
1	0	$FFFF	Word, data(ADDR[n])=DH, data(ADDR[n+1])=DL	Match data at ADDR[n] & ADDR[n+1]
1	1	$0000	Byte	No databus comparison
1	1	$FF00	Byte, data(ADDR[n])=DH	Match data at ADDR[n]

each trace buffer entry. In Detail mode CINF comprises of R/W and size access information (CRW and CSZ respectively).

Single byte data accesses in Detail Mode are always stored to the low byte of the trace buffer (DATAL) and the high byte is cleared. When tracing word accesses, the byte at the lower address is always stored to trace buffer byte1 and the byte at the higher address is stored to byte0.

Table 6-37. Trace Buffer Organization (Normal,Loop1,Detail modes)

Mode	Entry Number	4-bits	8-bits	8-bits
		Field 2	Field 1	Field 0
Detail Mode	Entry 1	CINF1,ADRH1	ADRM1	ADRL1
		0	DATAH1	DATAL1
	Entry 2	CINF2,ADRH2	ADRM2	ADRL2
		0	DATAH2	DATAL2
Normal/Loop1 Modes	Entry 1	PCH1	PCM1	PCL1
	Entry 2	PCH2	PCM2	PCL2

6.4.5.3.1 Information Bit Organization

The format of the bits is dependent upon the active trace mode as described below.

Field2 Bits in Detail Mode

Bit 3	Bit 2	Bit 1	Bit 0
CSZ	CRW	ADDR[17]	ADDR[16]

Figure 6-25. Field2 Bits in Detail Mode

In Detail Mode the CSZ and CRW bits indicate the type of access being made by the CPU.

Table 6-38. Field Descriptions

Bit	Description
3 CSZ	**Access Type Indicator**— This bit indicates if the access was a byte or word size when tracing in Detail Mode 0 Word Access 1 Byte Access
2 CRW	**Read Write Indicator** — This bit indicates if the corresponding stored address corresponds to a read or write access when tracing in Detail Mode. 0 Write Access 1 Read Access
1 ADDR[17]	**Address Bus bit 17**— Corresponds to system address bus bit 17.
0 ADDR[16]	**Address Bus bit 16**— Corresponds to system address bus bit 16.

7.3 Memory Map and Registers

This section provides a detailed description of all registers accessible in the S12CPMU.

7.3.1 Module Memory Map

The S12CPMU registers are shown in Figure 7-3.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0034	CPMU SYNR	R	VCOFRQ[1:0]		SYNDIV[5:0]					
		W								
0x0035	CPMU REFDIV	R	REFFRQ[1:0]		0	0	REFDIV[3:0]			
		W								
0x0036	CPMU POSTDIV	R	0	0	0	POSTDIV[4:0]				
		W								
0x0037	CPMUFLG	R	RTIF	PORF	LVRF	LOCKIF	LOCK	ILAF	OSCIF	UPOSC
		W								
0x0038	CPMUINT	R	RTIE	0	0	LOCKIE	0	0	OSCIE	0
		W								
0x0039	CPMUCLKS	R	PLLSEL	PSTP	0	0	PRE	PCE	RTI OSCSEL	COP OSCSEL
		W								
0x003A	CPMUPLL	R	0	0	FM1	FM0	0	0	0	0
		W								
0x003B	CPMURTI	R	RTDEC	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		W								
0x003C	CPMUCOP	R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		W			WRTMASK					
0x003D	RESERVED CPMUTEST0	R	0	0	0	0	0	0	0	0
		W								
0x003E	RESERVED CPMUTEST1	R	0	0	0	0	0	0	0	0
		W								
0x003F	CPMU ARMCOP	R	0	0	0	0	0	0	0	0
		W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x02F0	CPMU HTCTL	R	0	0	VSEL	0	HTE	HTDS	HTIE	HTIF
		W								
0x02F1	CPMU LVCTL	R	0	0	0	0	0	LVDS	LVIE	LVIF
		W								
0x02F2	CPMU APICTL	R	APICLK	0	0	APIES	APIEA	APIFE	APIE	APIF
		W								
			= Unimplemented or Reserved							

Figure 7-3. CPMU Register Summary

7.3.2.18 Reserved Register CPMUTEST3

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in special mode can alter the S12CPMU's functionality.

0x02F6

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 7-23. Reserved Register (CPMUTEST3)

Read: Anytime

Write: Only in special mode

7.4.6 System Clock Configurations

7.4.6.1 PLL Engaged Internal Mode (PEI)

This mode is the default mode after System Reset or Power-On Reset.

The Bus Clock is based on the PLLCLK, the reference clock for the PLL is internally generated (IRC1M). The PLL is configured to 64 MHz VCOCLK with POSTDIV set to 0x03. If locked (LOCK=1) this results in a PLLCLK of 16 MHz and a Bus Clock of 8 MHz. The PLL can be re-configured to other bus frequencies.

The clock sources for COP and RTI are based on the internal reference clock generator (IRC1M).

7.4.6.2 PLL Engaged External Mode (PEE)

In this mode, the Bus Clock is based on the PLLCLK as well (like PEI). The reference clock for the PLL is based on the external oscillator. The adaptive spike filter and detection logic which uses the VCOCLK to filter and qualify the external oscillator clock can be enabled.

The clock sources for COP and RTI can be based on the internal reference clock generator or on the external oscillator clock.

This mode can be entered from default mode PEI by performing the following steps:

1. Configure the PLL for desired bus frequency.
2. Optionally the adaptive spike filter and detection logic can be enabled by calculating the integer value for the OSCFIL[4:0] bits and setting the bandwidth (OSCBW) accordingly.
3. Enable the external oscillator (OSCE bit).
4. Wait for the PLL being locked (LOCK = 1) and the oscillator to start-up and additionally being qualified if the adaptive spike filter is enabled (UPOSC =1).
5. Clear all flags in the CPMUFLG register to be able to detect any future status bit change.
6. Optionally status interrupts can be enabled (CPMUINT register).

Since the adaptive spike filter (filter and detection logic) uses the VCOCLK to continuously filter and qualify the external oscillator clock, loosing PLL lock status (LOCK=0) means loosing the oscillator status information as well (UPOSC=0).

The impact of loosing the oscillator status in PEE mode is as follows:

- The PLLCLK is derived from the VCO clock (with its actual frequency) divided by four until the PLL locks again.

Application software needs to be prepared to deal with the impact of loosing the oscillator status at any time.

— a) the 14 most significant bits of the extended identifier plus the SRR and IDE bits of CAN 2.0B messages or

— b) the 11 bits of the standard identifier, the RTR and IDE bits of CAN 2.0A/B messages. Figure 8-41 shows how the first 32-bit filter bank (CANIDAR0–CANIDA3, CANIDMR0–3CANIDMR) produces filter 0 and 1 hits. Similarly, the second filter bank (CANIDAR4–CANIDAR7, CANIDMR4–CANIDMR7) produces filter 2 and 3 hits.

- Eight identifier acceptance filters, each to be applied to the first 8 bits of the identifier. This mode implements eight independent filters for the first 8 bits of a CAN 2.0A/B compliant standard identifier or a CAN 2.0B compliant extended identifier. Figure 8-42 shows how the first 32-bit filter bank (CANIDAR0–CANIDAR3, CANIDMR0–CANIDMR3) produces filter 0 to 3 hits. Similarly, the second filter bank (CANIDAR4–CANIDAR7, CANIDMR4–CANIDMR7) produces filter 4 to 7 hits.
- Closed filter. No CAN message is copied into the foreground buffer RxFG, and the RXF flag is never set.

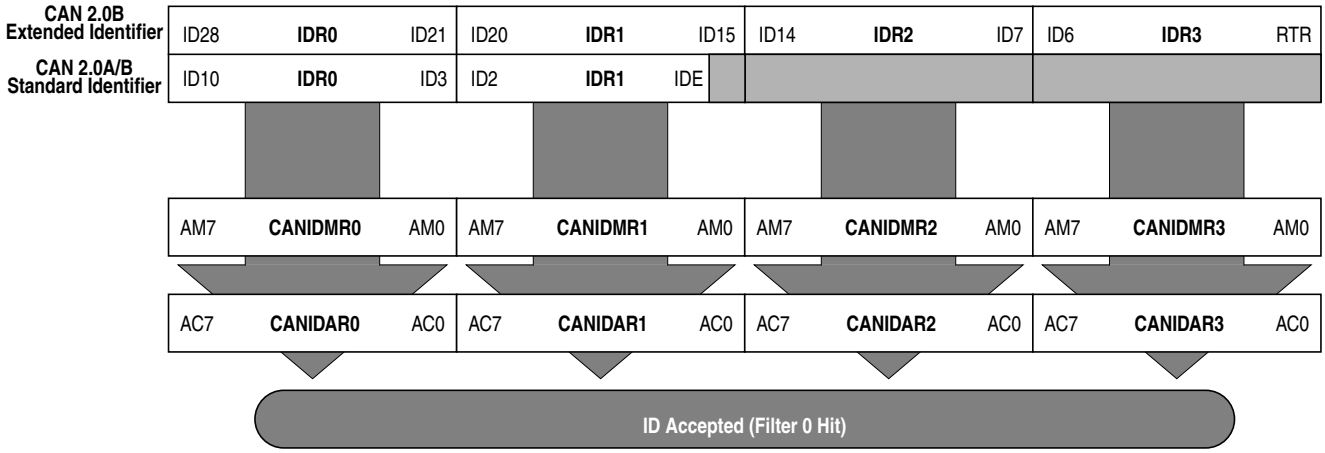

Figure 8-40. 32-bit Maskable Identifier Acceptance Filter

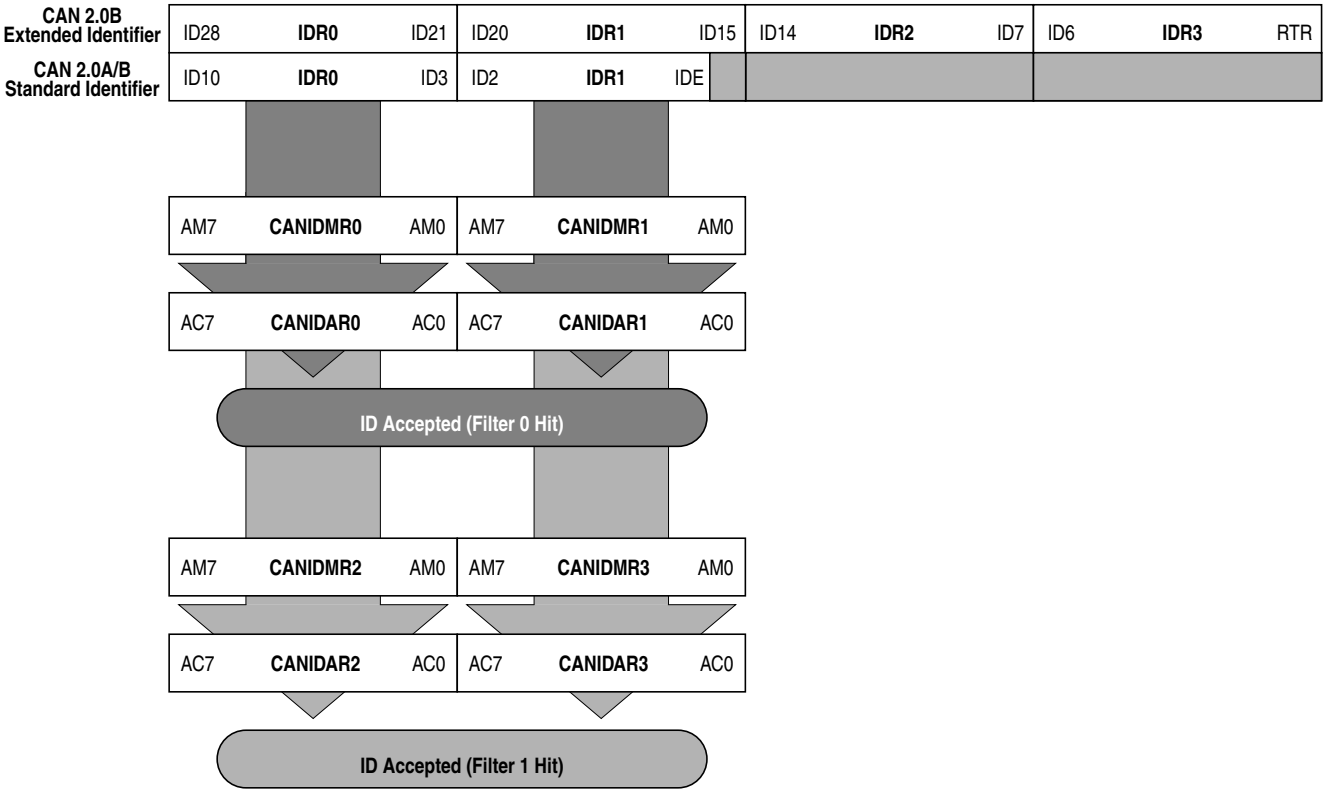

Figure 8-41. 16-bit Maskable Identifier Acceptance Filters

Table 9-15. Analog Input Channel Select Coding

SC	CD	CC	CB	CA	Analog Input Channel
0	0	0	0	0	AN0
	0	0	0	1	AN1
	0	0	1	0	AN2
	0	0	1	1	AN3
	0	1	0	0	AN4
	0	1	0	1	AN5
	0	1	1	0	AN6
	0	1	1	1	AN7
	1	0	0	0	AN8
	1	0	0	1	AN9
	1	0	1	0	AN9
	1	0	1	1	AN9
	1	1	0	0	AN9
	1	1	0	1	AN9
	1	1	1	0	AN9
	1	1	1	1	AN9
1	0	0	0	0	Reserved
	0	0	0	1	SPECIAL17
	0	0	1	X	Reserved
	0	1	0	0	V_{RH}
	0	1	0	1	V_{RL}
	0	1	1	0	$(V_{RH}+V_{RL}) / 2$
	0	1	1	1	Reserved
	1	X	X	X	Reserved

9.3.2.7 ATD Status Register 0 (ATDSTAT0)

This register contains the Sequence Complete Flag, overrun flags for external trigger and FIFO mode, and the conversion counter.

Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	SCF	0	ETORF	FIFOR	CC3	CC2	CC1	CC0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-9. ATD Status Register 0 (ATDSTAT0)

9.4.1 Analog Sub-Block

The analog sub-block contains all analog electronics required to perform a single conversion. Separate power supplies V_{DDA} and V_{SSA} allow to isolate noise of other MCU circuitry from the analog sub-block.

9.4.1.1 Sample and Hold Machine

The Sample and Hold (S/H) Machine accepts analog signals from the external world and stores them as capacitor charge on a storage node.

During the sample process the analog input connects directly to the storage node.

The input analog signals are unipolar and must fall within the potential range of V_{SSA} to V_{DDA}.

During the hold process the analog input is disconnected from the storage node.

9.4.1.2 Analog Input Multiplexer

The analog input multiplexer connects one of the 10 external analog input channels to the sample and hold machine.

9.4.1.3 Analog-to-Digital (A/D) Machine

The A/D Machine performs analog to digital conversions. The resolution is program selectable at either 8 or 10 or 12 bits. The A/D machine uses a successive approximation architecture. It functions by comparing the stored analog sample potential with a series of digitally generated analog potentials. By following a binary search algorithm, the A/D machine locates the approximating potential that is nearest to the sampled potential.

When not converting the A/D machine is automatically powered down.

Only analog input signals within the potential range of V_{RL} to V_{RH} (A/D reference potentials) will result in a non-railed digital output code.

9.4.2 Digital Sub-Block

This subsection explains some of the digital features in more detail. See Section 9.3.2, “Register Descriptions” for all details.

9.4.2.1 External Trigger Input

The external trigger feature allows the user to synchronize ATD conversions to the external environment events rather than relying on software to signal the ATD module when ATD conversions are to take place. The external trigger signal (out of reset ATD channel 9, configurable in ATDCTL1) is programmable to

Write: Anytime

Table 11-12. SCISR2 Field Descriptions

Field	Description
7 AMAP	**Alternative Map** — This bit controls which registers sharing the same address space are accessible. In the reset condition the SCI behaves as previous versions. Setting AMAP=1 allows the access to another set of control and status registers and hides the baud rate and SCI control Register 1. 0 The registers labelled SCIBDH (0x0000),SCIBDL (0x0001), SCICR1 (0x0002) are accessible 1 The registers labelled SCIASR1 (0x0000),SCIACR1 (0x0001), SCIACR2 (0x00002) are accessible
4 TXPOL	**Transmit Polarity** — This bit control the polarity of the transmitted data. In NRZ format, a one is represented by a mark and a zero is represented by a space for normal polarity, and the opposite for inverted polarity. In IrDA format, a zero is represented by short high pulse in the middle of a bit time remaining idle low for a one for normal polarity, and a zero is represented by short low pulse in the middle of a bit time remaining idle high for a one for inverted polarity. 0 Normal polarity 1 Inverted polarity
3 RXPOL	**Receive Polarity** — This bit control the polarity of the received data. In NRZ format, a one is represented by a mark and a zero is represented by a space for normal polarity, and the opposite for inverted polarity. In IrDA format, a zero is represented by short high pulse in the middle of a bit time remaining idle low for a one for normal polarity, and a zero is represented by short low pulse in the middle of a bit time remaining idle high for a one for inverted polarity. 0 Normal polarity 1 Inverted polarity
2 BRK13	**Break Transmit Character Length** — This bit determines whether the transmit break character is 10 or 11 bit respectively 13 or 14 bits long. The detection of a framing error is not affected by this bit. 0 Break character is 10 or 11 bit long 1 Break character is 13 or 14 bit long
1 TXDIR	**Transmitter Pin Data Direction in Single-Wire Mode** — This bit determines whether the TXD pin is going to be used as an input or output, in the single-wire mode of operation. This bit is only relevant in the single-wire mode of operation. 0 TXD pin to be used as an input in single-wire mode 1 TXD pin to be used as an output in single-wire mode
0 RAF	**Receiver Active Flag** — RAF is set when the receiver detects a logic 0 during the RT1 time period of the start bit search. RAF is cleared when the receiver detects an idle character. 0 No reception in progress 1 Reception in progress

11.3.2.9 SCI Data Registers (SCIDRH, SCIDRL)

Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	R8	T8	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 11-12. SCI Data Registers (SCIDRH)

The main element of the SPI system is the SPI data register. The n-bit[1] data register in the master and the n-bit[1] data register in the slave are linked by the MOSI and MISO pins to form a distributed 2n-bit[1] register. When a data transfer operation is performed, this 2n-bit[1] register is serially shifted n[1] bit positions by the S-clock from the master, so data is exchanged between the master and the slave. Data written to the master SPI data register becomes the output data for the slave, and data read from the master SPI data register after a transfer operation is the input data from the slave.

A read of SPISR with SPTEF = 1 followed by a write to SPIDR puts data into the transmit data register. When a transfer is complete and SPIF is cleared, received data is moved into the receive data register. This data register acts as the SPI receive data register for reads and as the SPI transmit data register for writes. A common SPI data register address is shared for reading data from the read data buffer and for writing data to the transmit data register.

The clock phase control bit (CPHA) and a clock polarity control bit (CPOL) in the SPI control register 1 (SPICR1) select one of four possible clock formats to be used by the SPI system. The CPOL bit simply selects a non-inverted or inverted clock. The CPHA bit is used to accommodate two fundamentally different protocols by sampling data on odd numbered SCK edges or on even numbered SCK edges (see Section 12.4.3, “Transmission Formats”).

The SPI can be configured to operate as a master or as a slave. When the MSTR bit in SPI control register1 is set, master mode is selected, when the MSTR bit is clear, slave mode is selected.

NOTE

A change of CPOL or MSTR bit while there is a received byte pending in the receive shift register will destroy the received byte and must be avoided.

12.4.1 Master Mode

The SPI operates in master mode when the MSTR bit is set. Only a master SPI module can initiate transmissions. A transmission begins by writing to the master SPI data register. If the shift register is empty, data immediately transfers to the shift register. Data begins shifting out on the MOSI pin under the control of the serial clock.

- Serial clock

  The SPR2, SPR1, and SPR0 baud rate selection bits, in conjunction with the SPPR2, SPPR1, and SPPR0 baud rate preselection bits in the SPI baud rate register, control the baud rate generator and determine the speed of the transmission. The SCK pin is the SPI clock output. Through the SCK pin, the baud rate generator of the master controls the shift register of the slave peripheral.
- MOSI, MISO pin

  In master mode, the function of the serial data output pin (MOSI) and the serial data input pin (MISO) is determined by the SPC0 and BIDIROE control bits.
- $\overline{SS}$ pin

  If MODFEN and SSOE are set, the $\overline{SS}$ pin is configured as slave select output. The $\overline{SS}$ output becomes low during each transmission and is high when the SPI is in idle state.

  If MODFEN is set and SSOE is cleared, the $\overline{SS}$ pin is configured as input for detecting mode fault error. If the $\overline{SS}$ input becomes low this indicates a mode fault error where another master tries to

1. n depends on the selected transfer width, please refer to Section 12.3.2.2, “SPI Control Register 2 (SPICR2)

P-Flash phrase containing the D-Flash protection byte during the reset sequence, the DPOPEN bit will be cleared and DPS bits will be set to leave the D-Flash memory fully protected.

Trying to alter data in any protected area in the D-Flash memory will result in a protection violation error and the FPVIOL bit will be set in the FSTAT register. Block erase of the D-Flash memory is not possible if any of the D-Flash sectors are protected.

Table 13-21. DFPROT Field Descriptions

Field	Description
7 DPOPEN	**D-Flash Protection Control** 0 Enables D-Flash memory protection from program and erase with protected address range defined by DPS bits 1 Disables D-Flash memory protection from program and erase
3–0 DPS[3:0]	**D-Flash Protection Size** — The DPS[3:0] bits determine the size of the protected area in the D-Flash memory as shown in Table 13-22.

Table 13-22. D-Flash Protection Address Range

DPS[3:0]	Global Address Range	Protected Size
0000	0x0_4400 – 0x0_44FF	256 bytes
0001	0x0_4400 – 0x0_45FF	512 bytes
0010	0x0_4400 – 0x0_46FF	768 bytes
0011	0x0_4400 – 0x0_47FF	1024 bytes
0100	0x0_4400 – 0x0_48FF	1280 bytes
0101	0x0_4400 – 0x0_49FF	1536 bytes
0110	0x0_4400 – 0x0_4AFF	1792 bytes
0111	0x0_4400 – 0x0_4BFF	2048 bytes
1000	0x0_4400 – 0x0_4CFF	2304 bytes
1001	0x0_4400 – 0x0_4DFF	2560 bytes
1010	0x0_4400 – 0x0_4EFF	2816 bytes
1011	0x0_4400 – 0x0_4FFF	3072 bytes
1100	0x0_4400 – 0x0_50FF	3328 bytes
1101	0x0_4400 – 0x0_51FF	3584 bytes
1110	0x0_4400 – 0x0_52FF	3840 bytes
1111	0x0_4400 – 0x0_53FF	4096 bytes

13.3.2.11 Flash Common Command Object Register (FCCOB)

The FCCOB is an array of six words addressed via the CCOBIX index found in the FCCOBIX register. Byte wide reads and writes are allowed to the FCCOB register.

Table A-16. ATD Conversion Performance 5V range

Conditions are shown in Table A-4. unless otherwise noted. $V_{REF} = V_{RH} - V_{RL} = 5.12V$. $f_{ATDCLK} = 8.0MHz$
The values are tested to be valid with no PortAD output drivers switching simultaneous with conversions.

Num	C	Rating[1]		Symbol	Min	Typ	Max	Unit
1	P	Resolution	12-Bit	LSB		1.25		mV
2	P	Differential Nonlinearity	12-Bit	DNL	-4	±2	4	counts
3	P	Integral Nonlinearity	12-Bit	INL	-5	±2.5	5	counts
4	P	Absolute Error[2]	12-Bit	AE	-7	±4	7	counts
5	C	Resolution	10-Bit	LSB		5		mV
6	C	Differential Nonlinearity	10-Bit	DNL	-1	±0.5	1	counts
7	C	Integral Nonlinearity	10-Bit	INL	-2	±1	2	counts
8	C	Absolute Error[2.]	10-Bit	AE	-3	±2	3	counts
9	C	Resolution	8-Bit	LSB		20		mV
10	C	Differential Nonlinearity	8-Bit	DNL	-0.5	±0.3	0.5	counts
11	C	Integral Nonlinearity	8-Bit	INL	-1	±0.5	1	counts
12	C	Absolute Error[2.]	8-Bit	AE	-1.5	±1	1.5	counts

1. The 8-bit and 10-bit mode operation is structurally tested in production test. Absolute values are tested in 12-bit mode.
2. These values include the quantization error which is inherently 1/2 count for any A/D converter.

Table A-17. ATD Conversion Performance 3.3V range

Conditions are shown in Table A-4. unless otherwise noted. $V_{REF} = V_{RH} - V_{RL} = 3.3V$. $f_{ATDCLK} = 8.0MHz$
The values are tested to be valid with no PortAD output drivers switching simultaneous with conversions.

Num	C	Rating[1]		Symbol	Min	Typ	Max	Unit
1	P	Resolution	12-Bit	LSB		0.80		mV
2	P	Differential Nonlinearity	12-Bit	DNL	-6	±3	6	counts
3	P	Integral Nonlinearity	12-Bit	INL	-7	±3	7	counts
4	P	Absolute Error[2]	12-Bit	AE	-8	±4	8	counts
5	C	Resolution	10-Bit	LSB		3.22		mV
6	C	Differential Nonlinearity	10-Bit	DNL	-1.5	±1	1.5	counts
7	C	Integral Nonlinearity	10-Bit	INL	-2	±1	2	counts
8	C	Absolute Error[2.]	10-Bit	AE	-3	±2	3	counts
9	C	Resolution	8-Bit	LSB		12.89		mV
10	C	Differential Nonlinearity	8-Bit	DNL	-0.5	±0.3	0.5	counts
11	C	Integral Nonlinearity	8-Bit	INL	-1	±0.5	1	counts
12	C	Absolute Error[2.]	8-Bit	AE	-1.5	±1	1.5	counts

1. The 8-bit and 10-bit mode operation is structurally tested in production test. Absolute values are tested in 12-bit mode.
2. These values include the quantization error which is inherently 1/2 count for any A/D converter.

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NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

TITLE:	CASE NUMBER: 841B-02	
QUAD FLAT PACKAGE, 80 LEAD, 14 X 14 X 2.2 PKG, 0.65 LEAD PITCH	STANDARD: NON-JEDEC	
	PACKAGE CODE: 6020	SHEET: 3 OF 4