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Details

Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.72V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TFQFN Exposed Pad
Supplier Device Package	48-QFN-EP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12p96j0mftr

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1.9.2 Low Power Operation

The MC9S12P has two static low-power modes Pseudo Stop and Stop Mode. For a detailed description refer to S12CPMU section.

1.10 Security

The MCU security mechanism prevents unauthorized access to the Flash memory. Refer to Section 5.4.1 Security and Section 13.5 Security

1.11 Resets and Interrupts

Consult the S12 CPU manual and the S12SINT section for information on exception processing.

1.11.1 Resets

Table 1-11. lists all Reset sources and the vector locations. Resets are explained in detail in the Section Chapter 7 S12 Clock, Reset and Power Management Unit (S12CPMU)

Vector Address	Reset Source	CCR Mask	Local Enable
\$FFFE	Power-On Reset (POR)	None	None
\$FFFE	Low Voltage Reset (LVR)	None	None
\$FFFE	External pin RESET	None	None
\$FFFE	Illegal Address Reset	None	None
\$FFFC	Clock monitor reset	None	OSCE Bit in CPMUOSC register
\$FFFA	COP watchdog reset	None	CR[2:0] in CPMUCOP register

Table 1-11. Reset Sources and Vector Locations

1.11.2 Interrupt Vectors

Table 1-12 lists all interrupt sources and vectors in the default order of priority. The interrupt module (see **Section Chapter 4 Interrupt Module (S12SINTV1)**) provides an interrupt vector base register (IVBR) to relocate the vectors.

 Table 1-12. Interrupt Vector Locations (Sheet 1 of 3)

Vector Address ⁽¹⁾	Interrupt Source	CCR Mask	Local Enable	Wake up from STOP	Wakeup from WAIT
Vector base + \$F8	Unimplemented instruction trap	None	None	-	-
Vector base+ \$F6	SWI	None	None	-	-
Vector base+ \$F4	XIRQ	X Bit	None	Yes	Yes
Vector base+ \$F2	ĪRQ	I bit	IRQCR (IRQEN)	Yes	Yes

Device Overview MC9S12P-Family

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1.12 COP Configuration

The COP time-out rate bits CR[2:0] and the WCOP bit in the CPMUCOP register at address 0x003C are loaded from the Flash register FOPT. See Table 1-13 and Table 1-14 for coding. The FOPT register is loaded from the Flash configuration field byte at global address 0x3_FF0E during the reset sequence.

NV[2:0] in FOPT Register	CR[2:0] in COPCTL Register
000	111
001	110
010	101
011	100
100	011
101	010
110	001
111	000

Table 1-13. Initial COP Rate Configuratio	Table [•]	1-13.	Initial	COP	Rate	Configuratio
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Table 1-14. Initial WCOP Configuration

NV[3] in FOPT Register	WCOP in COPCTL Register
1	0
0	1

1.13 ATD External Trigger Input Connection

The ATD module includes external trigger inputs ETRIG0 and ETRIG1. The external trigger allows the user to synchronize ATD conversion to external trigger events. Table 1-15 shows the connection of the external trigger inputs.

Table 1-15. ATD	External	Trigger	Sources
-----------------	----------	---------	---------

External Trigger Input	Connectivity
ETRIG0	PWM channel 1
ETRIG1	PWM channel 3

Consult the ATD section for information about the analog-to-digital converter module. References to freeze mode are equivalent to active BDM mode.

egration Module (S12PPIMV1)

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Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x026D PPSJ	R W	PPSJ7	PPSJ6	0	0	0	PPSJ2	PPSJ1	PPSJ0
0x026E PIEJ	R W	PIEJ7	PIEJ6	0	0	0	PIEJ2	PIEJ1	PIEJ0
0x026F PIFJ	R W	PIFJ7	PIFJ6	0	0	0	PIFJ2	PIFJ1	PIFJ0
0x0270 PT0AD	R W	0	0	0	0	0	0	PT0AD1	PT0AD0
0x0271 PT1AD	R W	PT1AD7	PT1AD6	PT1AD5	PT1AD4	PT1AD3	PT1AD2	PT1AD1	PT1AD0
0x0272 DDR0AD	R W	0	0	0	0	0	0	DDR0AD1	DDR0AD0
0x0273 DDR1AD	R W	DDR1AD7	DDR1AD6	DDR1AD5	DDR1AD4	DDR1AD3	DDR1AD2	DDR1AD1	DDR1AD0
0x0274 RDR0AD	R W	0	0	0	0	0	0	RDR0AD1	RDR0AD0
0x0275 RDR1AD	R W	RDR1AD7	RDR1AD6	RDR1AD5	RDR1AD4	RDR1AD3	RDR1AD2	RDR1AD1	RDR1AD0
0x0276 PER0AD	R W	0	0	0	0	0	0	PER0AD1	PER0AD0
0x0277 PER1AD	R W	PER1AD7	PER1AD6	PER1AD5	PER1AD4	PER1AD3	PER1AD2	PER1AD1	PER1AD0
0x0278 Reserved	R W	0	0	0	0	0	0	0	0
0x0279 Reserved	R W	0	0	0	0	0	0	0	0
0x027A Reserved	R W	0	0	0	0	0	0	0	0
0x027B Reserved	R W	0	0	0	0	0	0	0	0
	[= Unimpleme	ented or Reser	ved				



3.5.1 Chip Bus Control

The S12PMMC controls the address buses and the data buses that interface the bus masters (CPU12, S12SBDM) with the rest of the system (master buses). In addition the MMC handles all CPU read data bus swapping operations. All internal resources are connected to specific target buses (see Figure 3-12).



Figure 3-12. S12I platform

3.5.1.1 Master Bus Prioritization regarding Access Conflicts on Target Buses

The arbitration scheme allows only one master to be connected to a target at any given time. The following rules apply when prioritizing accesses from different masters to the same target bus:

- CPU12 always has priority over BDM.
- BDM has priority over CPU12 when its access is stalled for more than 128 cycles. In the later case the CPU will be stalled after finishing the current operation and the BDM will gain access to the bus.

3.5.2 Interrupts

The MMC does not generate any interrupts.





Register Global Address 0x3_FF06

Read: All modes through BDM operation when not secured

Write: All modes through BDM operation when not secured

NOTE

When BDM is made active, the CPU stores the content of its CCR register in the BDMCCR register. However, out of special single-chip reset, the BDMCCR is set to 0xD8 and not 0xD0 which is the reset value of the CCR register in this CPU mode. Out of reset in all other modes the BDMCCR register is read zero.

When entering background debug mode, the BDM CCR holding register is used to save the condition code register of the user's program. It is also used for temporary storage in the standard BDM firmware mode. The BDM CCR holding register can be written to modify the CCR value.

5.3.2.2 BDM Program Page Index Register (BDMPPR)

Register Global Address 0x3_FF08



Figure 5-5. BDM Program Page Register (BDMPPR)

Read: All modes through BDM operation when not secured

Write: All modes through BDM operation when not secured

 Table 5-3. BDMPPR Field Descriptions

Field	Description
7 BPAE	BDM Program Page Access Enable Bit — BPAE enables program page access for BDM hardware and firmware read/write instructions The BDM hardware commands used to access the BDM registers (READ_BD and WRITE_BD) can not be used for global accesses even if the BGAE bit is set.0BDM Program Paging disabled 11BDM Program Paging enabled
3–0 BPP[3:0]	BDM Program Page Index Bits 3–0 — These bits define the selected program page. For more detailed information regarding the program page window scheme, please refer to the S12S_MMC Block Guide.

Field	Description
3–2 TRCMOD	Trace Mode Bits — See 6.4.5.2 for detailed Trace Mode descriptions. In Normal Mode, change of flow information is stored. In Loop1 Mode, change of flow information is stored but redundant entries into trace memory are inhibited. In Detail Mode, address and data for all memory and register accesses is stored. In Compressed Pure PC mode the program counter value for each instruction executed is stored. See Table 6-8.
0 TALIGN	 Trigger Align Bit — This bit controls whether the trigger is aligned to the beginning or end of a tracing session. 0 Trigger at end of stored data 1 Trigger before storing data

Table 6-7. DBGTCR Field Descriptions (continued)

Table 6-8. TRCMOD Trace Mode Bit Encoding

TRCMOD	Description
00	Normal
01	Loop1
10	Detail
11	Compressed Pure PC

6.3.2.4 Debug Control Register2 (DBGC2)

Address: 0x0023



Figure 6-6. Debug Control Register2 (DBGC2)

Read: Anytime

Write: Anytime the module is disarmed.

This register configures the comparators for range matching.

Table 6-9. DBGC2 Field Descriptions

Field	Description
1–0 ABCM[1:0]	A and B Comparator Match Control — These bits determine the A and B comparator match mapping as described in Table 6-10.

Table 6-10. ABCM Encoding

ABCM	Description
00	Match0 mapped to comparator A match: Match1 mapped to comparator B match.
01	Match 0 mapped to comparator A/B inside range: Match1 disabled.
10	Match 0 mapped to comparator A/B outside range: Match1 disabled.



6.4.2.2.2 Outside Range (address < CompA_Addr or address > CompB_Addr)

In the Outside Range comparator mode, comparator pair A and B can be configured for range comparisons. A single match condition on either of the comparators is recognized as valid. An aligned word access which straddles the range boundary is valid only if the aligned address is outside the range.

Outside range mode in combination with tagging can be used to detect if the opcode fetches are from an unexpected range. In forced match mode the outside range match would typically be activated at any interrupt vector fetch or register access. This can be avoided by setting the upper range limit to \$3FFFF or lower range limit to \$00000 respectively.

6.4.3 Match Modes (Forced or Tagged)

Match modes are used as qualifiers for a state sequencer change of state. The Comparator control register TAG bits select the match mode. The modes are described in the following sections.

6.4.3.1 Forced Match

When configured for forced matching, a comparator channel match can immediately initiate a transition to the next state sequencer state whereby the corresponding flags in DBGSR are set. The state control register for the current state determines the next state. Forced matches are typically generated 2-3 bus cycles after the final matching address bus cycle, independent of comparator RWE/RW settings. Furthermore since opcode fetches occur several cycles before the opcode execution a forced match of an opcode address typically precedes a tagged match at the same address.

6.4.3.2 Tagged Match

If a CPU taghit occurs a transition to another state sequencer state is initiated and the corresponding DBGSR flags are set. For a comparator related taghit to occur, the DBG must first attach tags to instructions as they are fetched from memory. When the tagged instruction reaches the execution stage of the instruction queue a taghit is generated by the CPU. This can initiate a state sequencer transition.

6.4.3.3 Immediate Trigger

Independent of comparator matches it is possible to initiate a tracing session and/or breakpoint by writing to the TRIG bit in DBGC1. If configured for begin aligned tracing, this triggers the state sequencer into the Final State, if configured for end alignment, setting the TRIG bit disarms the module, ending the session and issues a forced breakpoint request to the CPU.

It is possible to set both TRIG and ARM simultaneously to generate an immediate trigger, independent of the current state of ARM.

6.4.3.4 Channel Priorities

In case of simultaneous matches the priority is resolved according to Table 6-36. The lower priority is suppressed. It is thus possible to miss a lower priority match if it occurs simultaneously with a higher priority. The priorities described in Table 6-36 dictate that in the case of simultaneous matches, the match pointing to final state has highest priority followed by the lower channel number (0,1,2).



each trace buffer entry. In Detail mode CINF comprises of R/W and size access information (CRW and CSZ respectively).

Single byte data accesses in Detail Mode are always stored to the low byte of the trace buffer (DATAL) and the high byte is cleared. When tracing word accesses, the byte at the lower address is always stored to trace buffer byte1 and the byte at the higher address is stored to byte0.

Mode	Entry Number	4-bits	8-bits	8-bits
		Field 2	Field 1	Field 0
Detail Mode	Entry 1	CINF1,ADRH1	ADRM1	ADRL1
		0	DATAH1	DATAL1
	Entry 2	CINF2,ADRH2	ADRM2	ADRL2
		0	DATAH2	DATAL2
Normal/Loop1 Modes	Entry 1	PCH1	PCM1	PCL1
	Entry 2	PCH2	PCM2	PCL2

Table 6-37. Trace Buffer Organization (Normal,Loop1,Detail modes)

6.4.5.3.1 Information Bit Organization

The format of the bits is dependent upon the active trace mode as described below.

Field2 Bits in Detail Mode

Bit 3	Bit 2	Bit 1	Bit 0
CSZ	CRW	ADDR[17]	ADDR[16]

Figure 6-25. Field2 Bits in Detail Mode

In Detail Mode the CSZ and CRW bits indicate the type of access being made by the CPU.

 Table 6-38.
 Field Descriptions

Bit	Description
3 CSZ	 Access Type Indicator— This bit indicates if the access was a byte or word size when tracing in Detail Mode 0 Word Access 1 Byte Access
2 CRW	 Read Write Indicator — This bit indicates if the corresponding stored address corresponds to a read or write access when tracing in Detail Mode. 0 Write Access 1 Read Access
1 ADDR[17]	Address Bus bit 17— Corresponds to system address bus bit 17.
0 ADDR[16]	Address Bus bit 16— Corresponds to system address bus bit 16.

>bug Module (S12SDBGV2)

If a tracing session is selected by the TSOURCE bit, breakpoints are requested when the tracing session has completed, thus if Begin aligned triggering is selected, the breakpoint is requested only on completion of the subsequent trace (see Table 6-42). If no tracing session is selected, breakpoints are requested immediately.

If the BRK bit is set, then the associated breakpoint is generated immediately independent of tracing trigger alignment.

BRK	TALIGN	DBGBRK	Breakpoint Alignment
0	0	0	Fill Trace Buffer until trigger then disarm (no breakpoints)
0	0	1	Fill Trace Buffer until trigger, then breakpoint request occurs
0	1	0	Start Trace Buffer at trigger (no breakpoints)
0	1	1	Start Trace Buffer at trigger A breakpoint request occurs when Trace Buffer is full
1	x	1	Terminate tracing and generate breakpoint immediately on trigger
1	x	0	Terminate tracing immediately on trigger

6.4.7.2 Breakpoints Generated Via The TRIG Bit

If a TRIG triggers occur, the Final State is entered whereby tracing trigger alignment is defined by the TALIGN bit. If a tracing session is selected by the TSOURCE bit, breakpoints are requested when the tracing session has completed, thus if Begin aligned triggering is selected, the breakpoint is requested only on completion of the subsequent trace (see Table 6-42). If no tracing session is selected, breakpoints are requested immediately. TRIG breakpoints are possible with a single write to DBGC1, setting ARM and TRIG simultaneously.

6.4.7.3 Breakpoint Priorities

If a TRIG trigger occurs after Begin aligned tracing has already started, then the TRIG no longer has an effect. When the associated tracing session is complete, the breakpoint occurs. Similarly if a TRIG is followed by a subsequent comparator channel match, it has no effect, since tracing has already started.

If a forced SWI breakpoint coincides with a BGND in user code with BDM enabled, then the BDM is activated by the BGND and the breakpoint to SWI is suppressed.

6.4.7.3.1 DBG Breakpoint Priorities And BDM Interfacing

Breakpoint operation is dependent on the state of the BDM module. If the BDM module is active, the CPU is executing out of BDM firmware, thus comparator matches and associated breakpoints are disabled. In addition, while executing a BDM TRACE command, tagging into BDM is disabled. If BDM is not active, the breakpoint gives priority to BDM requests over SWI requests if the breakpoint happens to coincide with a SWI instruction in user code. On returning from BDM, the SWI from user code gets executed.



6.5.2 Scenario 1

A trigger is generated if a given sequence of 3 code events is executed.

Figure 6-27. Scenario 1



Scenario 1 is possible with S12SDBGV1 SCR encoding

6.5.3 Scenario 2

A trigger is generated if a given sequence of 2 code events is executed.

Figure 6-28. Scenario 2a



A trigger is generated if a given sequence of 2 code events is executed, whereby the first event is entry into a range (COMPA,COMPB configured for range mode). M1 is disabled in range modes.



A trigger is generated if a given sequence of 2 code events is executed, whereby the second event is entry into a range (COMPA,COMPB configured for range mode)





All 3 scenarios 2a,2b,2c are possible with the S12SDBGV1 SCR encoding





7.3.2.10 Reserved Register CPMUTEST0

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in special mode can alter the S12CPMU's functionality.



Figure 7-13. Reserved Register (CPMUTEST0)

Read: Anytime

Write: Only in special mode

7.3.2.11 Reserved Register CPMUTEST1

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in special mode can alter the S12CPMU's functionality.

0x003E



Figure 7-14. Reserved Register (CPMUTEST1)

Read: Anytime

Write: Only in special mode



The detailed register descriptions follow in the order they appear in the register map.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 CANCTL0	R W	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
0x0001 CANCTL1	R W	CANE	CLKSRC	LOOPB	LISTEN	BORM	WUPM	SLPAK	INITAK
0x0002 CANBTR0	R W	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
0x0003 CANBTR1	R W	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
0x0004 CANRFLG	R W	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
0x0005 CANRIER	R W	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
0x0006 CANTFLG	R W	0	0	0	0	0	TXE2	TXE1	TXE0
0x0007 CANTIER	R W	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
0x0008 CANTARQ	R W	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
0x0009 CANTAAK	R W	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
0x000A CANTBSEL	R W	0	0	0	0	0	TX2	TX1	ТХ0
0x000B CANIDAC	R W	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
0x000C Reserved	R W	0	0	0	0	0	0	0	0
0x000D CANMISC	R W	0	0	0	0	0	0	0	BOHOLD

= Unimplemented or Reserved

Figure 8-3. MSCAN Register Summary





Figure 8-16. MSCAN Reserved Register

 Read: Always reads zero in normal system operation modes Write: Unimplemented in normal system operation modes

NOTE

Writing to this register when in special systm operating modes can alter the MSCAN functionality.

8.3.2.14 MSCAN Miscellaneous Register (CANMISC)

This register provides additional features.



1. Read: Anytime

Write: Anytime; write of '1' clears flag; write of '0' ignored

Table 8-21	. CANMISC	Register	Field	Descriptions
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Field	Description
0	Bus-off State Hold Until User Request — If BORM is set in MSCAN Control Register 1 (CANCTL1), this bit
BOHOLD	indicates whether the module has entered the bus-off state. Clearing this bit requests the recovery from bus-off.
	Refer to Section 8.5.2, "Bus-Off Recovery," for details.
	0 Module is not bus-off or recovery has been requested by user in bus-off state
	1 Module is bus-off and holds this state until user request

8.3.2.15 MSCAN Receive Error Counter (CANRXERR)

This register reflects the status of the MSCAN receive error counter.



FRZ1	FRZ0	Behavior in Freeze Mode
0	1	Reserved
1	0	Finish current conversion, then freeze
1	1	Freeze Immediately

Table 9-11. ATD Behavior in Freeze Mode (Breakpoint)

9.3.2.5 ATD Control Register 4 (ATDCTL4)

Writes to this register will abort current conversion sequence.

Module Base + 0x0004



Read: Anytime

Write: Anytime

Table 9-12. ATDCTL4 Field Descriptions

Field	Description
7–5 SMP[2:0]	Sample Time Select — These three bits select the length of the sample time in units of ATD conversion clock cycles. Note that the ATD conversion clock period is itself a function of the prescaler value (bits PRS4-0). Table 9-13 lists the available sample time lengths.
4–0 PRS[4:0]	ATD Clock Prescaler — These 5 bits are the binary prescaler value PRS. The ATD conversion clock frequency is calculated as follows:
	$f_{ATDCLK} = \frac{f_{BUS}}{2 \times (PRS + 1)}$
	Refer to Device Specification for allowed frequency range of f _{ATDCLK} .

Table 9-13. Sample Time Select

SMP2	SMP1	SMP0	Sample Time in Number of ATD Clock Cycles
0	0	0	4
0	0	1	6
0	1	0	8
0	1	1	10
1	0	0	12
1	0	1	16
1	1	0	20
1	1	1	24





13.3.2.11.1 FCCOB - NVM Command Mode

NVM command mode uses the indexed FCCOB register to provide a command code and its relevant parameters to the Memory Controller. The user first sets up all required FCCOB fields and then initiates the command's execution by writing a 1 to the CCIF bit in the FSTAT register (a 1 written by the user clears the CCIF command completion flag to 0). When the user clears the CCIF bit in the FSTAT register all FCCOB parameter fields are locked and cannot be changed by the user until the command completes (as evidenced by the Memory Controller returning CCIF to 1). Some commands return information to the FCCOB register array.

The generic format for the FCCOB parameter fields in NVM command mode is shown in Table 13-23. The return values are available for reading after the CCIF flag in the FSTAT register has been returned to 1 by the Memory Controller. Writes to the unimplemented parameter fields (CCOBIX = 110 and CCOBIX = 111) are ignored with reads from these fields returning 0x0000.

Table 13-23 shows the generic Flash command format. The high byte of the first word in the CCOB array contains the command code, followed by the parameters for this specific Flash command. For details on the FCCOB settings required by each command, see the Flash command descriptions in Section 13.4.5.

CCOBIX[2:0]	Byte	FCCOB Parameter Fields (NVM Command Mode)			
000	н	FCMD[7:0] defining Flash command			
000	LO	6'h0, Global address [17:16]			
001	н	Global address [15:8]			
001	LO	Global address [7:0]			
010	н	Data 0 [15:8]			
010	LO	Data 0 [7:0]			

Table 13-23. FCCOB - NVM Command Mode (Typical Usage)



Register	Error Bit	Error Condition			
	ACCEPP	Set if CCOBIX[2:0] != 000 at command launch			
	ACCERK	Set if command not available in current mode (see Table 13-27)			
FSTAT	FPVIOL	Set if any area of the P-Flash or D-Flash memory is protected			
-	MGSTAT1	Set if any errors have been encountered during the verify operation			
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation			

Table 13-44. Erase All Blocks Command Error Handling

13.4.5.8 Erase Flash Block Command

The Erase Flash Block operation will erase all addresses in a P-Flash or D-Flash block.

 Table 13-45. Erase Flash Block Command FCCOB Requirements

CCOBIX[2:0]	FCCOB P	arameters	
000	0x09	Global address [17:16] to identify Flash block	
001	Global address [15:0] in Flash block to be erased		

Upon clearing CCIF to launch the Erase Flash Block command, the Memory Controller will erase the selected Flash block and verify that it is erased. The CCIF flag will set after the Erase Flash Block operation has completed.

Table 13-46	. Erase Flash	Block Command	Error Handling
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Register	Error Bit	Error Condition		
		Set if CCOBIX[2:0] != 001 at command launch		
		Set if command not available in current mode (see Table 13-27)		
	ACCERR	Set if an invalid global address [17:16] is supplied		
FSTAT		Set if the supplied P-Flash address is not phrase-aligned or if the D-Flash address is not word-aligned		
	FPVIOL	Set if an area of the selected Flash block is protected		
	MGSTAT1	Set if any errors have been encountered during the verify operation		
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation		

13.4.5.9 Erase P-Flash Sector Command

The Erase P-Flash Sector operation will erase all addresses in a P-Flash sector.



Register	Error Bit	Error Condition				
	ACCEPR	i if CCOBIX[2:0] != 000 at command launch				
	ACCERR	et if command not available in current mode (see Table 13-27)				
FSTAT	FPVIOL	Set if any area of the P-Flash or D-Flash memory is protected				
-	MGSTAT1	Set if any errors have been encountered during the verify operation				
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation				

Table 13-50. Unsecure Flash Command Error Handling

13.4.5.11 Verify Backdoor Access Key Command

The Verify Backdoor Access Key command will only execute if it is enabled by the KEYEN bits in the FSEC register (see Table 13-9). The Verify Backdoor Access Key command releases security if user-supplied keys match those stored in the Flash security bytes of the Flash configuration field (see Table 13-3). The Verify Backdoor Access Key command must not be executed from the Flash block containing the backdoor comparison key to avoid code runaway.

CCOBIX[2:0]	FCCOB Parameters				
000	0x0C Not required				
001	Key 0				
010	Key 1				
011	Key 2				
100	Key 3				

Table 13-51. Verify Backdoor Access Key Command FCCOB Requirements

Upon clearing CCIF to launch the Verify Backdoor Access Key command, the Memory Controller will check the FSEC KEYEN bits to verify that this command is enabled. If not enabled, the Memory Controller sets the ACCERR bit in the FSTAT register and terminates. If the command is enabled, the Memory Controller compares the key provided in FCCOB to the backdoor comparison key in the Flash configuration field with Key 0 compared to 0x3_FF00, etc. If the backdoor keys match, security will be released. If the backdoor keys do not match, security is not released and all future attempts to execute the Verify Backdoor Access Key command are aborted (set ACCERR) until a reset occurs. The CCIF flag is set after the Verify Backdoor Access Key operation has completed.

Table 14-6. TSCR1 Field Descriptions (continued)

Field	Description
4 TFFCA	 Timer Fast Flag Clear All Allows the timer flag clearing to function normally. For TFLG1(0x000E), a read from an input capture or a write to the output compare channel (0x0010–0x001F) causes the corresponding channel flag, CnF, to be cleared. For TFLG2 (0x000F), any access to the TCNT register (0x0004, 0x0005) clears the TOF flag. Any access to the PACNT registers (0x0022, 0x0023) clears the PAOVF and PAIF flags in the PAFLG register (0x0021). This has the advantage of eliminating software overhead in a separate clear sequence. Extra care is required to avoid accidental flag clearing due to unintended accesses.
3 PRNT	 Precision Timer 0 Enables legacy timer. PR0, PR1, and PR2 bits of the TSCR2 register are used for timer counter prescaler selection. 1 Enables precision timer. All bits of the PTPSR register are used for Precision Timer Prescaler Selection, and all bits. This bit is writable only once out of reset.

14.3.2.7 Timer Toggle On Overflow Register 1 (TTOV)

Module Base + 0x0007

	7	6	5	4	3	2	1	0
R W	TOV7	TOV6	TOV5	TOV4	TOV3	TOV2	TOV1	TOV0
Reset	0	0	0	0	0	0	0	0

Figure 14-13. Timer Toggle On Overflow Register 1 (TTOV)

Read: Anytime

Write: Anytime

Table 14-7. TTOV Field Descriptions

Field	Description
7:0 TOV[7:0]	 Toggle On Overflow Bits — TOVx toggles output compare pin on overflow. This feature only takes effect when in output compare mode. When set, it takes precedence over forced output compare but not channel 7 override events. 0 Toggle output compare pin on overflow feature disabled. 1 Toggle output compare pin on overflow feature enabled.