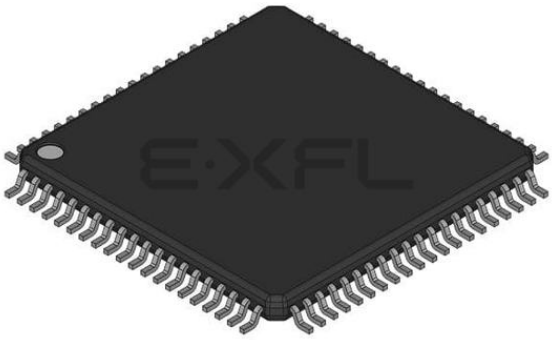

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Audio Processor
Interface	Host Interface, I²C, SAI, SPI
Clock Rate	150MHz
Non-Volatile Memory	ROM (384kB)
On-Chip RAM	264kB
Voltage - I/O	3.30V
Voltage - Core	1.25V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=dspb56371af150

2.5 Peripheral Overview

The DSP56371 is designed to perform a wide variety of fixed-point digital signal processing functions. In addition to the core features previously discussed, the DSP56371 provides the following peripherals:

- As many as 39 dedicate or user-configurable general purpose input/output (GPIO) signals
- Timer/event counter (TEC) module, containing three independent timers
- Memory switch mode in on-chip memory
- Four external interrupt/mode control lines and one external non-maskable interrupt line
- Enhanced serial audio interface (ESAI) with up to four receivers and up to six transmitters, master or slave, using the I^2S, Sony, AC97, network and other programmable protocols
- A second enhanced serial audio interface (ESAI_1) with up to four receivers and up to six transmitters, master or slave, using the I^2S, Sony, AC97, network and other programmable protocols.
- Serial host interface (SHI) using SPI and I^2C protocols, with multi-master capability, 10-word receive FIFO and support for 8-, 16- and 24-bit words
- A Digital audio transmitter (DAX): a serial transmitter capable of supporting the SPDIF, IEC958, CP-340 and AES/EBU digital audio formats

2.5.1 General Purpose Input/Output (GPIO)

The DSP56371 provides 11 dedicated GPIO and 28 programmable signals that can operate either as GPIO pins or peripheral pins (ESAI, ESAI_1, DAX, and TEC). The signals are configured as GPIO after hardware reset. Register programming techniques for all GPIO functionality among these interfaces are very similar and are described in the following sections.

2.5.2 Triple Timer (TEC)

This section describes a peripheral module composed of a common 21-bit prescaler and three independent and identical general purpose 24-bit timer/event counters, each one having its own register set.

Each timer can use internal or external clocking and can interrupt the DSP after a specified number of events (clocks). Two of the three timers can signal an external device after counting internal events. Each timer can also be used to trigger DMA transfers after a specified number of events (clocks) occurred. Two of the three timers connect to the external world through bidirectional pins (TIO0, TIO1). When a TIO pin is configured as input, the timer functions as an external event counter or can measure external pulse width/signal period. When a TIO pin is used as output the timer is functioning as either a timer, a watchdog or a Pulse Width Modulator. When a TIO pin is not used by the timer it can be used as a General Purpose Input/Output Pin. Refer to DSP56371 User's Manual, *Triple Timer Module* section.

2.5.3 Enhanced Serial Audio Interface (ESAI)

The ESAI provides a full-duplex serial port for serial communication with a variety of serial devices including one or more industry-standard codecs, other DSPs, microprocessors and peripherals that

implement the Motorola SPI serial protocol. The ESAI consists of independent transmitter and receiver sections, each with its own clock generator. It is a superset of the DSP56300 family ESSI peripheral and of the DSP56000 family SAI peripheral. For more information on the ESAI, refer to DSP56371 User's Manual, *Enhanced Serial Audio Interface (ESAI)* section.

2.5.4 Enhanced Serial Audio Interface 1 (ESAI_1)

The ESAI_1 is a second ESAI interface. The ESAI_1 is functionally identical to ESAI. For more information on the ESAI_1, refer to DSP56371 User's Manual, *Enhanced Serial Audio Interface (ESAI_1)* section.

2.5.5 Serial Host Interface (SHI)

The SHI is a serial input/output interface providing a path for communication and program/coefficient data transfers between the DSP and an external host processor. The SHI can also communicate with other serial peripheral devices. The SHI can interface directly to either of two well-known and widely used synchronous serial buses: the Motorola serial peripheral interface (SPI) bus and the Philips inter-integrated-circuit control (I^2C) bus. The SHI supports either the SPI or I^2C bus protocol, as required, from a slave or a single-master device. To minimize DSP overhead, the SHI supports single-, double- and triple-byte data transfers. The SHI has a 10-word receive FIFO that permits receiving up to 30 bytes before generating a receive interrupt, reducing the overhead for data reception. For more information on the SHI, refer to DSP56371 User's Manual, *Serial Host Interface* section.

2.5.6 Digital Audio Transmitter (DAX)

The DAX is a serial audio interface module that outputs digital audio data in the AES/EBU, CP-340 and IEC958 formats. For more information on the DAX, refer to DSP56371 User's Manual, *Digital Audio* section.

3 Signal/Connection Descriptions

3.1 Signal Groupings

The input and output signals of the DSP56374 are organized into functional groups, which are listed in Table 1. and illustrated in Figure 2.

The DSP56374 is operated from a 1.25 V and 3.3 V supply; however, some of the inputs can tolerate 5.0 V. A special notice for this feature is added to the signal descriptions of those inputs.

3.3 Ground

Table 3. Grounds

Ground Name	Description
PLLA_GND(1) PLLP_GND(1)	**PLL Ground**—The PLL ground should be provided with an extremely low-impedance path to ground. The user must provide adequate external decoupling capacitors.
PLLD_GND(1)	**PLL Ground**—The PLL ground should be provided with an extremely low-impedance path to ground. The user must provide adequate external decoupling capacitors.
CORE_GND (4)	**Core Ground**—The Core ground should be provided with an extremely low-impedance path to ground. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
IO_GND (5)	**SHI, ESAI, ESAI_1, DAX and Timer I/O Ground**—IO_GND is an isolated ground for the SHI, ESAI, ESAI_1, DAX and Timer I/O. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.

3.4 SCAN

Table 4. SCAN Signals

Signal Name	Type	State During Reset	Signal Description
SCAN	Input	Input	**SCAN**—Manufacturing test pin. This pin should be pulled low. Internal Pull down resistor.

3.5 Clock and PLL

Table 5. Clock and PLL Signals

Signal Name	Type	State during Reset	Signal Description
EXTAL	Input	Input	**External Clock Input**—An external clock source must be connected to EXTAL in order to supply the clock to the internal clock generator and PLL. *This input is 5 V tolerant.*
PINIT/$\overline{\text{NMI}}$	Input	Input	**PLL Initial/Nonmaskable Interrupt**—During assertion of $\overline{\text{RESET}}$, the value of PINIT/$\overline{\text{NMI}}$ is written into the PLL Enable (PEN) bit of the PLL control register, determining whether the PLL is enabled or disabled. After $\overline{\text{RESET}}$ de assertion and during normal instruction processing, the PINIT/$\overline{\text{NMI}}$ Schmitt-trigger input is a negative-edge-triggered nonmaskable interrupt (NMI) request internally synchronized to internal system clock. Internal Pull up resistor. This input is 5 V tolerant.

3.6 Interrupt and Mode Control

The interrupt and mode control signals select the chip's operating mode as it comes out of hardware reset. After RESET is deasserted, these inputs are hardware interrupt request lines.

Table 6. Interrupt and Mode Control

Signal Name	Type	State During Reset	Signal Description
MODA/IRQA	Input	Input	**Mode Select A/External Interrupt Request A—**MODA/IRQA is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODA/IRQA selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC and MODD select one of 16 initial chip operating modes, latched into the OMR when the RESET signal is deasserted. If the processor is in the stop standby state and the MODA/IRQA pin is pulled to GND, the processor will exit the stop state. Internal Pull up resistor. This input is 5 V tolerant.

Table 9. Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
SCKR_1	Input or output	GPIO disconnected	**Receiver Serial Clock_1**—SCKR_1 provides the receiver serial bit clock for the ESAI_1. The SCKR_1 operates as a clock input or output used by all the enabled receivers in the asynchronous mode (SYN=0), or as serial flag 0 pin in the synchronous mode (SYN=1). When this pin is configured as serial flag pin, its direction is determined by the RCKD bit in the RCCR_1 register. When configured as the output flag OF0, this pin will reflect the value of the OF0 bit in the SAICR_1 register, and the data in the OF0 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF0, the data value at the pin will be stored in the IF0 bit in the SAISR_1 register, synchronized by the frame sync in normal mode or the slot in network mode.
PE0	Input, output, or disconnected		**Port E0**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SCKT_1	Input or output	GPIO disconnected	**Transmitter Serial Clock_1**—This signal provides the serial bit rate clock for the ESAI_1. SCKT_1 is a clock input or output used by all enabled transmitters and receivers in synchronous mode, or by all enabled transmitters in asynchronous mode.
PE3	Input, output, or disconnected		**Port E3**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO5_1	Output	GPIO disconnected	**Serial Data Output 5_1**—When programmed as a transmitter, SDO5_1 is used to transmit data from the TX5 serial transmit shift register.
SDI0_1	Input		**Serial Data Input 0_1**—When programmed as a receiver, SDI0_1 is used to receive serial data into the RX0 serial receive shift register.
PE6	Input, output, or disconnected		**Port E6**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 9. Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
SDO4_1	Output	GPIO disconnected	**Serial Data Output 4_1**—When programmed as a transmitter, SDO4_1 is used to transmit data from the TX4 serial transmit shift register.
SDI1_1	Input		**Serial Data Input 1_1**—When programmed as a receiver, SDI1_1 is used to receive serial data into the RX1 serial receive shift register.
PE7	Input, output, or disconnected		**Port E7**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO3_1	Output	GPIO disconnected	**Serial Data Output 3**—When programmed as a transmitter, SDO3_1 is used to transmit data from the TX3 serial transmit shift register.
SDI2_1	Input		**Serial Data Input 2**—When programmed as a receiver, SDI2_1 is used to receive serial data into the RX2 serial receive shift register.
PE8	Input, output, or disconnected		**Port E8**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO2_1	Output	GPIO disconnected	**Serial Data Output 2**—When programmed as a transmitter, SDO2_1 is used to transmit data from the TX2 serial transmit shift register.
SDI3_1	Input		**Serial Data Input 3**—When programmed as a receiver, SDI3_1 is used to receive serial data into the RX3 serial receive shift register.
PE9	Input, output, or disconnected		**Port E9**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 9. Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
SDO1_1 PE10	Output Input, output, or disconnected	GPIO disconnected	**Serial Data Output 1**—SDO1_1 is used to transmit data from the TX1 serial transmit shift register. **Port E10**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO0_1 PE11	Output Input, output, or disconnected	GPIO disconnected	**Serial Data Output 0**—SDO0_1 is used to transmit data from the TX0 serial transmit shift register. **Port E11**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 11. Dedicated GPIO Signals (continued)

Signal Name	Type	State During Reset	Signal Description
PF7	Input, output, or disconnected	GPIO disconnected	**Port F7**— this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
PF8	Input, output, or disconnected	GPIO disconnected	**Port F8**— this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
PF9	Input, output, or disconnected	GPIO disconnected	**Port F9**— this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
PF10	Input, output, or disconnected	GPIO disconnected	**Port F10**— this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

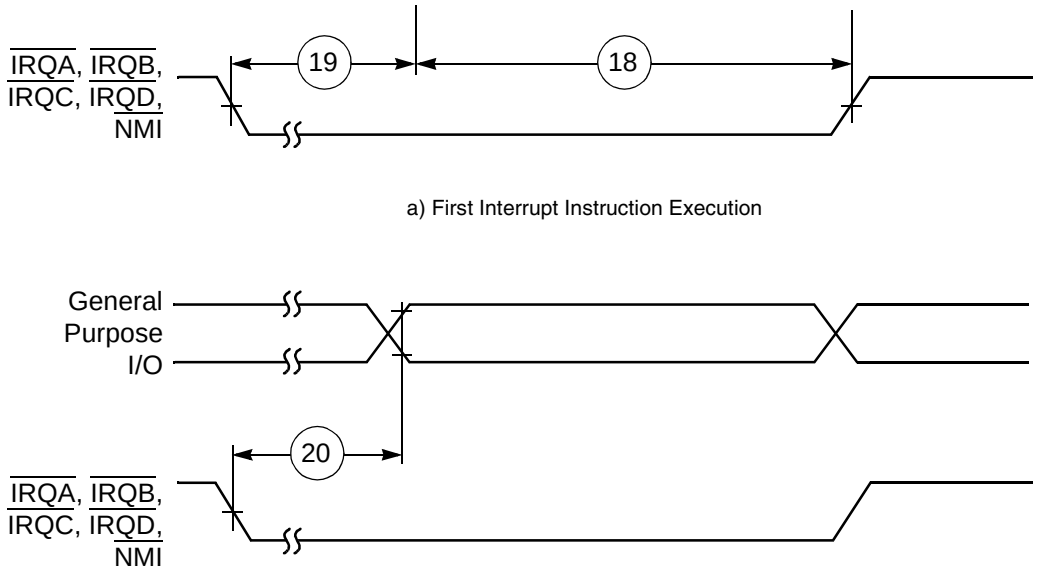


Figure 8. External Fast Interrupt Timing

12 Serial Host Interface SPI Protocol Timing

Table 20. Serial Host Interface SPI Protocol Timing

No.	Characteristics[1,3,4]	Mode	Expressions	Min	Max	Unit
23	Minimum serial clock cycle = t_{SPICC}(min)	Master	10.0 x T_C + 9	64.0	—	ns
24	Serial clock high period	Master	—	29.5	—	ns
		Slave	2.0 x T_C + 19.6	27.5	—	ns
25	Serial clock low period	Master	—	29.5	—	ns
		Slave	2.0 x T_C + 19.6	27.5	—	ns
26	Serial clock rise/fall time	Master	—	—	10	ns
		Slave	—	—	10	ns
27	$\overline{SS}$ assertion to first SCK edge CPHA = 0	Slave	2.0 x T_C + 12.6	34.4	—	ns
	CPHA = 1	Slave	—	10.0	—	ns
28	Last SCK edge to $\overline{SS}$ not asserted	Slave	—	12.0	—	ns
29	Data input valid to SCK edge (data input set-up time)	Master/Slave	—	0	—	ns
30	SCK last sampling edge to data input not valid	Master/Slave	3.0 x T_C	22.4	—	ns
31	$\overline{SS}$ assertion to data out active	Slave	—	5	—	ns
32	$\overline{SS}$ deassertion to data high impedance[2]	Slave	—	—	9	ns
33	SCK edge to data out valid (data out delay time)	Master/Slave	3.0 x T_C + 26.1	50.0	100	ns

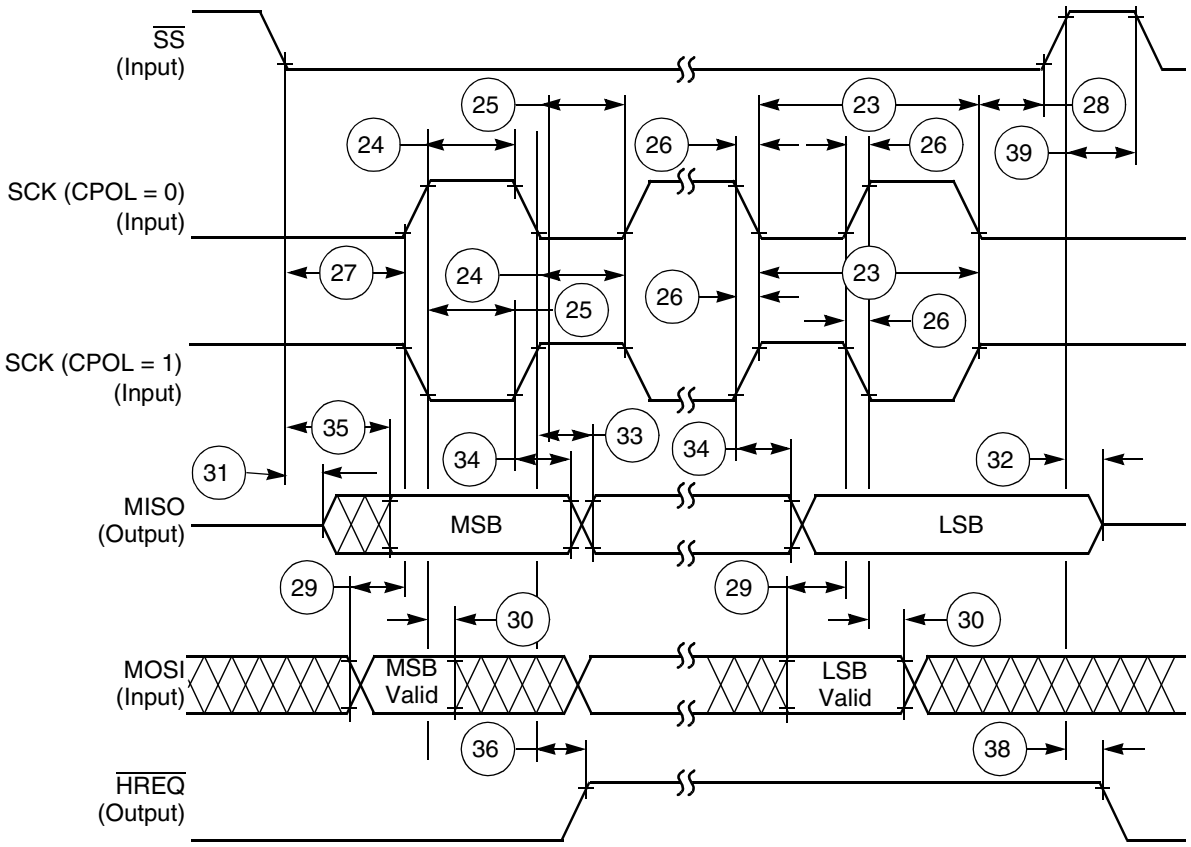


Figure 11. SPI Slave Timing (CPHA = 0)

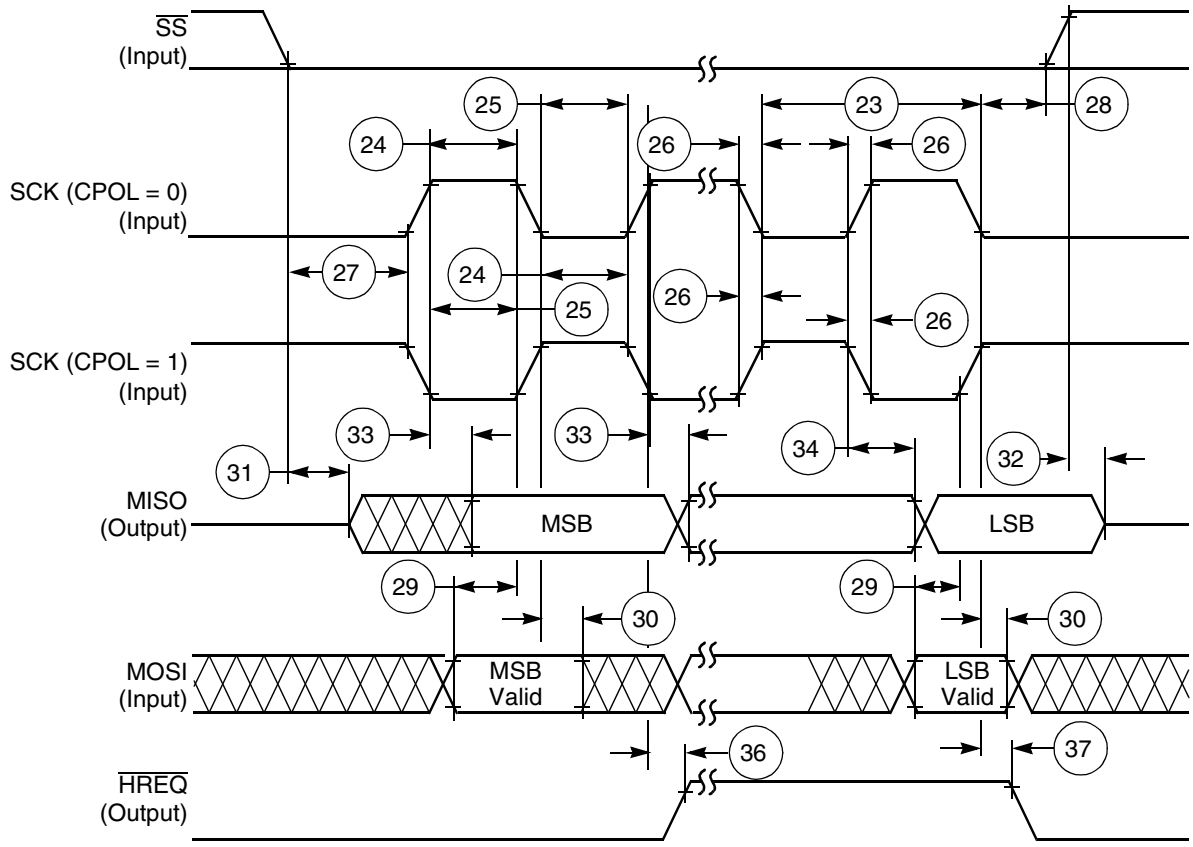


Figure 12. SPI Slave Timing (CPHA = 1)

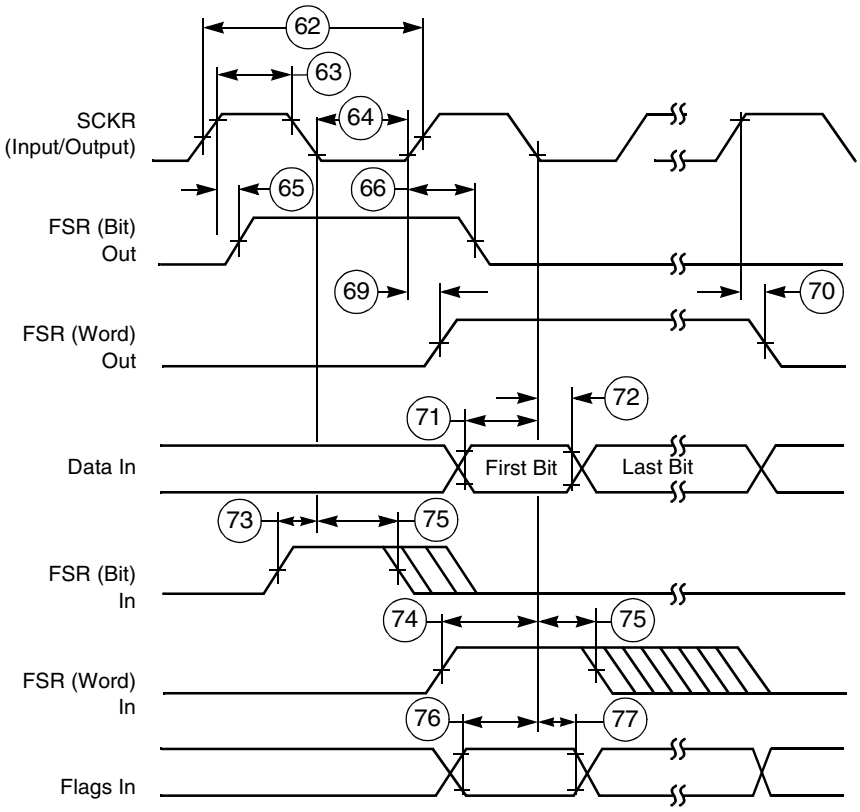
13 Serial Host Interface (SHI) I2C Protocol Timing

Table 21. SHI I2C Protocol Timing

Standard I2C*							
No.	Characteristics[1]	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
44	SCL clock frequency	F_{SCL}	—	100	—	400	kHz
44	SCL clock cycle	T_{SCL}	10	—	2.5	—	µs
45	Bus free time	T_{BUF}	4.7	—	1.3	—	µs
46	Start condition set-up time	T_{SUSTA}	4.7	—	0.6	—	µs
47	Start condition hold time	$T_{HD;STA}$	4.0	—	0.6	—	µs
48	SCL low period	T_{LOW}	4.7	—	1.3	—	µs
49	SCL high period	T_{HIGH}	4.0	—	1.3	—	µs
50	SCL and SDA rise time	T_R	—	5	—	5	ns
51	SCL and SDA fall time	T_F	—	5	—	5	ns

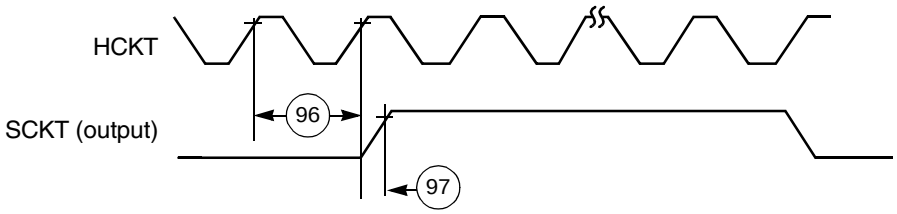
Table 22. Enhanced Serial Audio Interface Timing (continued)

No.	Characteristics[1, 2, 3]	Symbol	Expression	Min	Max	Condition[4]	Unit
67	SCKR edge to FSR out (wr) high[6]	—	—	— —	39.0 24.0	x ck i ck a	ns
68	SCKR edge to FSR out (wr) low[6]	—	—	— —	39.0 24.0	x ck i ck a	ns
69	SCKR edge to FSR out (wl) high	—	—	— —	36.0 21.0	x ck i ck a	ns
70	SCKR edge to FSR out (wl) low	—	—	— —	37.0 22.0	x ck i ck a	ns
71	Data in setup time before SCKR (SCK in synchronous mode) edge	—	—	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after SCKR edge	—	—	5.0 3.0	— —	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR edge [6]	—	—	2.0 23.0	— —	x ck i ck a	ns
74	FSR input (wl) high before SCKR edge	—	—	2.0 23.0	— —	x ck i ck a	ns
75	FSR input hold time after SCKR edge	—	—	3.0 0.0	— —	x ck i ck a	ns
76	Flags input setup before SCKR edge	—	—	0.0 19.0	— —	x ck i ck s	ns
77	Flags input hold time after SCKR edge	—	—	6.0 0.0	— —	x ck i ck s	ns
78	SCKT edge to FST out (bl) high	—	—	— —	29.0 15.0	x ck i ck	ns
79	SCKT edge to FST out (bl) low	—	—	— —	31.0 17.0	x ck i ck	ns
80	SCKT edge to FST out (wr) high[6]	—	—	— —	31.0 17.0	x ck i ck	ns
81	SCKT edge to FST out (wr) low[6]	—	—	— —	33.0 19.0	x ck i ck	ns
82	SCKT edge to FST out (wl) high	—	—	— —	30.0 16.0	x ck i ck	ns
83	SCKT edge to FST out (wl) low	—	—	— —	31.0 17.0	x ck i ck	ns
84	SCKT edge to data out enable from high impedance	—	—	— —	31.0 17.0	x ck i ck	ns
85	SCKT edge to transmitter #0 drive enable assertion	—	—	— —	34.0 20.0	x ck i ck	ns
86	SCKT edge to data out valid	—	—	— —	26.5 21.0	x ck i ck	ns
87	SCKT edge to data out high impedance[7]	—	—	— —	31.0 16.0	x ck i ck	ns



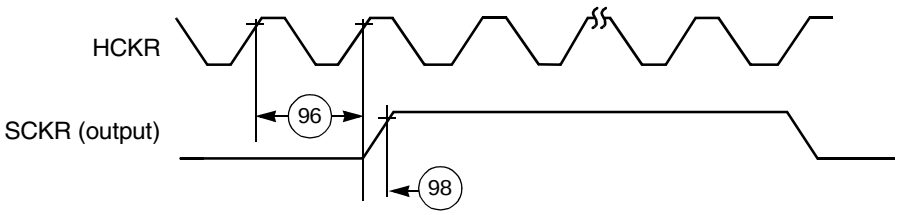
Note: Figure 15 is drawn assuming positive polarity bit clock (RCKP=0) and positive frame sync polarity (RFSP=0).

Figure 15. ESAI Receiver Timing



Note: Figure 16 is drawn assuming positive polarity high frequency clock (THCKP=0) and positive bit clock polarity (TCKP=0).

Figure 16. ESAI HCKT Timing



Note: Figure 17 is drawn assuming positive polarity high frequency clock (RHCKP=0) and positive bit clock polarity (RCKP=0).

Figure 17. ESAI HCKR Timing

15 Digital Audio Transmitter Timing

Table 23. Digital Audio Transmitter Timing

No.	Characteristic	Expression	181 MHz		Unit
			Min	Max	
99	ACI frequency (see note)	1 / (2 x T_C)	—	90	MHz
100	ACI period	$2 \times T_C$	11.1	—	ns
101	ACI high duration	$0.5 \times T_C$	2.8	—	ns
102	ACI low duration	$0.5 \times T_C$	2.8	—	ns
103	ACI rising edge to ADO valid	$1.5 \times T_C$	—	8.3	ns

Note:

1. In order to assure proper operation of the DAX, the ACI frequency should be less than 1/2 of theDSP56371 internal clock frequency. For example, if the DSP56371 is running at 181 MHz internally, the ACI frequency should be less than 90MHz.

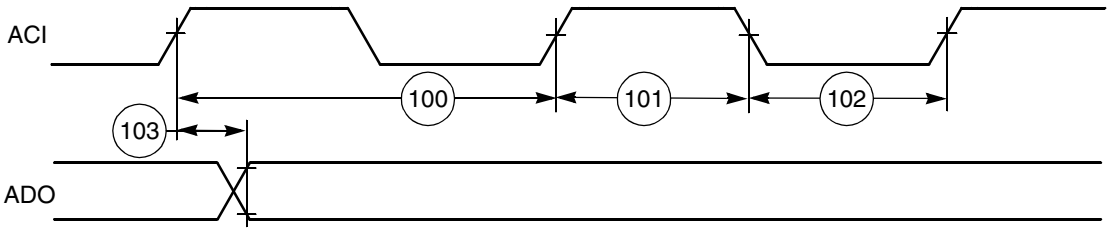


Figure 18. Digital Audio Transmitter Timing

16 Timer Timing

Table 24. Timer Timing

No.	Characteristics	Expression	181 MHz		Unit
			Min	Max	
104	TIO Low	$2 \times T_C + 2.0$	13	—	ns
105	TIO High	$2 \times T_C + 2.0$	13	—	ns

Note:
1. V_{CORE_VDD} = 1.25 V ± 0.05 V; T_J = –40°C to 115°C for 150 MHz; T_J = 0°C to 100°C for 181 MHz; C_L = 50 pF

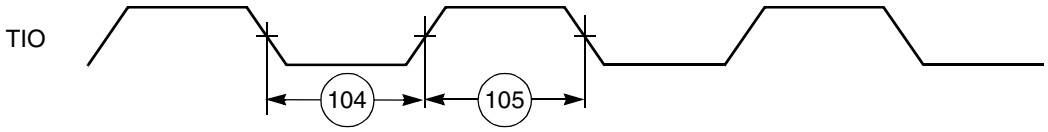


Figure 19. TIO Timer Event Input Restrictions

17 GPIO Timing

Table 25. GPIO Timing

No.	Characteristics[1]	Expression	Min	Max	Unit
106	FOSC edge to GPIO out valid (GPIO out delay time)		—	7	ns
107	FOSC edge to GPIO out not valid (GPIO out hold time)		—	7	ns
108	FOSC In valid to EXTAL edge (GPIO in set-up time)		2	—	ns
109	FOSC edge to GPIO in not valid (GPIO in hold time)		0	—	ns
110	Minimum GPIO pulse high width (except Port F)	T_C + 13	19	—	ns
111	Minimum GPIO pulse low width (except Port F)	T_C + 13	19		ns
112	Minimum GPIO pulse low width (Port F)	6 x T_C	33.3		ns
113	Minimum GPIO pulse high width (Port F)	6 x T_C	33.3		ns
114	GPIO out rise time	—	—	13	ns
115	GPIO out fall time	—	—	13	ns

Note:
1. V_{CORE_VDD} = 1.25 V ± 0.05 V; T_J = –40°C to 115°C for 150 MHz; T_J = 0°C to 100°C for 181 MHz; C_L = 50 pF
2. PLL Disabled, EXTAL driven by a square wave

Figure 20. GPIO Timing

18 JTAG Timing

Table 26. JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
116	TCK frequency of operation (1/($T_C \times 6$); maximum 22 MHz)	0.0	22.0	MHz
117	TCK cycle time	45.0	—	ns
118	TCK clock pulse width	20.0	—	ns
119	TCK rise and fall times	0.0	10.0	ns
120	TCK low to output data valid	0.0	40.0	ns
121	TCK low to output high impedance	0.0	40.0	ns
122	TMS, TDI data setup time	5.0	—	ns
123	TMS, TDI data hold time	25.0	—	ns
124	TCK low to TDO data valid	0.0	44.0	ns
125	TCK low to TDO high impedance	0.0	44.0	ns

Note:
V_{CORE_VDD} = 1.25 V ± 0.05 V; T_J = –40°C to 115°C for 150 MHz; T_J = 0°C to 100°C for 181 MHz; C_L = 50 pF
All timings apply to OnCE module data transfers because it uses the JTAG port as an interface.

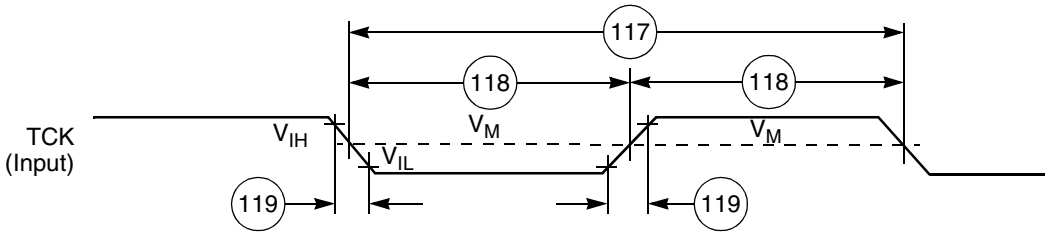


Figure 21. Test Clock Input Timing Diagram

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23237W
		PAGE: 917A
	DO NOT SCALE THIS DRAWING	REV: E

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION : MILIMETER.
3. DATUM PLANE H IS LOCATED AT THE BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUM E, F AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	CASE NUMBER: 917A–03	
	STANDARD: FREESCALE	
	PACKAGE CODE: 8258	SHEET: 3 OF 4

22 Power Consumption Benchmark

The following benchmark program permits evaluation of DSP power usage in a test situation.

```
;*********************************;*******************************

;* ;* CHECKS Typical Power Consumption

;*************************************************************************

ORG P:$000800
move #$000000,r1
move #$000000,r0
do #1024,ldmem
move r1,p:(r0)
move r1,y:(r0)+
ldmem nop



move #0,b1

;jmp $FF2AE0

;org P:$FF2AE0
move b1,y:>$100
move #$FF,B
move #>$AF080,X0
move #>$FF2AD6,r0
move #$0,r1

dor #6,loop1

move p:(r0)+,x1
move x0,p:(r1)+
move x1,p:(r1)+
nop
loop1

move #$0,vba
move #$0,sp
move #$0,sc
reset
move #$FFFFFF,m0
move m0,m1
move m0,m2
move m0,m3
move m0,m4
move m0,m5
move m0,m6
move m0,m7
move #>$102,ep
move #>$18,sz
move #>$110000,omr
```

```
move #$300,sr
movep #>$F02000,X:$FFFFFF
movep #$187,X:$FFFFFE

;then sets up BCR and AAR registers

;then sets up PORTB and HDI08 PORT

andi #$FC,mr

;start running ROM intialisation stage
;jsr $FF1C7E

; Set green HLX zone table
jsr $FF1D64

; Run GPIONil function
jsr $FF2F82

; Initialise Green HLX
jsr $FF1FA1

; Disable DAX
move #>$15F,x1
move x1,P:$FF0D7F

; Run Green HLX
jmp $FF1FDB


nop
nop
nop
nop
nop
nop
dor forever,endprog
nop
nop
endprog nop
```

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