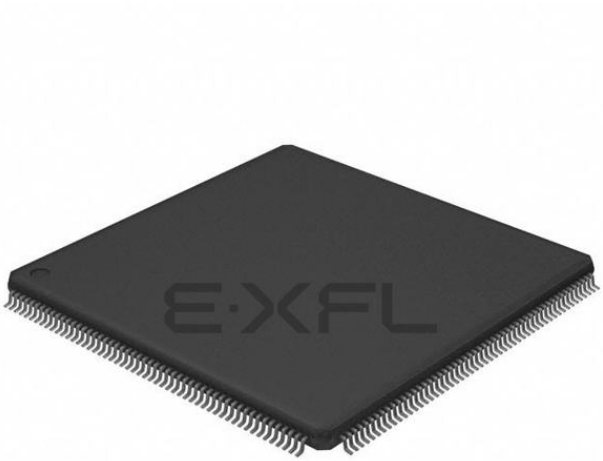

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, MMC/SD, QEI, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	142
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	154K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 16x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4367jbd208e

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
P2_5	K14	D10	131	[3]	N; PU	I/O	**SGPIO14 —** General purpose digital input/output pin.
						I	**CTIN_2 —** SCT input 2. Capture input 2 of timer 0.
						I	**USB1_VBUS —** Monitors the presence of USB1 bus power. **Note:** This signal must be HIGH for USB reset to occur.
						I	**ADCTRIG1 —** ADC trigger input 1.
						I/O	**GPIO5[5] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						O	**T3_MAT2 —** Match output 2 of timer 3.
						O	**USB0_IND0 —** USB0 port indicator LED control output 0.
P2_6	K16	G9	137	[2]	N; PU	I/O	**SGPIO7 —** General purpose digital input/output pin.
						I/O	**U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0.
						I/O	**EMC_A10 —** External memory address line 10.
						O	**USB0_IND0 —** USB0 port indicator LED control output 0.
						I/O	**GPIO5[6] —** General purpose digital input/output pin.
						I	**CTIN_7 —** SCT input 7.
						I	**T3_CAP3 —** Capture input 3 of timer 3.
						O	**$\overline{\text{EMC\_BLS1}}$ —** LOW active Byte Lane select signal 1.
P2_7	H14	C10	138	[2]	N; PU	I/O	**GPIO0[7] —** General purpose digital input/output pin. If this pin is pulled LOW at reset, the part enters ISP mode or boots from an external source (see Table 4 and Table 5).
						O	**CTOUT_1 —** SCT output 1. Match output 3 of timer 3.
						I/O	**U3_UCLK —** Serial clock input/output for USART3 in synchronous mode.
						I/O	**EMC_A9 —** External memory address line 9.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**T3_MAT3 —** Match output 3 of timer 3.
						-	**R —** Function reserved.
P2_8	J16	C6	140	[2]	N; PU	I/O	**SGPIO15 —** General purpose digital input/output pin. Boot pin (see Table 5).
						O	**CTOUT_0 —** SCT output 0. Match output 0 of timer 0.
						I/O	**U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3.
						I/O	**EMC_A8 —** External memory address line 8.
						I/O	**GPIO5[7] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
P6_11	H12	C9	143	[2]	N; PU	I/O	**GPIO3[7] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**EMC_CKEOUT0 —** SDRAM clock enable 0.
						-	**R —** Function reserved.
						O	**T2_MAT3 —** Match output 3 of timer 2.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P6_12	G15	-	145	[2]	N; PU	I/O	**GPIO2[8] —** General purpose digital input/output pin.
						O	**CTOUT_7 —** SCT output 7. Match output 3 of timer 1.
						-	**R —** Function reserved.
						O	**EMC_DQMOUT0 —** Data mask 0 used with SDRAM and static devices.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P7_0	B16	-	158	[2]	N; PU	I/O	**GPIO3[8] —** General purpose digital input/output pin.
						O	**CTOUT_14 —** SCT output 14. Match output 2 of timer 3.
						-	**R —** Function reserved.
						O	**LCD_LE —** Line end signal.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SGPIO4 —** General purpose digital input/output pin.
P7_1	C14	-	162	[2]	N; PU	I/O	**GPIO3[9] —** General purpose digital input/output pin.
						O	**CTOUT_15 —** SCT output 15. Match output 3 of timer 3.
						I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
						O	**LCD_VD19 —** LCD data.
						O	**LCD_VD7 —** LCD data.
						-	**R —** Function reserved.
						O	**U2_TXD —** Transmitter output for USART2.
						I/O	**SGPIO5 —** General purpose digital input/output pin.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
P7_6	C7	-	194	[2]	N; PU	I/O	**GPIO3[14] —** General purpose digital input/output pin.
						O	**CTOUT_11 —** SCT output 1. Match output 3 of timer 2.
						-	**R —** Function reserved.
						O	**LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
						-	**R —** Function reserved.
						O	**TRACEDATA[2] —** Trace data, bit 2.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P7_7	B6	-	201	[5]	N; PU	I/O	**GPIO3[15] —** General purpose digital input/output pin.
						O	**CTOUT_8 —** SCT output 8. Match output 0 of timer 2.
						-	**R —** Function reserved.
						O	**LCD_PWR —** LCD panel power enable.
						-	**R —** Function reserved.
						O	**TRACEDATA[3] —** Trace data, bit 3.
						O	**ENET_MDC —** Ethernet MIIM clock.
						I/O	**SGPIO7 —** General purpose digital input/output pin.
						AI	**ADC1_6 —** ADC1 and ADC0, input channel 6. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P8_0	E5	-	2	[3]	N; PU	I/O	**GPIO4[0] —** General purpose digital input/output pin.
						I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
						-	**R —** Function reserved.
						I	**MCI2 —** Motor control PWM channel 2, input.
						I/O	**SGPIO8 —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**T0_MAT0 —** Match output 0 of timer 0.
P8_1	H5	-	34	[3]	N; PU	I/O	**GPIO4[1] —** General purpose digital input/output pin.
						O	**USB0_IND1 —** USB0 port indicator LED control output 1.
						-	**R —** Function reserved.
						I	**MCI1 —** Motor control PWM channel 1, input.
						I/O	**SGPIO9 —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**T0_MAT1 —** Match output 1 of timer 0.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
P8_2	K4	-	36	[3]	N; PU	I/O	**GPIO4[2] —** General purpose digital input/output pin.
						O	**USB0_IND0 —** USB0 port indicator LED control output 0.
						-	**R —** Function reserved.
						I	**MCI0 —** Motor control PWM channel 0, input.
						I/O	**SGPIO10 —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**T0_MAT2 —** Match output 2 of timer 0.
P8_3	J3	-	37	[2]	N; PU	I/O	**GPIO4[3] —** General purpose digital input/output pin.
						I/O	**USB1_ULPI_D2 —** ULPI link bidirectional data line 2.
						-	**R —** Function reserved.
						O	**LCD_VD12 —** LCD data.
						O	**LCD_VD19 —** LCD data.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**T0_MAT3 —** Match output 3 of timer 0.
P8_4	J2	-	39	[2]	N; PU	I/O	**GPIO4[4] —** General purpose digital input/output pin.
						I/O	**USB1_ULPI_D1 —** ULPI link bidirectional data line 1.
						-	**R —** Function reserved.
						O	**LCD_VD7 —** LCD data.
						O	**LCD_VD16 —** LCD data.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I	**T0_CAP0 —** Capture input 0 of timer 0.
P8_5	J1	-	40	[2]	N; PU	I/O	**GPIO4[5] —** General purpose digital input/output pin.
						I/O	**USB1_ULPI_D0 —** ULPI link bidirectional data line 0.
						-	**R —** Function reserved.
						O	**LCD_VD6 —** LCD data.
						O	**LCD_VD8 —** LCD data.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I	**T0_CAP1 —** Capture input 1 of timer 0.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
P9_5	M9	-	98	[2]	N; PU	-	**R —** Function reserved.
						O	**MCOA1 —** Motor control PWM channel 1, output A.
						O	**USB1_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active high). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
						-	**R —** Function reserved.
						I/O	**GPIO5[18] —** General purpose digital input/output pin.
						O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
						I/O	**SGPIO3 —** General purpose digital input/output pin.
						O	**U0_TXD —** Transmitter output for USART0.
P9_6	L11	-	103	[2]	N; PU	I/O	**GPIO4[11] —** General purpose digital input/output pin.
						O	**MCOB1 —** Motor control PWM channel 1, output B.
						I	**USB1_PWR_FAULT —** USB1 Port power fault signal indicating over-current condition; this signal monitors over-current on the USB1 bus (external circuitry required to detect over-current condition).
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I	**ENET_COL —** Ethernet Collision detect (MII interface).
						I/O	**SGPIO8 —** General purpose digital input/output pin.
						I	**U0_RXD —** Receiver input for USART0.
PA_0	L12	-	126	[2]	N; PU	-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**I2S1_RX_MCLK —** I2S1 receive master clock.
						O	**CGU_OUT1 —** CGU spare clock output 1.
						-	**R —** Function reserved.
PA_1	J14	-	134	[3]	N; PU	I/O	**GPIO4[8] —** General purpose digital input/output pin.
						I	**QEI_IDX —** Quadrature Encoder Interface INDEX input.
						-	**R —** Function reserved.
						O	**U2_TXD —** Transmitter output for USART2.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
PE_2	M14	-	115	[2]	N; PU	I	**ADCTRIG0 —** ADC trigger input 0.
						I	**CAN0_RD —** CAN receiver input.
						-	**R —** Function reserved.
						I/O	**EMC_A20 —** External memory address line 20.
						I/O	**GPIO7[2] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PE_3	K12	-	118	[2]	N; PU	-	**R —** Function reserved.
						O	**CAN0_TD —** CAN transmitter output.
						I	**ADCTRIG1 —** ADC trigger input 1.
						I/O	**EMC_A21 —** External memory address line 21.
						I/O	**GPIO7[3] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PE_4	K13	-	120	[2]	N; PU	-	**R —** Function reserved.
						I	**NMI —** External interrupt input to NMI.
						-	**R —** Function reserved.
						I/O	**EMC_A22 —** External memory address line 22.
						I/O	**GPIO7[4] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PE_5	N16	-	122	[2]	N; PU	-	**R —** Function reserved.
						O	**CTOUT_3 —** SCT output 3. Match output 3 of timer 0.
						O	**U1_RTS —** Request to Send output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
						I/O	**EMC_D24 —** External memory data line 24.
						I/O	**GPIO7[5] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
PF_9	D6	-	203	[5]	N; PU	-	**R —** Function reserved.
						I/O	**U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0.
						O	**CTOUT_1 —** SCT output 1. Match output 3 of timer 3.
						-	**R —** Function reserved.
						I/O	**GPIO7[23] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						I/O	**SGPIO3 —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						AI	**ADC1_2 —** ADC1 and ADC0, input channel 2. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PF_10	A3	-	205	[5]	N; PU	-	**R —** Function reserved.
						O	**U0_TXD —** Transmitter output for USART0.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**GPIO7[24] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						I	**SD_WP —** SD/MMC card write protect input.
						-	**R —** Function reserved.
						AI	**ADC0_5 —** ADC0 and ADC1, input channel 5. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PF_11	A2	-	207	[5]	N; PU	-	**R —** Function reserved.
						I	**U0_RXD —** Receiver input for USART0.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**GPIO7[25] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						O	**SD_VOLT2 —** SD/MMC bus voltage select output 2.
						-	**R —** Function reserved.
						AI	**ADC1_5 —** ADC1 and ADC0, input channel 5. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 5. Boot mode when OPT BOOT_SRC bits are zero

Boot mode	Pins				Description
	P2_9	P2_8	P1_2	P1_1	
EMC 32-bit	LOW	HIGH	LOW	LOW	Boot from external static memory (such as NOR flash) using CS0 and a 32-bit data bus.
USB0	LOW	HIGH	LOW	HIGH	Boot from USB0
USB1	LOW	HIGH	HIGH	LOW	Boot from USB1.
SPI (SSP)	LOW	HIGH	HIGH	HIGH	Boot from SPI flash connected to the SSP0 interface on P3_3 (function SSP0_SCK), P3_6 (function SSP0_SSEL), P3_7 (function SSP0_MISO), and P3_8 (function SSP0_MOSI)[1].
USART3	HIGH	LOW	LOW	LOW	Enter ISP mode using USART3 pins P2_3 and P2_4.

[1] The boot loader programs the appropriate pin function at reset to boot using either SSP0 or SPIFI.
Remark: Pin functions for SPIFI and SSP0 boot are different.

7.14 Memory mapping

The memory map shown in Figure 6 and Figure 7 is global to both the Cortex-M4 and the Cortex-M0 processors and all SRAM, flash, and EEPROM memory is shared between both processors. Each processor uses its own ARM private bus memory map for the NVIC and other system functions.

- Supports both full-duplex and half-duplex operation
  - Supports CSMA/CD Protocol for half-duplex operation.
  - Supports IEEE 802.3x flow control for full-duplex operation.
  - Optional forwarding of received pause control frames to the user application in full-duplex operation.
  - Back-pressure support for half-duplex operation.
  - Automatic transmission of zero-quanta pause frame on deassertion of flow control input in full-duplex operation.
- Supports IEEE1588 time stamping and IEEE 1588 advanced time stamping (IEEE 1588-2008 v2).

7.19 Digital serial peripherals

7.19.1 UART1

Remark: The LPC436x contain one UART with standard transmit and receive data lines.

UART1 also provides a full modem control handshake interface and support for RS-485/9-bit mode allowing both software address detection and automatic address detection using 9-bit mode.

UART1 includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.19.1.1 Features

- Maximum UART data bit rate of 8 MBit/s.
- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Equipped with standard modem interface signals. This module also provides full support for hardware flow control.
- Support for RS-485/9-bit/EIA-485 mode (UART1).
- DMA support.

7.19.2 USART0/2/3

Remark: The LPC436x contain three USARTs. In addition to standard transmit and receive data lines, the USARTs support a synchronous mode.

The USARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.19.2.1 Features

- Maximum UART data bit rate of 8 MBit/s.

8. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)	on pin VDDREG		–0.5	3.6	V
$V_{DD(IO)}$	input/output supply voltage	on pin VDDIO		–0.5	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	on pin VDDA		–0.5	3.6	V
V_{BAT}	battery supply voltage	on pin VBAT		–0.5	3.6	V
$V_{prog(pf)}$	polyfuse programming voltage	on pin VPP		–0.5	3.6	V
V_I	input voltage	when $V_{DD(IO)} \geq 2.4$ V 5 V tolerant digital I/O pins	[2]	–0.5	5.5	V
		ADC/DAC pins and digital I/O pins configured for an analog function		–0.5	$V_{DDA(3V3)}$	V
		USB0 pins USB0_DP; USB0_DM;USB0_VBUS		–0.3	5.25	V
		USB0 pins USB0_ID; USB0_RREF		–0.3	3.6	V
		USB1 pins USB1_DP and USB1_DM		–0.3	5.25	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(IO)}) < V_I < (1.5V_{DD(IO)})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[3]	–65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[4]	-	2000	V

[1] The following applies to the limiting values:

a) Absolute maximum ratings state the extreme limits that the product can withstand without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device. Conditions for functional operation of the part are shown in Table 11 "Static characteristics".

b) This product includes circuitry designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

c) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] Dependent on package type.

[4] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

10. Static characteristics

Table 11. Static characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply pins							
$V_{DD(IO)}$	input/output supply voltage		[17]	2.4	-	3.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)		[2]	2.4	-	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	on pin VDDA		2.4	-	3.6	V
		on pins USB0_VDDA3V3_ DRIVER and USB0_VDDA3V3		3.0	3.3	3.6	V
V_{BAT}	battery supply voltage		[2]	2.4	-	3.6	V
$V_{prog(pf)}$	polyfuse programming voltage	on pin VPP (for OTP)	[3]	2.7	-	3.6	V
$I_{prog(pf)}$	polyfuse programming current	on pin VPP; OTP programming time ≤ 1.6 ms		-	-	30	mA
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	Active mode; ARM Cortex-M0 core in reset; code `while(1){}` executed from RAM; all peripherals disabled; PLL1 enabled					
		CCLK = 12 MHz	[4]	-	10	-	mA
		CCLK = 60 MHz	[4]		28	-	mA
		CCLK = 120 MHz	[4]	-	51	-	mA
		CCLK = 180 MHz	[4]	-	74	-	mA
		CCLK = 204 MHz	[4]	-	83	-	mA
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	after WFE/WFI instruction executed from RAM; all peripherals disabled; ARM Cortex-M0 core in reset					
		sleep mode	[4][5]	-	8.8	-	mA
		deep-sleep mode	[4]	-	145	-	µA
		power-down mode	[4]	-	23	-	µA
		deep power-down mode	[4][6]	-	0.05	-	µA
		deep power-down mode; VBAT floating	[4]	-	3.0	-	µA
I_{BAT}	battery supply current	V_{BAT} = 3.0 V; $V_{DD(REG)(3V3)}$ = 3.3 V	[7]	-		0.1	nA

10.4 BOD and band gap static characteristics

Table 13. BOD static characteristics[1]

T_{amb} = 25 °C; simulated values for nominal processing.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 2					
		assertion		-	2.95	-	V
		de-assertion		-	3.03	-	V
		interrupt level 3					
		assertion		-	3.05	-	V
		de-assertion		-	3.13	-	V
		reset level 2					
		assertion		-	2.1	-	V
		de-assertion		-	2.18	-	V
		reset level 3					
		assertion		-	2.2	-	V
		de-assertion		-	2.28	-	V

[1] Interrupt and reset levels are selected by writing to the BODLV1/2 bits in the control register CREGE0, see the *LPC43xx user manual*.

Table 14. Band gap characteristics

$V_{DDA(3V3)}$ over specified ranges; T_{amb} = −40 °C to +105 °C; unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Unit
$V_{ref(bg)}$	band gap reference voltage	[1]	0.707	0.745	0.783	mV

[1] Based on characterization, not tested in production.

11.2 Wake-up times

Table 17. Dynamic characteristic: Wake-up from Deep-sleep, Power-down, and Deep power-down modes

T_{amb} = −40 °C to +105 °C

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from Sleep mode	[2]	$3 \times T_{cy(clk)}$	$5 \times T_{cy(clk)}$	-	ns
		from Deep-sleep and Power-down mode		12	51	-	µs
		from Deep power-down mode		-	200	-	µs
		after reset		-	200	-	µs

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] $T_{cy(clk)}$ = 1/CCLK with CCLK = CPU clock frequency.

11.3 External clock for oscillator in slave mode

Remark: The input voltage on the XTAL1/2 pins must be ≤ 1.2 V (see Table 11). For connecting the oscillator to the XTAL pins, also see Section 13.2 and Section 13.4.

Table 18. Dynamic characteristic: external clock

T_{amb} = −40 °C to +105 °C; $V_{DD(IO)}$ over specified ranges.[1]

Symbol	Parameter	Conditions		Min	Max	Unit
f_{osc}	oscillator frequency			1	25	MHz
$T_{cy(clk)}$	clock cycle time			40	1000	ns
t_{CHCX}	clock HIGH time			$T_{cy(clk)} \times 0.4$	$T_{cy(clk)} \times 0.6$	ns
t_{CLCX}	clock LOW time			$T_{cy(clk)} \times 0.4$	$T_{cy(clk)} \times 0.6$	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

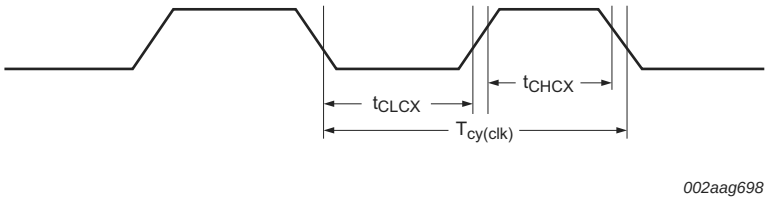


Fig 25. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

11.4 Crystal oscillator

Table 19. Dynamic characteristic: oscillator

T_{amb} = −40 °C to +105 °C; $V_{DD(IO)}$ over specified ranges; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
Low-frequency mode (1-20 MHz)[5]							
$t_{jit(per)}$	period jitter time	5 MHz crystal	[3][4]	-	13.2	-	ps
		10 MHz crystal		-	6.6	-	ps
		15 MHz crystal		-	4.8	-	ps
High-frequency mode (20 - 25 MHz)[6]							
$t_{jit(per)}$	period jitter time	20 MHz crystal	[3][4]	-	4.3	-	ps
		25 MHz crystal		-	3.7	-	ps

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Indicates RMS period jitter.

[4] PLL-induced jitter is not included.

[5] Select HF = 0 in the XTAL_OSC_CTRL register.

[6] Select HF = 1 in the XTAL_OSC_CTRL register.

11.5 IRC oscillator

Table 20. Dynamic characteristic: IRC oscillator

2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-40 °C ≤ T_{amb} < 0 °C	12.0 - 3 %	12.0	12.0 + 3 %	MHz
		0 °C ≤ T_{amb} ≤ 85 °C	12.0 - 1.5 %	12.0	12.0 + 1.5 %	MHz
		85 °C < T_{amb} < 105 °C	12.0 - 3 %	12.0	12.0 + 3 %	MHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.6 RTC oscillator

See Section 13.3 for connecting the RTC oscillator to an external clock source.

Table 21. Dynamic characteristic: RTC oscillator

T_{amb} = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V or 2.4 V ≤ V_{BAT} ≤ 3.6 V[1]

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_i	input frequency	-		-	32.768	-	kHz
$I_{CC(osc)}$	oscillator supply current				280	800	nA

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.7 GPCLKIN

Table 22. Dynamic characteristic: GPCLKIN

T_{amb} = 25 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V

Symbol	Parameter	Min	Typ	Max	Unit
GP_CLKIN	input frequency	-	-	25	MHz

11.8 I/O pins

Table 23. Dynamic characteristic: I/O pins[1]

T_{amb} = −40 °C to +85 °C; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Standard I/O pins - normal drive strength							
t_r	rise time	pin configured as output; EHS = 1	[2][3]	1.0	-	2.5	ns
t_f	fall time	pin configured as output; EHS = 1	[2][3]	0.9	-	2.5	ns
t_r	rise time	pin configured as output; EHS = 0	[2][3]	1.9	-	4.3	ns
t_f	fall time	pin configured as output; EHS = 0	[2][3]	1.9	-	4.0	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns
I/O pins - high drive strength							
t_r	rise time	pin configured as output; standard drive mode (EHD = 0x0)	[2][5]	4.3	-	7.9	ns
t_f	fall time	pin configured as output; standard drive mode (EHD = 0x0)	[2][5]	4.7	-	8.7	ns
t_r	rise time	pin configured as output; medium drive mode (EHD = 0x1)	[2][5]	3.2	-	5.7	ns
t_f	fall time	pin configured as output; medium drive mode (EHD = 0x1)	[2][5]	3.2	-	5.5	ns
t_r	rise time	pin configured as output; high drive mode (EHD = 0x2)	[2][5]	2.9	-	4.9	ns
t_f	fall time	pin configured as output; high drive mode (EHD = 0x2)	[2][5]	2.5	-	3.9	ns
t_r	rise time	pin configured as output; ultra-high drive mode (EHD = 0x3)	[2][5]	2.8	-	4.7	ns
t_f	fall time	pin configured as output; ultra-high drive mode (EHD = 0x3)	[2][5]	2.4	-	3.4	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns
I/O pins - high-speed							
t_r	rise time	pin configured as output; EHS = 1	[2][3]	350	-	670	ps
t_f	fall time	pin configured as output; EHS = 1	[2][3]	450	-	730	ps
t_r	rise time	pin configured as output; EHS = 0	[2][3]	1.0	-	1.9	ns
t_f	fall time	pin configured as output; EHS = 0	[2][3]	1.0	-	2.0	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns

[1] Simulated data.

[9] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

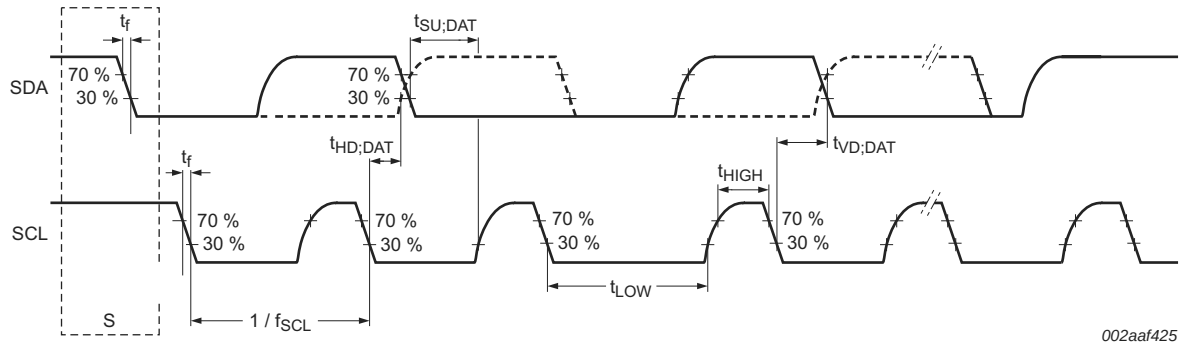


Fig 26. I^2C-bus pins clock timing

11.10 I^2S-bus interface

Table 25. Dynamic characteristics: I^2S-bus interface pins

T_{amb} = −40 °C to 105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Conditions and data refer to I2S0 and I2S1 pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
common to input and output							
t_r	rise time			-	4	-	ns
t_f	fall time			-	4	-	ns
t_{WH}	pulse width HIGH	on pins I2Sx_TX_SCK and I2Sx_RX_SCK		36	-	-	ns
t_{WL}	pulse width LOW	on pins I2Sx_TX_SCK and I2Sx_RX_SCK		36	-	-	ns
output							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[1]	-	4.4	-	ns
		on pin I2Sx_TX_WS		-	4.3	-	ns
input							
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[1]	-	0	-	ns
		on pin I2Sx_RX_WS			0.20		ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[1]	-	3.7	-	ns
		on pin I2Sx_RX_WS		-	3.9	-	ns

[1] Clock to the I^2S-bus interface BASE_APB1_CLK = 150 MHz; peripheral clock to the I^2S-bus interface PCLK = BASE_APB1_CLK / 12. I^2S clock cycle time $T_{cy(clk)}$ = 79.2 ns, corresponds to the SCK signal in the *I^2S-bus specification*.

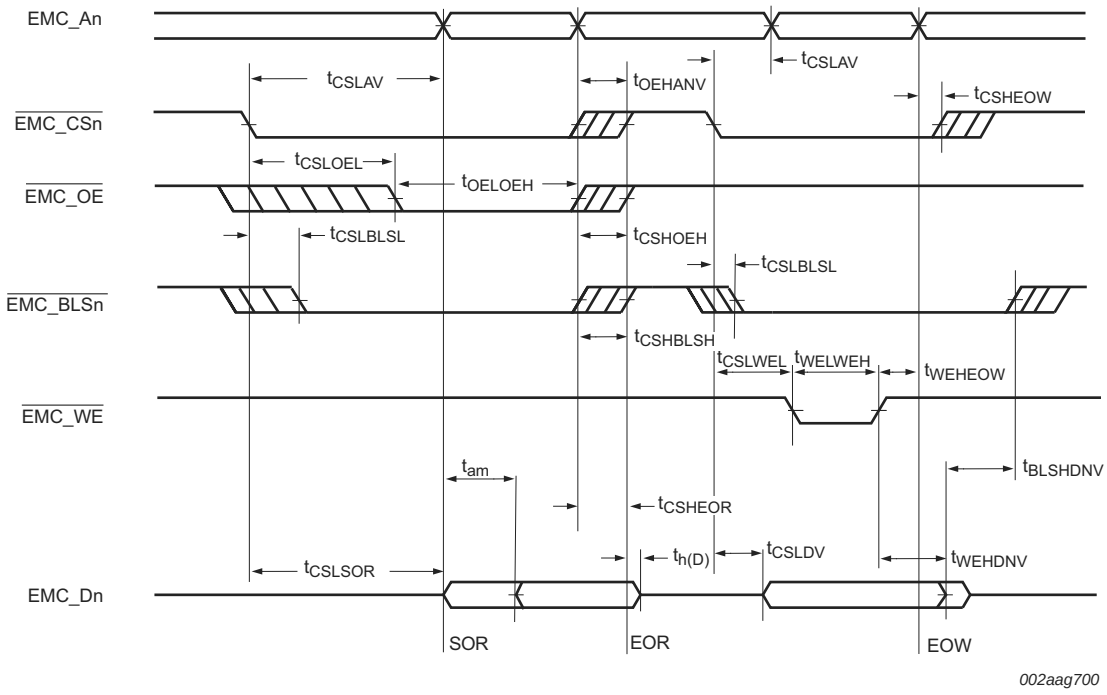


Fig 35. External static memory read/write access (PB = 1)

Table 36. Dynamic characteristics: Ethernet

T_{amb} = −40 °C to 105 °C, 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V. Values guaranteed by design.

Symbol	Parameter	Conditions		Min	Max	Unit
RMII mode						
f_{clk}	clock frequency	for ENET_RX_CLK	[1]	-	50	MHz
δ_{clk}	clock duty cycle		[1]	50	50	%
t_{su}	set-up time	for ENET_TXDn, ENET_TX_EN, ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	4	-	ns
t_h	hold time	for ENET_TXDn, ENET_TX_EN, ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	2	-	ns
MII mode						
f_{clk}	clock frequency	for ENET_TX_CLK	[1]	-	25	MHz
δ_{clk}	clock duty cycle		[1]	50	50	%
t_{su}	set-up time	for ENET_TXDn, ENET_TX_EN, ENET_TX_ER	[1][2]	4	-	ns
t_h	hold time	for ENET_TXDn, ENET_TX_EN, ENET_TX_ER	[1][2]	2	-	ns
f_{clk}	clock frequency	for ENET_RX_CLK	[1]	-	25	MHz
δ_{clk}	clock duty cycle		[1]	50	50	%
t_{su}	set-up time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	4	-	ns
t_h	hold time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	2	-	ns

[1] Output drivers can drive a load ≥ 25 pF accommodating over 12 inch of PCB trace and the input capacitance of the receiving device.

[2] Timing values are given from the point at which the clock signal waveform crosses 1.4 V to the valid input or output level.

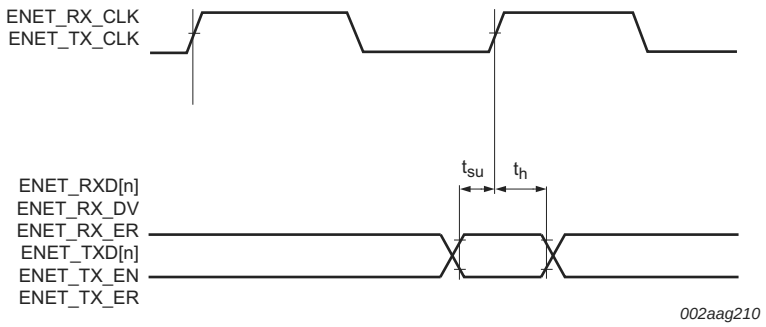


Fig 38. Ethernet timing

11.20 SD/MMC

Table 37. Dynamic characteristics: SD/MMC

T_{amb} = −40 °C to +105 °C, 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V, C_L = 20 pF. SAMPLE_DELAY = 0x9, DRV_DELAY = 0x6 in the SDDELAY register, sampled at 90 % and 10 % of the signal level, EHS = 1 for SD_CLK pin, EHS = 0 for SD_DATn and SD_CMD pins. Simulated values.

Symbol	Parameter	Conditions	Min	Max	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode	-	52	MHz
$t_{su(D)}$	data input set-up time	on pins SD_DATn as inputs	5.2	-	ns
		on pins SD_CMD as inputs	7	-	ns
$t_{h(D)}$	data input hold time	on pins SD_DATn as inputs	0.2	-	ns
		on pins SD_CMD as inputs	−1		ns
$t_{d(QV)}$	data output valid delay time	on pins SD_DATn as outputs	-	15.7	ns
		on pins SD_CMD as outputs	-	15.9	ns
$t_{h(Q)}$	data output hold time	on pins SD_DATn as outputs	3.5	-	ns
		on pins SD_CMD as outputs	3.5	-	ns

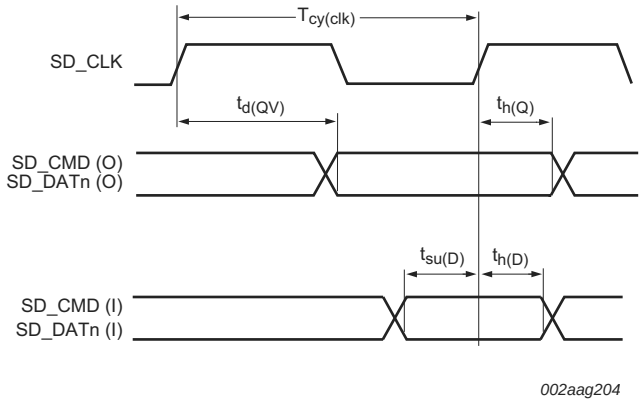


Fig 39. SD/MMC timing

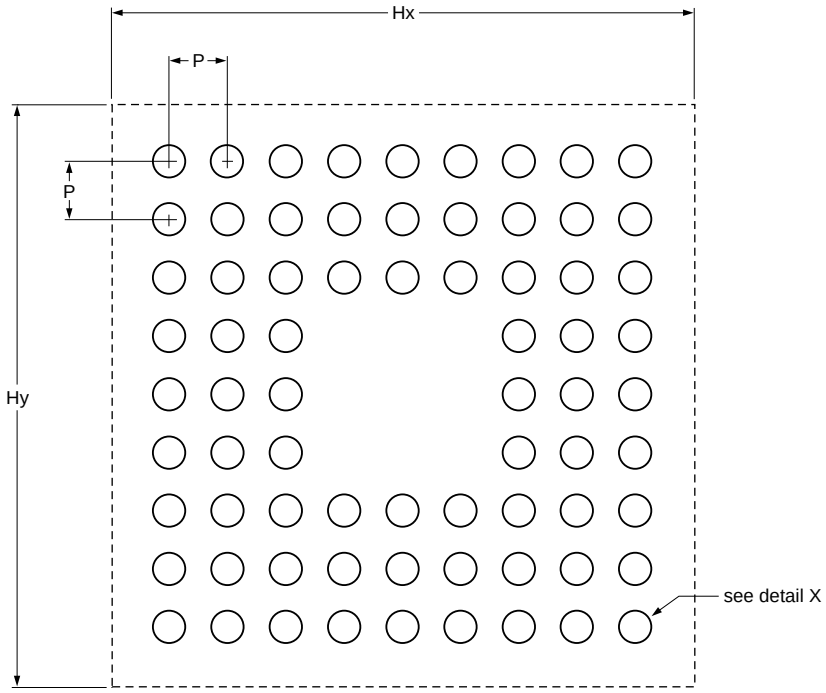
11.21 LCD

Table 38. Dynamic characteristics: LCD

T_{amb} = −40 °C to 105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Simulated values.

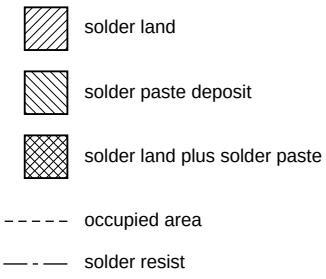
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	on pin LCD_DCLK	-	50	-	MHz
$t_{d(QV)}$	data output valid delay time		-	-	17	ns
$t_{h(Q)}$	data output hold time		8.5	-	-	ns

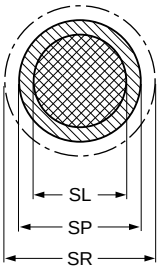
Footprint information for reflow soldering of TFBGA100 package **SOT926-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout





detail X

DIMENSIONS in mm

P	SL	SP	SR	Hx	Hy
0.80	0.330	0.400	0.480	9.400	9.400

sot926-1_fr

Fig 55. Reflow soldering of the TFBGA100 package