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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, MMC/SD, QEI, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	49
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	154K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 16x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4367jet100e

5. Block diagram

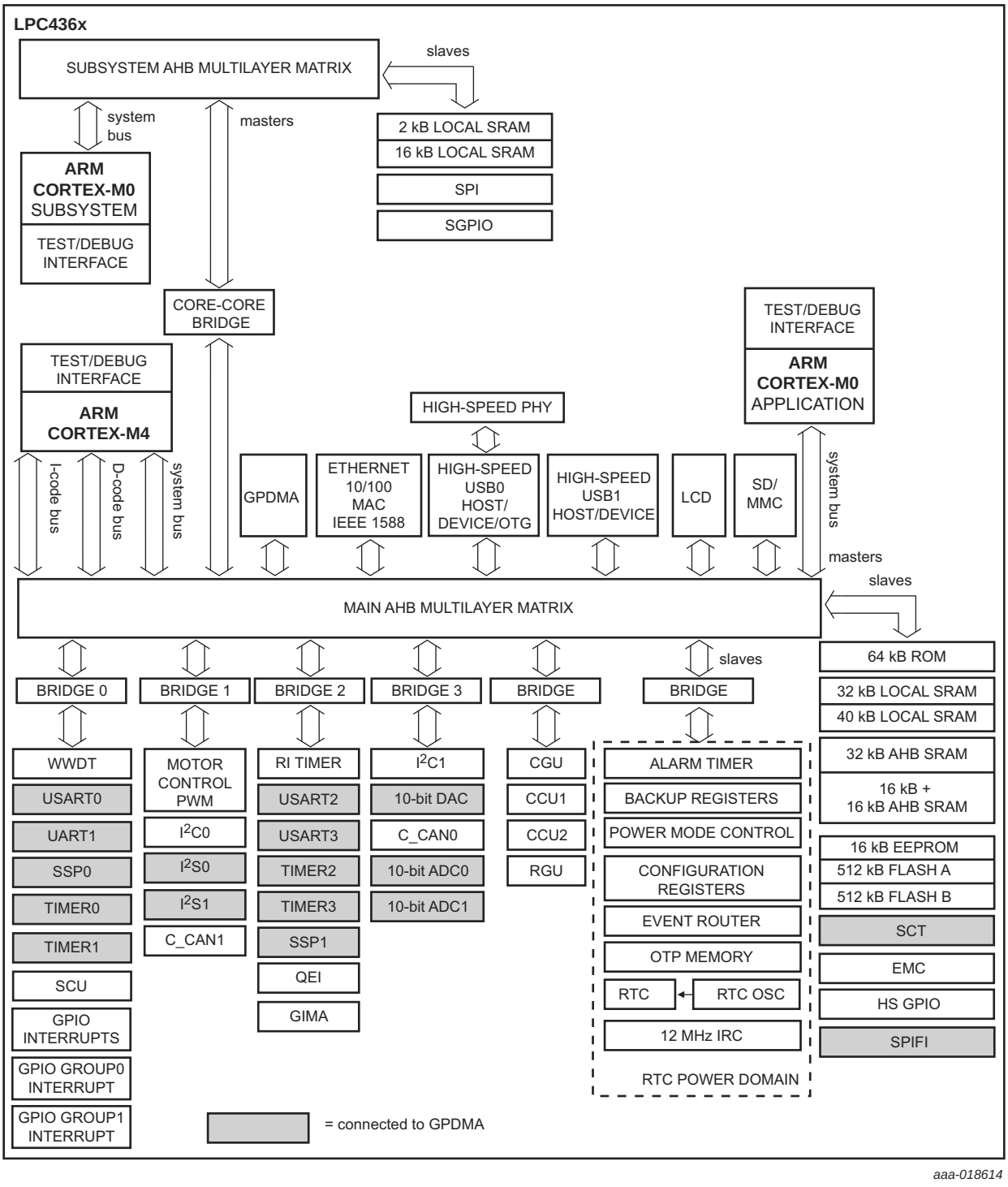


Fig 1. LPC436x Block diagram

6. Pinning information

6.1 Pinning

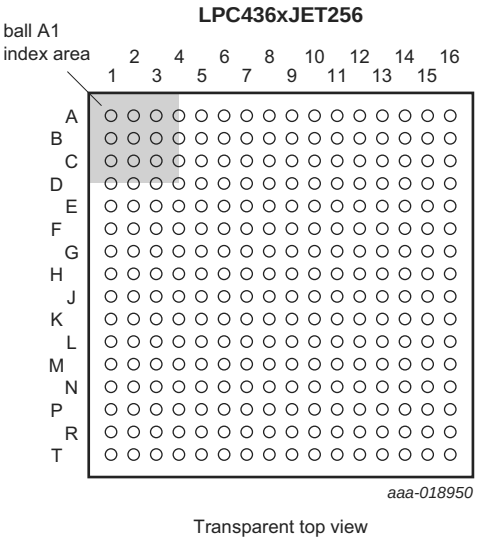


Fig 2. Pin configuration LBGA256 package

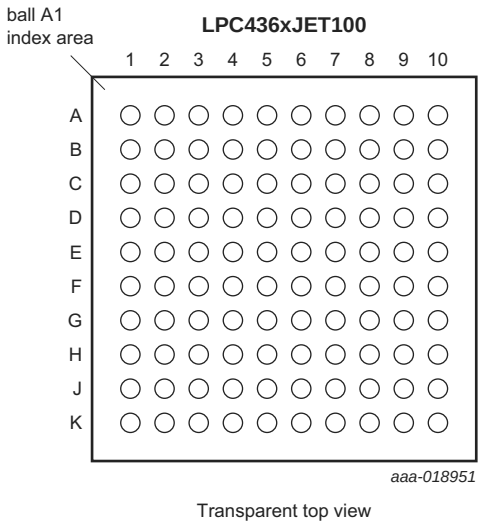


Fig 3. Pin configuration TFBGA100 package

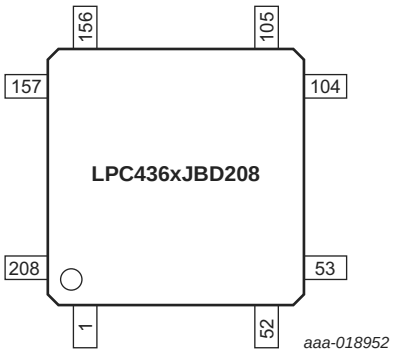


Fig 4. Pin configuration LQFP208 package

6.2 Pin description

On the LPC436x, digital pins are grouped into 16 ports, named P0 to P9 and PA to PF, with up to 20 pins used per port. Each digital pin can support up to eight different digital functions, including General Purpose I/O (GPIO), selectable through the System Configuration Unit (SCU) registers. The pin name is not indicative of the GPIO port assigned to it.

The parts contain two 10-bit ADCs (ADC0 and ADC1). The input channels of ADC0 and ADC1 on dedicated pins and multiplexed pins are combined in such a way that all channel 0 inputs (named ADC0_0 and ADC1_0) are tied together and connected to both, channel 0 on ADC0 and channel 0 on ADC1, channel 1 inputs (named ADC0_1 and ADC1_1) are tied together and connected to channel 1 on ADC0 and ADC1, and so forth. There are eight ADC channels total for the two ADCs.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
P1_1	R2	K2	58	[2]	N; PU	I/O	**GPIO0[8] —** General purpose digital input/output pin. Boot pin (see Table 5).
						O	**CTOUT_7 —** SCT output 7. Match output 3 of timer 1.
						I/O	**EMC_A6 —** External memory address line 6.
						I/O	**SGPIO8 —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
						-	**R —** Function reserved.
						I/O	**EMC_D13 —** External memory data line 13.
P1_2	R3	K1	60	[2]	N; PU	I/O	**GPIO0[9] —** General purpose digital input/output pin. Boot pin (see Table 5).
						O	**CTOUT_6 —** SCT output 6. Match output 2 of timer 1.
						I/O	**EMC_A7 —** External memory address line 7.
						I/O	**SGPIO9 —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
						-	**R —** Function reserved.
						I/O	**EMC_D14 —** External memory data line 14.
P1_3	P5	J1	61	[2]	N; PU	I/O	**GPIO0[10] —** General purpose digital input/output pin.
						O	**CTOUT_8 —** SCT output 8. Match output 0 of timer 2.
						I/O	**SGPIO10 —** General purpose digital input/output pin.
						O	**EMC_OE —** LOW active Output Enable signal.
						O	**USB0_IND1 —** USB0 port indicator LED control output 1.
						I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
						-	**R —** Function reserved.
						O	**SD_RST —** SD/MMC reset signal for MMC4.4 card.
P1_4	T3	J2	64	[2]	N; PU	I/O	**GPIO0[11] —** General purpose digital input/output pin.
						O	**CTOUT_9 —** SCT output 9. Match output 3 of timer 3.
						I/O	**SGPIO11 —** General purpose digital input/output pin.
						O	**EMC_BLS0 —** LOW active Byte Lane select signal 0.
						O	**USB0_IND0 —** USB0 port indicator LED control output 0.
						I/O	**SSP1_MOSI —** Master Out Slave in for SSP1.
						I/O	**EMC_D15 —** External memory data line 15.
						O	**SD_VOLT1 —** SD/MMC bus voltage select output 1.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
P1_8	R7	H5	71	[2]	N; PU	I/O	**GPIO1[1] —** General purpose digital input/output pin.
						O	**U1_DTR —** Data Terminal Ready output for UART1.
						O	**CTOUT_12 —** SCT output 12. Match output 3 of timer 3.
						I/O	**EMC_D1 —** External memory data line 1.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**SD_VOLT0 —** SD/MMC bus voltage select output 0.
P1_9	T7	J5	73	[2]	N; PU	I/O	**GPIO1[2] —** General purpose digital input/output pin.
						O	**U1_RTS —** Request to Send output for UART1.
						O	**CTOUT_11 —** SCT output 11. Match output 3 of timer 2.
						I/O	**EMC_D2 —** External memory data line 2.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SD_DAT0 —** SD/MMC data bus line 0.
P1_10	R8	H6	75	[2]	N; PU	I/O	**GPIO1[3] —** General purpose digital input/output pin.
						I	**U1_RI —** Ring Indicator input for UART1.
						O	**CTOUT_14 —** SCT output 14. Match output 2 of timer 3.
						I/O	**EMC_D3 —** External memory data line 3.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SD_DAT1 —** SD/MMC data bus line 1.
P1_11	T9	J7	77	[2]	N; PU	I/O	**GPIO1[4] —** General purpose digital input/output pin.
						I	**U1_CTS —** Clear to Send input for UART1.
						O	**CTOUT_15 —** SCT output 15. Match output 3 of timer 3.
						I/O	**EMC_D4 —** External memory data line 4.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SD_DAT2 —** SD/MMC data bus line 2.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
P6_11	H12	C9	143	[2]	N; PU	I/O	**GPIO3[7] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**EMC_CKEOUT0 —** SDRAM clock enable 0.
						-	**R —** Function reserved.
						O	**T2_MAT3 —** Match output 3 of timer 2.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P6_12	G15	-	145	[2]	N; PU	I/O	**GPIO2[8] —** General purpose digital input/output pin.
						O	**CTOUT_7 —** SCT output 7. Match output 3 of timer 1.
						-	**R —** Function reserved.
						O	**EMC_DQMOUT0 —** Data mask 0 used with SDRAM and static devices.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P7_0	B16	-	158	[2]	N; PU	I/O	**GPIO3[8] —** General purpose digital input/output pin.
						O	**CTOUT_14 —** SCT output 14. Match output 2 of timer 3.
						-	**R —** Function reserved.
						O	**LCD_LE —** Line end signal.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SGPIO4 —** General purpose digital input/output pin.
P7_1	C14	-	162	[2]	N; PU	I/O	**GPIO3[9] —** General purpose digital input/output pin.
						O	**CTOUT_15 —** SCT output 15. Match output 3 of timer 3.
						I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
						O	**LCD_VD19 —** LCD data.
						O	**LCD_VD7 —** LCD data.
						-	**R —** Function reserved.
						O	**U2_TXD —** Transmitter output for USART2.
						I/O	**SGPIO5 —** General purpose digital input/output pin.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
PC_14	N1	-	-	[2]	N; PU	-	**R —** Function reserved.
						-	**R —** Function reserved.
						I	**U1_RXD —** Receiver input for UART 1.
						-	**R —** Function reserved.
						I/O	**GPIO6[13] —** General purpose digital input/output pin.
						I/O	**SGPIO13 —** General purpose digital input/output pin.
						O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
						I/O	**SD_DAT7 —** SD/MMC data bus line 7.
PD_0	N2	-	-	[2]	N; PU	-	**R —** Function reserved.
						O	**CTOUT_15 —** SCT output 15. Match output 3 of timer 3.
						O	**EMC_DQMOUT2 —** Data mask 2 used with SDRAM and static devices.
						-	**R —** Function reserved.
						I/O	**GPIO6[14] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SGPIO4 —** General purpose digital input/output pin.
PD_1	P1	-	-	[2]	N; PU	-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**EMC_CKEOUT2 —** SDRAM clock enable 2.
						-	**R —** Function reserved.
						I/O	**GPIO6[15] —** General purpose digital input/output pin.
						O	**SD_POW —** SD/MMC power monitor output.
						-	**R —** Function reserved.
						I/O	**SGPIO5 —** General purpose digital input/output pin.
PD_2	R1	-	-	[2]	N; PU	-	**R —** Function reserved.
						O	**CTOUT_7 —** SCT output 7. Match output 3 of timer 1.
						I/O	**EMC_D16 —** External memory data line 16.
						-	**R —** Function reserved.
						I/O	**GPIO6[16] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SGPIO6 —** General purpose digital input/output pin.

One application of using the subsystem is to reduce power, for example when the main matrix runs at a very low speed and the M0 subsystem monitors activity and increases the main matrix speed when needed. Another application for the subsystem is to manage the serial GPIO peripheral, which can be configured as additional SPI, I2S, or other serial interface.

One of the two SRAM blocks connected to the subsystem AHB matrix is typically used for code running on the M0 subsystem and the other SRAM block for data. This allows other bus masters to access the data SRAM without interrupting the M0 processor instruction fetches and thereby stalling the M0 subsystem.

The M0 subsystem matrix runs at an asynchronous speed from the main matrix. This allows to operate the SGPIO at any desired frequency. The M0 subsystem can control the SGPIO in a deterministic way, without incurring latency that occurs when the M4 controls the SGPIO through a bridge.

7.4 Interprocessor communication

The ARM Cortex-M4 and ARM Cortex-M0 interprocessor communication is based on using shared SRAM as mailbox and one processor raising an interrupt on the other processor's NVIC, for example after it has delivered a new message in the mailbox. The receiving processor can reply by raising an interrupt on the sending processor's NVIC to acknowledge the message.

- Supports booting from external static memory such as NOR flash, SPI flash, quad SPI flash, USB0, and USB1.
- Includes API for OTP programming.
- Includes a flexible USB device stack that supports Human Interface Device (HID), Mass Storage Class (MSC), and Device Firmware Upgrade (DFU) drivers.

Several boot modes are available if P2_7 is LOW on reset depending on the values of the OTP bits BOOT_SRC. If the OTP memory is not programmed or the BOOT_SRC bits are all zero, the boot mode is determined by the states of the boot pins P2_9, P2_8, P1_2, and P1_1.

Table 4. Boot mode when OTP BOOT_SRC bits are programmed

Boot mode	BOOT_SRC bit 3	BOOT_SRC bit 2	BOOT_SRC bit 1	BOOT_SRC bit 0	Description
Pin state	0	0	0	0	Boot source is defined by the reset state of P1_1, P1_2, P2_8 pins, and P2_9. See Table 5.
USART0	0	0	0	1	Enter ISP mode using USART0 pins P2_0 and P2_1.
SPIFI	0	0	1	0	Boot from Quad SPI flash connected to the SPIFI interface using pins P3_3 to P3_8.
EMC 8-bit	0	0	1	1	Boot from external static memory (such as NOR flash) using CS0 and an 8-bit data bus.
EMC 16-bit	0	1	0	0	Boot from external static memory (such as NOR flash) using CS0 and a 16-bit data bus.
EMC 32-bit	0	1	0	1	Boot from external static memory (such as NOR flash) using CS0 and a 32-bit data bus.
USB0	0	1	1	0	Boot from USB0.
USB1	0	1	1	1	Boot from USB1.
SPI (SSP)	1	0	0	0	Boot from SPI flash connected to the SSP0 interface on P3_3 (function SSP0_SCK), P3_6 (function SSP0_SSEL), P3_7 (function SSP0_MISO), and P3_8 (function SSP0_MOSI)[1].
USART3	1	0	0	1	Enter ISP mode using USART3 pins P2_3 and P2_4.

[1] The boot loader programs the appropriate pin function at reset to boot using either SSP0 or SPIFI.
Remark: Pin functions for SPIFI and SSP0 boot are different.

Table 5. Boot mode when OPT BOOT_SRC bits are zero

Boot mode	Pins				Description
	P2_9	P2_8	P1_2	P1_1	
USART0	LOW	LOW	LOW	LOW	Enter ISP mode using USART0 pins P2_0 and P2_1.
SPIFI	LOW	LOW	LOW	HIGH	Boot from Quad SPI flash connected to the SPIFI interface on P3_3 to P3_8[1].
EMC 8-bit	LOW	LOW	HIGH	LOW	Boot from external static memory (such as NOR flash) using CS0 and an 8-bit data bus.
EMC 16-bit	LOW	LOW	HIGH	HIGH	Boot from external static memory (such as NOR flash) using CS0 and a 16-bit data bus.

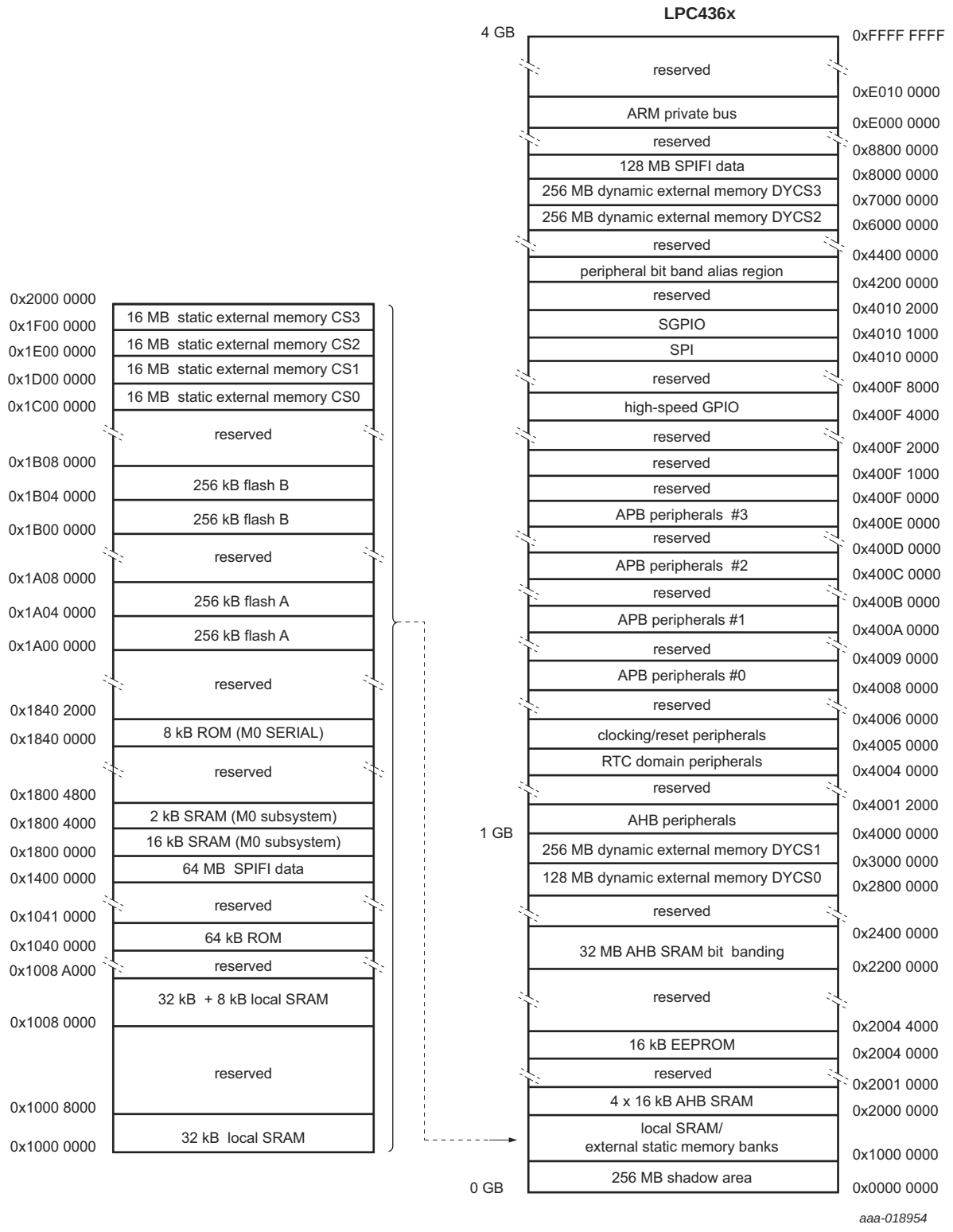


Fig 6. LPC436x Memory mapping (overview)

After a few commands configure the interface at startup, the entire flash content is accessible as normal memory using byte, halfword, and word accesses by the processor and/or DMA channels. Simple sequences of commands handle erasing and programming.

Many serial flash devices use a half-duplex command-driven SPI protocol for device setup and initialization and then move to a half-duplex, command-driven 4-bit protocol for normal operation. Different serial flash vendors and devices accept or require different commands and command formats. SPIFI provides sufficient flexibility to be compatible with common flash devices and includes extensions to help insure compatibility with future devices.

7.18.2.1 Features

- Interfaces to serial flash memory in the main memory map.
- Supports classic and 4-bit bidirectional serial protocols.
- Half-duplex protocol compatible with various vendors and devices.
- Quad SPI Flash Interface (SPIFI) with 1-, 2-, or 4-bit data at rates of up to 52 MB per second.
- Supports DMA access.

7.18.3 SD/MMC card interface

The SD/MMC card interface supports the following modes to control:

- Secure Digital memory (SD version 3.0)
- Secure Digital I/O (SDIO version 2.0)
- Consumer Electronics Advanced Transport Architecture (CE-ATA version 1.1)
- MultiMedia Cards (MMC version 4.4)

7.18.4 External Memory Controller (EMC)

Remark: The EMC is available on all LPC436x parts. The following memory bus widths are supported:

- LBGA256 packages: 32 bit
- TFBGA100 packages: 16 bit
- LQFP208 packages: 16 bit

The LPC436x EMC is a Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and NOR flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals.

Table 6. EMC pinout for different packages

Function	LBGA256	TFBGA100	LQFP208
A	EMC_A[23:0]	EMC_A[13:0]	EMC_A[23:0]
D	EMC_D[31:0]	EMC_D[15:0]	EMC_D[15:0]
$\overline{\text{BLS}}$	$\overline{\text{EMC\_BLS[3:0]}}$	$\overline{\text{EMC\_BLS0}}$	$\overline{\text{EMC\_BLS[1:0]}}$
$\overline{\text{CS}}$	$\overline{\text{EMC\_CS[3:0]}}$	$\overline{\text{EMC\_CS0}}$	$\overline{\text{EMC\_CS[3:0]}}$
$\overline{\text{OE}}$	$\overline{\text{EMC\_OE}}$	$\overline{\text{EMC\_OE}}$	$\overline{\text{EMC\_OE}}$

7.23.2 System Control Unit (SCU)

The system control unit determines the function and electrical mode of the digital pins. By default function 0 is selected for all pins with pull-up enabled. For pins that support a digital and analog function, the ADC function select registers in the SCU enable the analog function.

A separate set of analog I/Os for the ADCs and the DAC as well as most USB pins are located on separate pads and are not controlled through the SCU.

In addition, the clock delay register for the SDRAM EMC_CLK pins and the registers that select the pin interrupts are located in the SCU.

7.23.3 Clock Generation Unit (CGU)

The Clock Generator Unit (CGU) generates several base clocks. The base clocks can be unrelated in frequency and phase and can have different clock sources within the CGU. One CGU base clock is routed to the CLKOUT pins. The base clock that generates the CPU clock is referred to as CCLK.

Multiple branch clocks are derived from each base clock. The branch clocks offer flexible control for power-management purposes. All branch clocks are outputs of one of two Clock Control Units (CCUs) and can be controlled independently. Branch clocks derived from the same base clock are synchronous in frequency and phase.

7.23.4 Internal RC oscillator (IRC)

The IRC is used as the clock source for the WWDT and/or as the clock that drives the PLLs and the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1.5 % accuracy for T_{amb} = 0 °C to 85 °C and 3% accuracy for T_{amb} = -40 °C to 0 °C and T_{amb} = 85 °C to 105 °C.

Upon power-up or any chip reset, the LPC436x use the IRC as the clock source. The boot loader then configures the PLL1 to provide a 96 MHz clock for the core and PLL0USB or PLL0AUDIO as needed if an external boot source is selected.

7.23.5 PLL0USB (for USB0)

PLL0 is a dedicated PLL for the USB0 High-speed controller.

PLL0 accepts an input clock frequency from an external oscillator in the range of 14 kHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The CCO operates in the range of 4.3 MHz to 550 MHz.

7.23.6 PLL0AUDIO (for audio)

The audio PLL PLL0AUDIO is a general purpose PLL with a very small step size. This PLL accepts an input clock frequency derived from an external oscillator or internal IRC. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). A sigma-delta converter modulates the PLL divider ratios to obtain the desired output frequency. The output frequency can be set as a multiple of the sampling frequency f_s to $32 \times f_s$, $64 \times f_s$, $128 \times f_s$, $256 \times f_s$, $384 \times f_s$, $512 \times f_s$ and the sampling frequency f_s can range from 16 kHz to 192 kHz (16, 22.05, 32, 44.1, 48, 96,192) kHz. Many other frequencies are possible as well using the integrated fractional divider.

Wake-up from sleep mode is caused by an interrupt or event in the core's NVIC. The interrupt is captured in the NVIC and an event is captured in the Event router. Both cores can wake up from sleep mode independently of each other.

Wake-up from the Power-down modes, Deep-sleep, Power-down, and Deep power-down, is caused by an event on the WAKEUP pins or an event from the RTC or alarm timer.

When waking up from Deep power-down mode, the part resets and attempts to boot.

7.23.10 Power control

The LPC436x feature several independent power domains to control power to the core and the peripherals (see Figure 8). The RTC and its associated peripherals (the alarm timer, the CREG block, the OTP controller, the back-up registers, and the event router) are located in the RTC power-domain. The main regulator or a battery supply can power the RTC. A power selector switch ensures that the RTC block is always powered on.

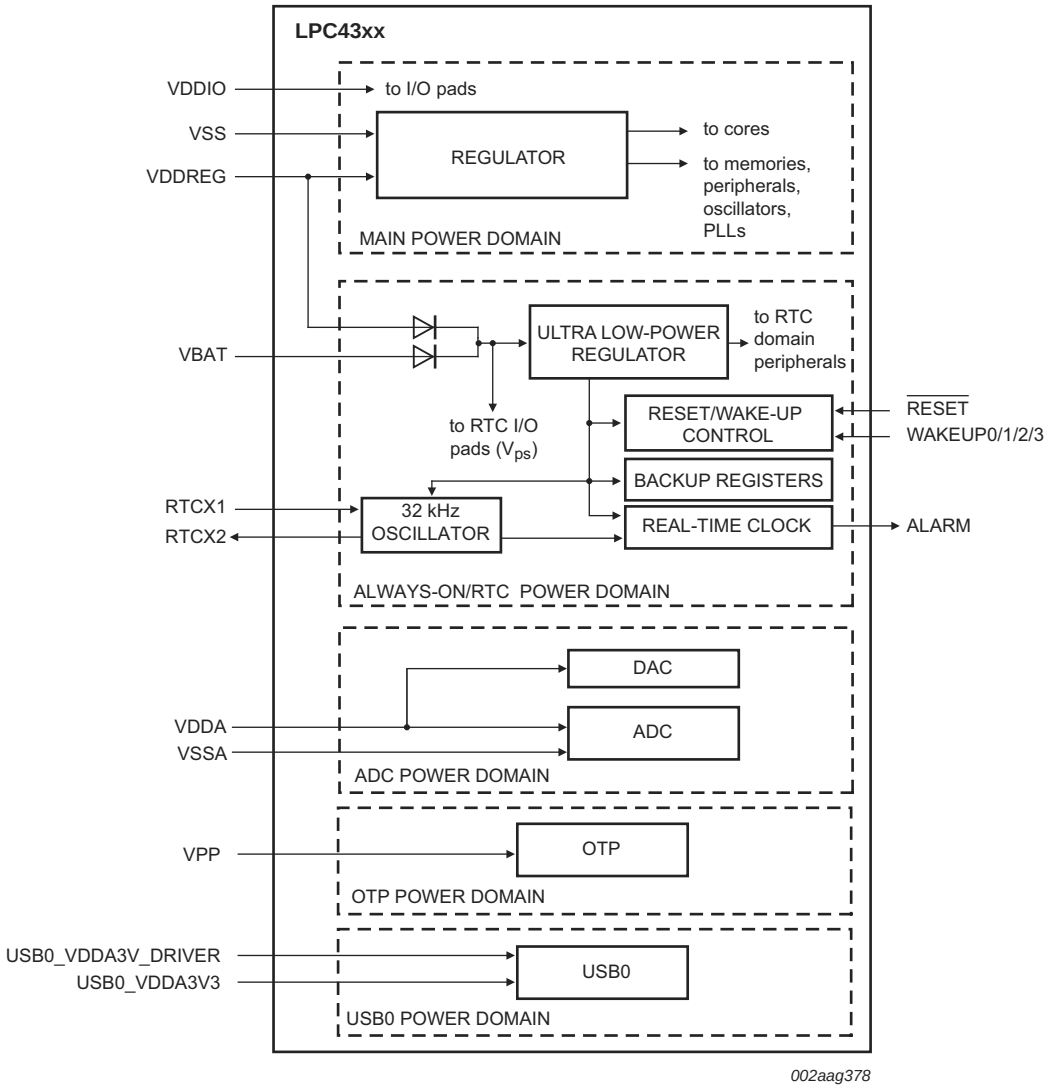


Fig 8. Power domains

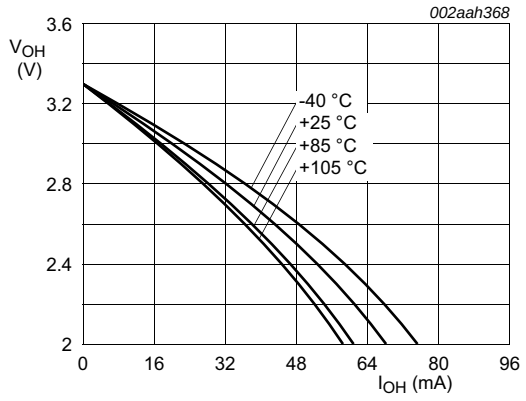
Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{BAT}	battery supply current	$V_{DD(REG)(3V3)}$ = 3.3 V; V_{BAT} = 3.6 V	[8]				
		deep-sleep mode		-	1.5	-	µA
		power-down mode	[8]	-	1.5	-	µA
		deep power-down mode	[8]	-	1.5	-	µA
I_{BAT}	battery supply current	Deep power-down mode; RTC running; $V_{DD(REG)}$ = VDDA = VDDIO = 0 V;		-	3.0	-	µA
		$V_{DD(REG)(3V3)}$ = V_{BAT} = 3.3 V		-	1.5	-	µA
$I_{DD(IO)}$	I/O supply current	deep sleep mode		-	< 0.1	-	µA
		power-down mode		-	< 0.1	-	µA
		deep power-down mode		-	< 0.1	-	µA
I_{DDA}	Analog supply current	on pin VDDA;	[10]	-	0.4	-	
		deep sleep mode					µA
		power-down mode	[10]	-	0.4	-	µA
		deep power-down mode	[10]	-	0.007	-	µA
$\overline{\text{RESET}}$ pin							
V_{IH}	HIGH-level input voltage		[9]	0.8 × (V_{ps} − 0.35)	-	5.5	V
V_{IL}	LOW-level input voltage		[9]	−0.5	-	0.3 × (V_{ps} − 0.1)	V
V_{hys}	hysteresis voltage		[9]	0.05 × (V_{ps} − 0.35)	-	-	V
Standard I/O pins - normal drive strength							
C_I	input capacitance			-	-	2	pF
I_{LL}	LOW-level leakage current	V_I = 0 V; on-chip pull-up resistor disabled		-	3	-	nA
I_{LH}	HIGH-level leakage current	V_I = $V_{DD(IO)}$; on-chip pull-down resistor disabled		-	3	-	nA
		V_I = 5 V; T_{amb} = 25 °C		-	0.5	-	nA
		V_I = 5 V; T_{amb} = 105 °C		-	40	-	nA
I_{OZ}	OFF-state output current	V_O = 0 V to $V_{DD(IO)}$; on-chip pull-up/down resistors disabled; absolute value		-	3	-	nA
V_I	input voltage	pin configured to provide a digital function;		0	-	5.5	V
		$V_{DD(IO)} \geq$ 2.4 V					
		$V_{DD(IO)}$ = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V

Table 12. Peripheral power consumption

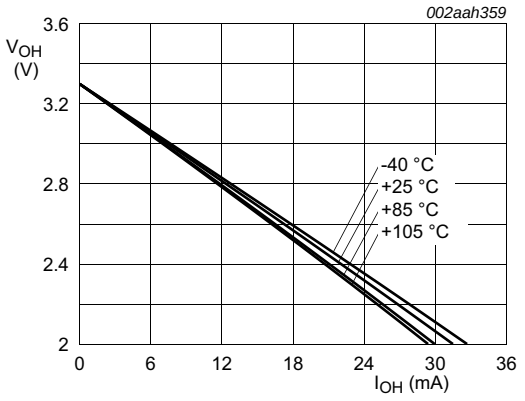
Peripheral	Branch clock	$I_{DD(REG)(3V3)}$ in mA	
		Branch clock frequency = 48 MHz	Branch clock frequency = 96 MHz
SPIFI	CLK_SPIFI, CLK_M4_SPIFI	1.14	2.29
GPIO	CLK_M4_GPIO	0.72	1.43
LCD	CLK_M4_LCD	0.91	1.82
ETHERNET	CLK_M4_ETHERNET	1.06	2.15
UART0	CLK_M4_UART0, CLK_APB0_UART0	0.24	0.43
UART1	CLK_M4_UART1, CLK_APB0_UART1	0.24	0.43
UART2	CLK_M4_UART2, CLK_APB2_UART2	0.26	0.5
UART3	CLK_M4_USART3, CLK_APB2_UART3	0.27	0.45
TIMER0	CLK_M4_TIMER0	0.08	0.15
TIMER1	CLK_M4_TIMER1	0.09	0.15
TIMER2	CLK_M4_TIMER2	0.1	0.19
TIMER3	CLK_M4_TIMER3	0.08	0.16
SDIO	CLK_M4_SDIO, CLK_SDIO	0.66	1.17
SCTimer/PWM	CLK_M4_SCT	0.66	1.3
SSP0	CLK_M4_SSP0, CLK_APB0_SSP0	0.13	0.23
SSP1	CLK_M4_SSP1, CLK_APB2_SSP1	0.14	0.27
DMA	CLK_M4_DMA	1.81	3.61
WWDT	CLK_M4_WWDT	0.03	0.09
QEI	CLK_M4_QEI	0.28	0.55
USB0	CLK_M4_USB0, CLK_USB0	1.9	3.9
USB1	CLK_M4_USB1, CLK_USB1	3.02	5.69
RITIMER	CLK_M4_RITIMER	0.05	0.1
EMC	CLK_M4_EMC, CLK_M4_EMC_DIV	3.94	7.95
SCU	CLK_M4_SCU	0.1	0.21
CREG	CLK_M4_CREG	0.35	0.7
Flash bank A	CLK_M4_FLASHA	1.47	2.97
Flash bank B	CLK_M4_FLASHB	1.4	2.84
SGPIO	CLK_PERIPH_SGPIO	0.1	0.17
SPI	CLK_SPI	0.07	0.11

10.3 Electrical pin characteristics



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V.

Fig 19. Standard I/O pins; typical LOW level output current I_{OL} versus LOW level output voltage V_{OL}



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V.

Fig 20. Standard I/O pins; typical HIGH level output voltage V_{OH} versus HIGH level output current I_{OH}

11.2 Wake-up times

Table 17. Dynamic characteristic: Wake-up from Deep-sleep, Power-down, and Deep power-down modes

T_{amb} = −40 °C to +105 °C

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from Sleep mode	[2]	$3 \times T_{cy(clk)}$	$5 \times T_{cy(clk)}$	-	ns
		from Deep-sleep and Power-down mode		12	51	-	µs
		from Deep power-down mode		-	200	-	µs
		after reset		-	200	-	µs

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] $T_{cy(clk)}$ = 1/CCLK with CCLK = CPU clock frequency.

11.3 External clock for oscillator in slave mode

Remark: The input voltage on the XTAL1/2 pins must be ≤ 1.2 V (see Table 11). For connecting the oscillator to the XTAL pins, also see Section 13.2 and Section 13.4.

Table 18. Dynamic characteristic: external clock

T_{amb} = −40 °C to +105 °C; $V_{DD(IO)}$ over specified ranges.[1]

Symbol	Parameter	Conditions		Min	Max	Unit
f_{osc}	oscillator frequency			1	25	MHz
$T_{cy(clk)}$	clock cycle time			40	1000	ns
t_{CHCX}	clock HIGH time			$T_{cy(clk)} \times 0.4$	$T_{cy(clk)} \times 0.6$	ns
t_{CLCX}	clock LOW time			$T_{cy(clk)} \times 0.4$	$T_{cy(clk)} \times 0.6$	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

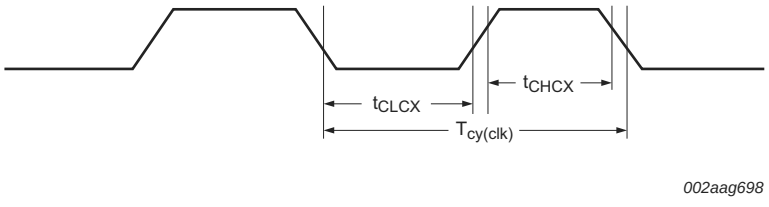


Fig 25. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

Table 27. Dynamic characteristics: SSP pins in SPI mode

T_{amb} = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF; sampled at 10 % and 90 % of the signal level; EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_d	delay time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		-	$0.5 \times T_{cy(clk)}$	-	ns
		SPI mode; CPOL = 0; CPHA = 1		-	n/a	-	ns
		SPI mode; CPOL = 1; CPHA = 0		-	$0.5 \times T_{cy(clk)}$	-	ns
		SPI mode; CPOL = 1; CPHA = 1		-	n/a	-	ns
		synchronous serial frame mode		-	$T_{cy(clk)}$	-	ns
		microwire frame format		-	n/a	-	ns
SSP slave							
PCLK	Peripheral clock frequency			-	-	204	MHz
$T_{cy(clk)}$	clock cycle time		[2]	$1/(11 \times 10^6)$	-	-	s
t_{DS}	data set-up time	in SPI mode		1.5	-	-	ns
t_{DH}	data hold time	in SPI mode		2	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode		-	-	[4 × (1/PCLK)] + 1	ns
$t_{h(Q)}$	data output hold time	in SPI mode		4.5	-	-	ns
t_{lead}	lead time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		$T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 0; CPHA = 1		$0.5 \times T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 1; CPHA = 0		$T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 1; CPHA = 1		$0.5 \times T_{cy(clk)}$	-	-	ns
		synchronous serial frame mode		$0.5 \times T_{cy(clk)}$	-	-	ns
		microwire frame format		$T_{cy(clk)}$	-	-	ns

11.15 SPIFI

Table 29. Dynamic characteristics: SPIFI

T_{amb} = −40 °C to 105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V. C_L = 20 pF. Sampled at 90 % and 10 % of the signal level. EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Min	Max	Unit
$T_{cy(clk)}$	clock cycle time	9.6	-	ns
t_{DS}	data set-up time	3.2	-	ns
t_{DH}	data hold time	0	-	ns
$t_{v(Q)}$	data output valid time	-	3.2	ns
$t_{h(Q)}$	data output hold time	0.6	-	ns

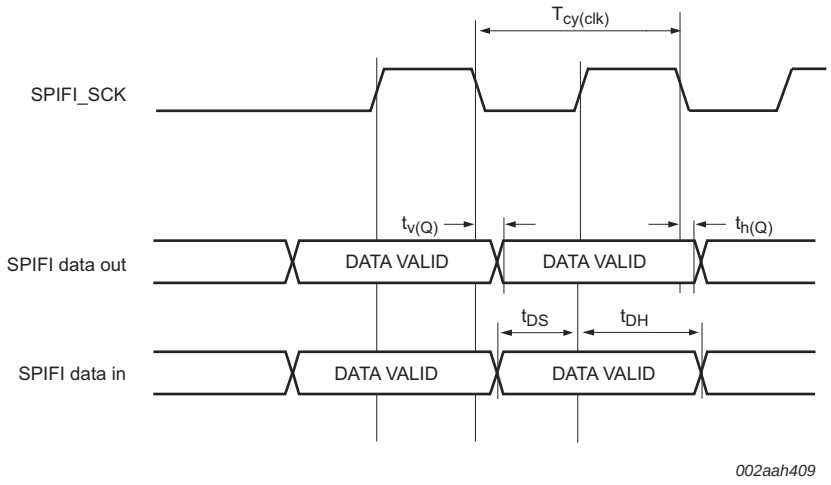


Fig 32. SPIFI timing (Mode 0)

11.16 SGPIO timing

The following considerations apply to SGPIO timing:

- SGPIO input signals are synchronized by the internal clock SGPIO_CLOCK. To guarantee that no samples are missed, all input signals should have a duration of at least one SGPIO_CLOCK cycle plus the set-up and hold times.
- When an external clock input is used to generate output data, synchronization causes a latency of at least one SGPIO_CLOCK cycle. The maximum output data rate is one output every two SGPIO_CLOCK cycles.
- Synchronization also causes a latency of one SGPIO_CLOCK cycle when sampling several inputs. This may cause inputs with very similar timings to be sampled with a difference of one SGPIO_CLOCK cycle.

Table 30. Dynamic characteristics: SGPIO

T_{amb} = −40 °C to +85 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{su(D)}$	data input set-up time			2	-	-	ns
$t_{h(D)}$	data input hold time		[1]	T_{SGPIO} + 2	-	-	ns
$t_{su(D)}$	data input set-up time	sampled by SGPIO_CLOCK	[1]	T_{SGPIO} + 2	-	-	ns
$t_{h(D)}$	data input hold time	sampled by SGPIO_CLOCK	[1]	T_{SGPIO} + 2	-	-	ns
$t_{v(Q)}$	data output valid time		[1]	-	-	2 x T_{SGPIO}	ns
$t_{h(Q)}$	data output hold time		[1]	T_{SGPIO}	-		ns
$t_{v(Q)}$	data output valid time	sampled by SGPIO_CLOCK	[1]	-3	-	3	ns
$t_{h(Q)}$	data output hold time	sampled by SGPIO_CLOCK	[1]	-3	-	3	ns

[1] SGPIO_CLOCK is the internally generated SGPIO clock. $T_{SGPIO} = 1/f_{SGPIO\_CLOCK}$.

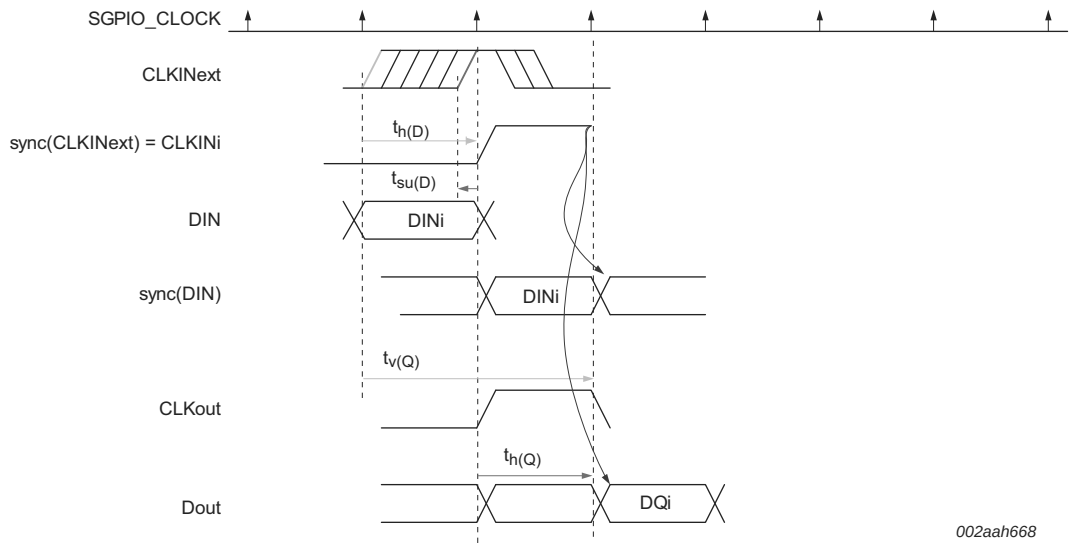


Fig 33. SGPIO timing