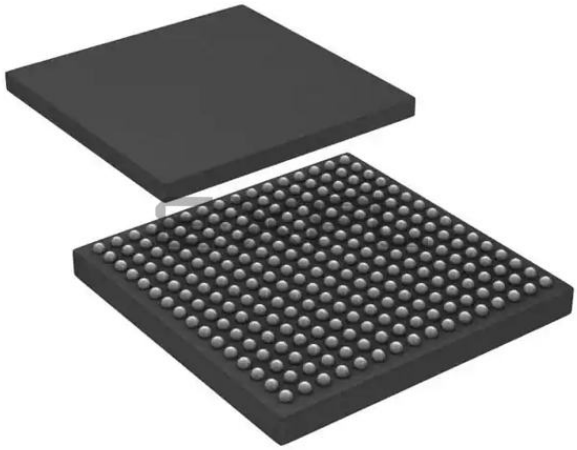

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, MMC/SD, QEI, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	164
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	154K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 16x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-LBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4367jet256e

6.2 Pin description

On the LPC436x, digital pins are grouped into 16 ports, named P0 to P9 and PA to PF, with up to 20 pins used per port. Each digital pin can support up to eight different digital functions, including General Purpose I/O (GPIO), selectable through the System Configuration Unit (SCU) registers. The pin name is not indicative of the GPIO port assigned to it.

The parts contain two 10-bit ADCs (ADC0 and ADC1). The input channels of ADC0 and ADC1 on dedicated pins and multiplexed pins are combined in such a way that all channel 0 inputs (named ADC0_0 and ADC1_0) are tied together and connected to both, channel 0 on ADC0 and channel 0 on ADC1, channel 1 inputs (named ADC0_1 and ADC1_1) are tied together and connected to channel 1 on ADC0 and ADC1, and so forth. There are eight ADC channels total for the two ADCs.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
P4_4	B1	-	14	[5]	N; PU	I/O	**GPIO2[4] —** General purpose digital input/output pin.
						O	**CTOUT_2 —** SCT output 2. Match output 2 of timer 0.
						O	**LCD_VD1 —** LCD data.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**LCD_VD20 —** LCD data.
						I/O	**U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3.
						I/O	**SGPIO10 —** General purpose digital input/output pin.
						O	**DAC —** DAC output. Configure the pin as GPIO input and use the analog function select register in the SCU to select the DAC.
P4_5	D2	-	15	[2]	N; PU	I/O	**GPIO2[5] —** General purpose digital input/output pin.
						O	**CTOUT_5 —** SCT output 5. Match output 3 of timer 3.
						O	**LCD_FP —** Frame pulse (STN). Vertical synchronization pulse (TFT).
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SGPIO11 —** General purpose digital input/output pin.
P4_6	C1	-	17	[2]	N; PU	I/O	**GPIO2[6] —** General purpose digital input/output pin.
						O	**CTOUT_4 —** SCT output 4. Match output 3 of timer 3.
						O	**LCD_ENAB/LCDM —** STN AC bias drive or TFT data enable input.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SGPIO12 —** General purpose digital input/output pin.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
P5_0	N3	-	53	[2]	N; PU	I/O	**GPIO2[9] —** General purpose digital input/output pin.
						O	**MCOB2 —** Motor control PWM channel 2, output B.
						I/O	**EMC_D12 —** External memory data line 12.
						-	**R —** Function reserved.
						I	**U1_DSR —** Data Set Ready input for UART 1.
						I	**T1_CAP0 —** Capture input 0 of timer 1.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P5_1	P3	-	55	[2]	N; PU	I/O	**GPIO2[10] —** General purpose digital input/output pin.
						I	**MCI2 —** Motor control PWM channel 2, input.
						I/O	**EMC_D13 —** External memory data line 13.
						-	**R —** Function reserved.
						O	**U1_DTR —** Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
						I	**T1_CAP1 —** Capture input 1 of timer 1.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P5_2	R4	-	63	[2]	N; PU	I/O	**GPIO2[11] —** General purpose digital input/output pin.
						I	**MCI1 —** Motor control PWM channel 1, input.
						I/O	**EMC_D14 —** External memory data line 14.
						-	**R —** Function reserved.
						O	**U1_RTS —** Request to Send output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
						I	**T1_CAP2 —** Capture input 2 of timer 1.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P5_3	T8	-	76	[2]	N; PU	I/O	**GPIO2[12] —** General purpose digital input/output pin.
						I	**MCI0 —** Motor control PWM channel 0, input.
						I/O	**EMC_D15 —** External memory data line 15.
						-	**R —** Function reserved.
						I	**U1_RI —** Ring Indicator input for UART 1.
						I	**T1_CAP3 —** Capture input 3 of timer 1.
						-	**R —** Function reserved.
						-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
PD_15	T15	-	101	[2]	N; PU	-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**EMC_A17 —** External memory address line 17.
						-	**R —** Function reserved.
						I/O	**GPIO6[29] —** General purpose digital input/output pin.
						I	**SD_WP —** SD/MMC card write protect input.
						O	**CTOUT_8 —** SCT output 8. Match output 0 of timer 2.
						-	**R —** Function reserved.
PD_16	R14	-	104	[2]	N; PU	-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**EMC_A16 —** External memory address line 16.
						-	**R —** Function reserved.
						I/O	**GPIO6[30] —** General purpose digital input/output pin.
						O	**SD_VOLT2 —** SD/MMC bus voltage select output 2.
						O	**CTOUT_12 —** SCT output 12. Match output 3 of timer 3.
						-	**R —** Function reserved.
PE_0	P14	-	106	[2]	N; PU	-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**EMC_A18 —** External memory address line 18.
						I/O	**GPIO7[0] —** General purpose digital input/output pin.
						O	**CAN1_TD —** CAN1 transmitter output.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PE_1	N14	-	112	[2]	N; PU	-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**EMC_A19 —** External memory address line 19.
						I/O	**GPIO7[1] —** General purpose digital input/output pin.
						I	**CAN1_RD —** CAN1 receiver input.
						-	**R —** Function reserved.
						-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
PE_14	C15	-	-	[2]	N; PU	-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**EMC_DYCS3 —** SDRAM chip select 3.
						I/O	**GPIO7[14] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PE_15	E13	-	-	[2]	N; PU	-	**R —** Function reserved.
						O	**CTOUT_0 —** SCT output 0. Match output 0 of timer 0.
						I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I2C pad).
						O	**EMC_CKEOUT3 —** SDRAM clock enable 3.
						I/O	**GPIO7[15] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PF_0	D12	-	159	[2]	O; PU	I/O	**SSP0_SCK —** Serial clock for SSP0.
						I	**GP_CLKIN —** General purpose clock input to the CGU.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**I2S1_TX_MCLK —** I2S1 transmit master clock.
PF_1	E11	-	-	[2]	N; PU	-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SSP0_SSEL —** Slave Select for SSP0.
						-	**R —** Function reserved.
						I/O	**GPIO7[16] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						I/O	**SGPIO0 —** General purpose digital input/output pin.
						-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
PF_9	D6	-	203	[5]	N; PU	-	**R —** Function reserved.
						I/O	**U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0.
						O	**CTOUT_1 —** SCT output 1. Match output 3 of timer 3.
						-	**R —** Function reserved.
						I/O	**GPIO7[23] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						I/O	**SGPIO3 —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						AI	**ADC1_2 —** ADC1 and ADC0, input channel 2. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PF_10	A3	-	205	[5]	N; PU	-	**R —** Function reserved.
						O	**U0_TXD —** Transmitter output for USART0.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**GPIO7[24] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						I	**SD_WP —** SD/MMC card write protect input.
						-	**R —** Function reserved.
						AI	**ADC0_5 —** ADC0 and ADC1, input channel 5. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PF_11	A2	-	207	[5]	N; PU	-	**R —** Function reserved.
						I	**U0_RXD —** Receiver input for USART0.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**GPIO7[25] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						O	**SD_VOLT2 —** SD/MMC bus voltage select output 2.
						-	**R —** Function reserved.
						AI	**ADC1_5 —** ADC1 and ADC0, input channel 5. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
XTAL2	E1	C1	19	[8]	-	O	Output from the oscillator amplifier.
Power and ground pins							
USB0_VDDA3V3_DRIVER	F3	D1	24		-	-	Separate analog 3.3 V power supply for driver.
USB0_VDDA3V3	G3	D2	25		-	-	USB 3.3 V separate power supply voltage.
USB0_VSSA_TERM	H3	D3	27		-	-	Dedicated analog ground for clean reference for termination resistors.
USB0_VSSA_REF	G1	F2	31		-	-	Dedicated clean analog ground for generation of reference currents and voltages.
VDDA	B4	B2	198		-	-	Analog power supply and ADC reference voltage.
VBAT	B10	C5	184		-	-	RTC power supply: 3.3 V on this pin supplies power to the RTC.
VDDREG	F10, F9, L8, L7	E4, E5, F4	135, 188, 195, 82, 33			-	Main regulator power supply. Tie the VDDREG and VDDIO pins to a common power supply to ensure the same ramp-up time for both supply voltages.
VPP	E8	-	-	[12]	-	-	OTP programming voltage.
VDDIO	D7, E12, F7, F8, G10, H10, J6, J7, K7, L9, L10, N7, N13	F10, K5	6, 52, 57, 102, 110, 155, 160, 202	[12]	-	-	I/O power supply. Tie the VDDREG and VDDIO pins to a common power supply to ensure the same ramp-up time for both supply voltages.
VSS	G9, H7, J10, J11, K8	C8, D4, D5, G8, J3, J6	-	[13]	-	-	Ground.
VSSIO	C4, D13, G6, G7, G8, H8, H9, J8, J9, K9, K10, M13, P7, P13	-	5, 56, 109, 157	[13]	-	-	Ground.
VSSA	B2	C2	196		-	-	Analog ground.

[1] N = neutral, input buffer disabled; no extra VDDIO current consumption if the input is driven midway between supplies; set the EZI bit in the SFS register to enable the input buffer; I = input, OL = output driving LOW; OH = output driving HIGH; AI/O = analog input/output; IA = inactive; PU = pull-up enabled (weak pull-up resistor pulls up pin to VDDIO; F = floating. Reset state reflects the pin state at reset without boot code operation.

[2] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength.

7.6 Nested Vectored Interrupt Controller (NVIC)

The NVIC is an integral part of the Cortex-M4. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

The ARM Cortex-M0 co-processor has its own NVIC with 32 vectored interrupts. Most peripheral interrupts are shared between the Cortex-M0 and Cortex-M4 NVICs.

7.6.1 Features

- ARM Cortex-M4 core:
  - Controls system exceptions and peripheral interrupts
  - Support for up to 53 vectored interrupts
  - Eight programmable interrupt priority levels with hardware priority level masking
  - Relocatable vector table
  - Non-Maskable Interrupt (NMI)
  - Software interrupt generation
- ARM Cortex-M0 core:
  - Support for up to 32 interrupts
  - Four programmable interrupt priority levels with hardware priority level masking

7.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

7.7 System Tick timer (SysTick)

The ARM Cortex-M4 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a 10 ms interval.

Remark: The SysTick is not included in the ARM Cortex-M0 core implementation.

7.8 Event router

The event router combines various internal signals, interrupts, and the external interrupt pins (WAKEUP[3:0]) to create an interrupt in the NVIC, if enabled. In addition, the event router creates a wake-up signal to the ARM core and the CCU for waking up from Sleep, Deep-sleep, Power-down, and Deep power-down modes. Individual events can be configured as edge or level sensitive and can be enabled or disabled in the event router. The event router can be battery powered.

The following events if enabled in the event router can create a wake-up signal from sleep, deep-sleep, power-down, and deep power-down modes and/or create an interrupt:

- External pins WAKEUP0/1/2/3 and $\overline{\text{RESET}}$
- Alarm timer, RTC (32 kHz oscillator running)

The following events if enabled in the event router can create a wake-up signal from sleep mode only and/or create an interrupt:

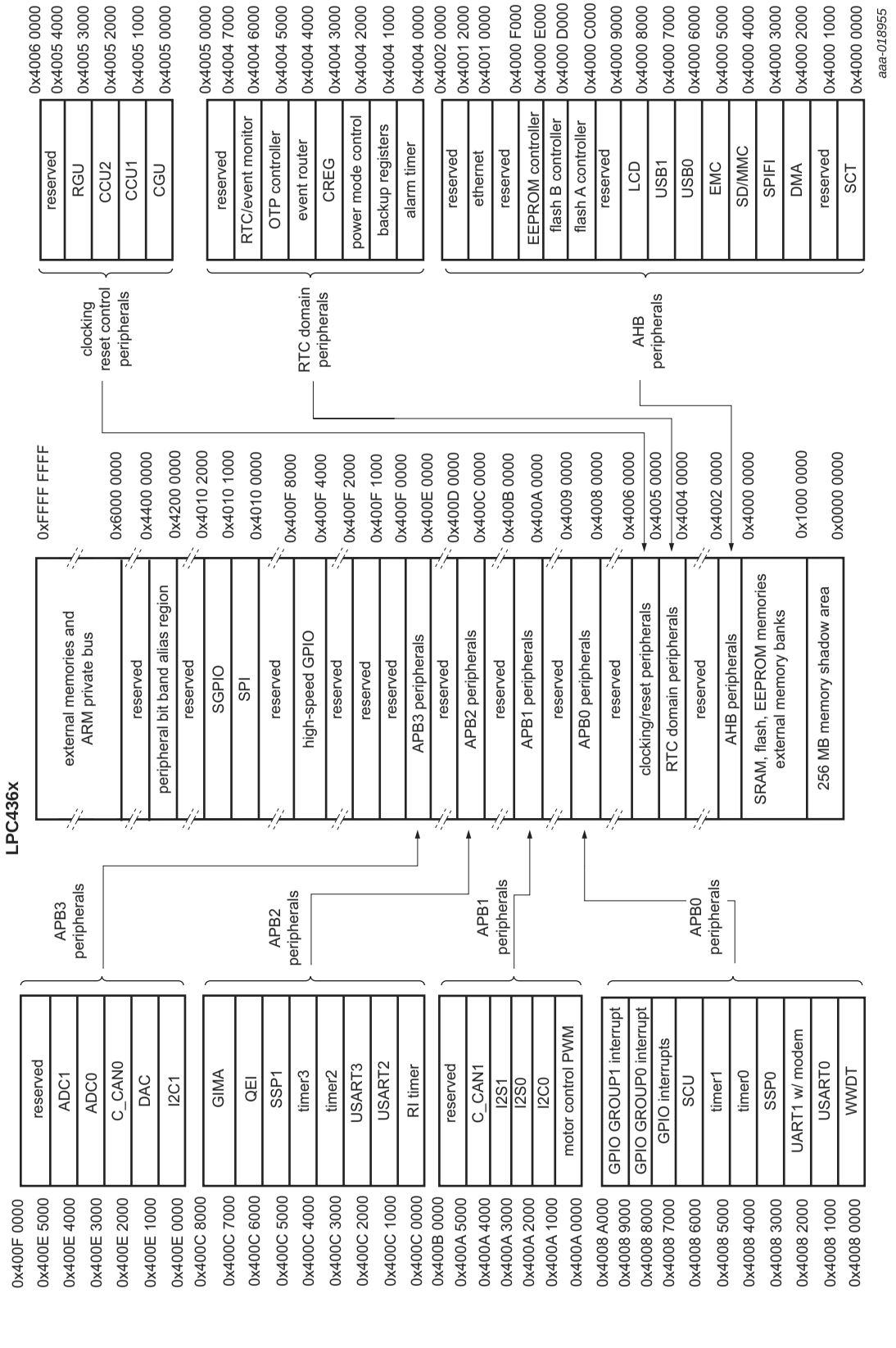


Fig 7. LPC436x Memory mapping (peripherals)

7.15 One-Time Programmable (OTP) memory

The OTP provides 64 bit+ 256 bit of memory for general-purpose use.

7.16 General Purpose I/O (GPIO)

The LPC436x provide eight GPIO ports with up to 31 GPIO pins each.

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

All GPIO pins default to inputs with pull-up resistors enabled and input buffer disabled on reset. The input buffer must be turned on in the system control block SFS register before the GPIO input can be read.

7.16.1 Features

- Accelerated GPIO functions:
  - GPIO registers are located on the AHB so that the fastest possible I/O timing can be achieved.
  - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
  - All GPIO registers are byte and half-word addressable.
  - Entire port value can be written in one instruction.
- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- Up to eight GPIO pins can be selected from all GPIO pins to create an edge- or level-sensitive GPIO interrupt request (GPIO interrupts).
- Two GPIO group interrupts can be triggered by any pin or pins in each port (GPIO group0 and group1 interrupts).

7.17 Configurable digital peripherals

7.17.1 SCTimer/PWM

The SCTimer/PWM allows a wide variety of timing, counting, output modulation, and input capture operations. The inputs and outputs of the SCTimer/PWM are shared with the capture and match inputs/outputs of the 32-bit general purpose counter/timers.

The SCTimer/PWM can be configured as two 16-bit counters or a unified 32-bit counter. In the two-counter case, in addition to the counter value the following operational elements are independent for each half:

- State variable.
- Limit, halt, stop, and start conditions.
- Values of Match/Capture registers, plus reload or capture control values.

7.18.5 High-speed USB Host/Device/OTG interface (USB0)

Remark: USB0 is available on the following parts: LPC435x, LPC433x, LPC432x. USB0 is not available on the LPC431x parts.

The USB OTG module allows the LPC436x to connect directly to a USB Host such as a PC (in device mode) or to a USB Device in host mode.

7.18.5.1 Features

- Contains UTMI+ compliant high-speed transceiver (PHY).
- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *USB On-The-Go supplement*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals.
- Supports all full-speed USB-compliant peripherals.
- Supports software Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for OTG peripherals.
- Supports interrupts.
- Supports Start Of Frame (SOF) frame length adjust.
- This module has its own, integrated DMA engine.
- USB interface electrical test software included in ROM USB stack.

7.18.6 High-speed USB Host/Device interface with ULPI (USB1)

Remark: USB1 is available on the following parts: LPC435x and LPC433x. USB1 is not available on the LPC432x and LPC431x parts.

The USB1 interface can operate as a full-speed USB Host/Device interface or can connect to an external ULPI PHY for High-speed operation.

7.18.6.1 Features

- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals if connected to external ULPI PHY.
- Supports all full-speed USB-compliant peripherals.
- Supports interrupts.
- Supports Start Of Frame (SOF) frame length adjust.
- This module has its own, integrated DMA engine.
- USB interface electrical test software included in ROM USB stack.

7.18.7 LCD controller

Remark: The LCD controller is only available on parts LPC435x. LCD is not available on parts LPC433x, LPC432x, and LPC431x.

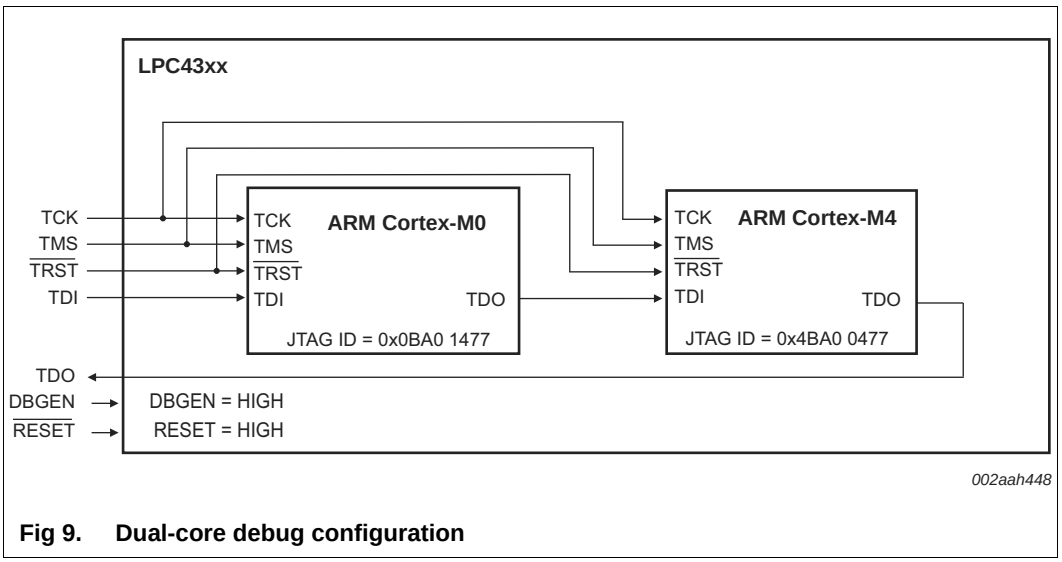
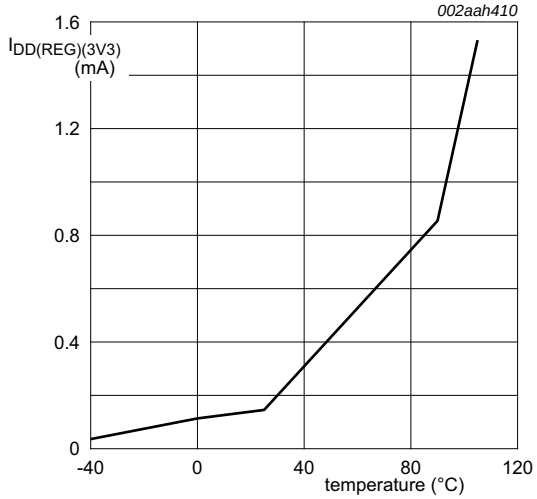
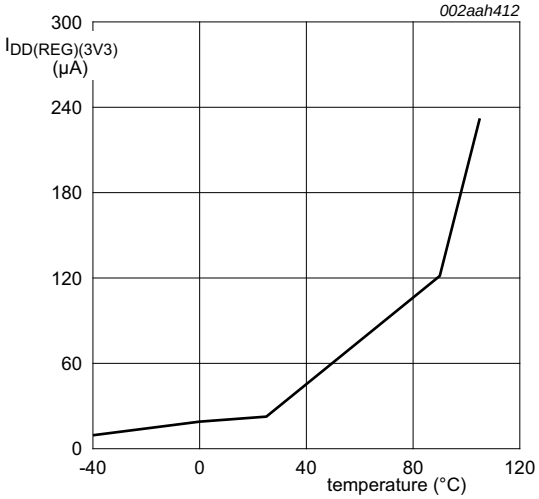


Fig 9. Dual-core debug configuration



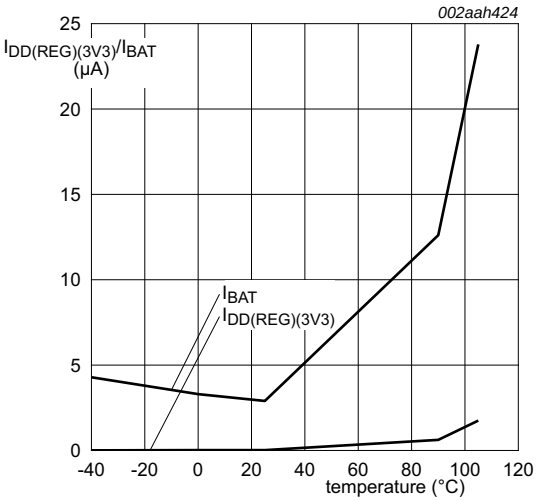
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V.

Fig 14. Typical supply current versus temperature in Deep-sleep mode



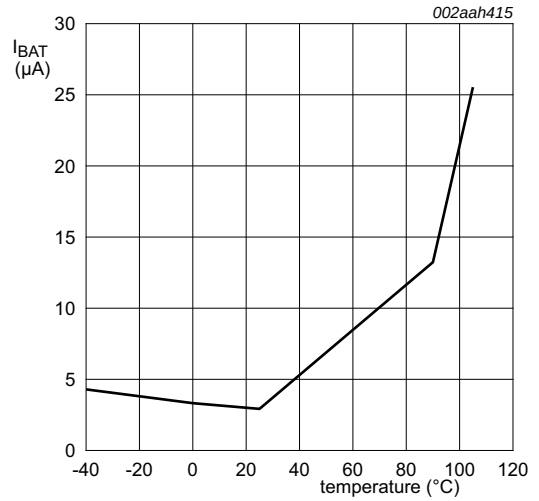
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V.

Fig 15. Typical supply current versus temperature in Power-down mode



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V. $V_{BAT} = V_{DD(REG)(3V3)} + 0.4$ V.

Fig 16. Typical supply current versus temperature in Deep power-down mode



Conditions: $V_{BAT} = 3.6$ V. $V_{DD(REG)(3V3)}$ not present.

Fig 17. Typical battery supply current versus temperature

Table 12. Peripheral power consumption

Peripheral	Branch clock	$I_{DD(REG)(3V3)}$ in mA	
		Branch clock frequency = 48 MHz	Branch clock frequency = 96 MHz
SPIFI	CLK_SPIFI, CLK_M4_SPIFI	1.14	2.29
GPIO	CLK_M4_GPIO	0.72	1.43
LCD	CLK_M4_LCD	0.91	1.82
ETHERNET	CLK_M4_ETHERNET	1.06	2.15
UART0	CLK_M4_UART0, CLK_APB0_UART0	0.24	0.43
UART1	CLK_M4_UART1, CLK_APB0_UART1	0.24	0.43
UART2	CLK_M4_UART2, CLK_APB2_UART2	0.26	0.5
UART3	CLK_M4_USART3, CLK_APB2_UART3	0.27	0.45
TIMER0	CLK_M4_TIMER0	0.08	0.15
TIMER1	CLK_M4_TIMER1	0.09	0.15
TIMER2	CLK_M4_TIMER2	0.1	0.19
TIMER3	CLK_M4_TIMER3	0.08	0.16
SDIO	CLK_M4_SDIO, CLK_SDIO	0.66	1.17
SCTimer/PWM	CLK_M4_SCT	0.66	1.3
SSP0	CLK_M4_SSP0, CLK_APB0_SSP0	0.13	0.23
SSP1	CLK_M4_SSP1, CLK_APB2_SSP1	0.14	0.27
DMA	CLK_M4_DMA	1.81	3.61
WWDT	CLK_M4_WWDT	0.03	0.09
QEI	CLK_M4_QEI	0.28	0.55
USB0	CLK_M4_USB0, CLK_USB0	1.9	3.9
USB1	CLK_M4_USB1, CLK_USB1	3.02	5.69
RITIMER	CLK_M4_RITIMER	0.05	0.1
EMC	CLK_M4_EMC, CLK_M4_EMC_DIV	3.94	7.95
SCU	CLK_M4_SCU	0.1	0.21
CREG	CLK_M4_CREG	0.35	0.7
Flash bank A	CLK_M4_FLASHA	1.47	2.97
Flash bank B	CLK_M4_FLASHB	1.4	2.84
SGPIO	CLK_PERIPH_SGPIO	0.1	0.17
SPI	CLK_SPI	0.07	0.11

11.4 Crystal oscillator

Table 19. Dynamic characteristic: oscillator

T_{amb} = −40 °C to +105 °C; $V_{DD(IO)}$ over specified ranges; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
Low-frequency mode (1-20 MHz)[5]							
$t_{jit(per)}$	period jitter time	5 MHz crystal	[3][4]	-	13.2	-	ps
		10 MHz crystal		-	6.6	-	ps
		15 MHz crystal		-	4.8	-	ps
High-frequency mode (20 - 25 MHz)[6]							
$t_{jit(per)}$	period jitter time	20 MHz crystal	[3][4]	-	4.3	-	ps
		25 MHz crystal		-	3.7	-	ps

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Indicates RMS period jitter.

[4] PLL-induced jitter is not included.

[5] Select HF = 0 in the XTAL_OSC_CTRL register.

[6] Select HF = 1 in the XTAL_OSC_CTRL register.

11.5 IRC oscillator

Table 20. Dynamic characteristic: IRC oscillator

2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-40 °C ≤ T_{amb} < 0 °C	12.0 - 3 %	12.0	12.0 + 3 %	MHz
		0 °C ≤ T_{amb} ≤ 85 °C	12.0 - 1.5 %	12.0	12.0 + 1.5 %	MHz
		85 °C < T_{amb} < 105 °C	12.0 - 3 %	12.0	12.0 + 3 %	MHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.6 RTC oscillator

See Section 13.3 for connecting the RTC oscillator to an external clock source.

Table 21. Dynamic characteristic: RTC oscillator

T_{amb} = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V or 2.4 V ≤ V_{BAT} ≤ 3.6 V[1]

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_i	input frequency	-		-	32.768	-	kHz
$I_{CC(osc)}$	oscillator supply current				280	800	nA

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.12 SSP interface

Table 27. Dynamic characteristics: SSP pins in SPI mode

T_{amb} = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF; sampled at 10 % and 90 % of the signal level; EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SSP master							
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	$1/(25.5 \times 10^6)$	-	-	s
		when only transmitting		$1/(51 \times 10^6)$	-	-	s
t_{DS}	data set-up time	in SPI mode		12.2	-	-	ns
t_{DH}	data hold time	in SPI mode		−3.6	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode		-	-	6.7	ns
$t_{h(Q)}$	data output hold time	in SPI mode		−1.7	-	-	ns
t_{lead}	lead time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		$T_{cy(clk)}$ + 3.3	-	$T_{cy(clk)}$ + 8.2	ns
		SPI mode; CPOL = 0; CPHA = 1		$0.5 \times T_{cy(clk)}$ + 3.3	-	$0.5 \times T_{cy(clk)}$ + 8.2	ns
		SPI mode; CPOL = 1; CPHA = 0		$T_{cy(clk)}$ + 3.3	-	$T_{cy(clk)}$ + 8.2	ns
		SPI mode; CPOL = 1; CPHA = 1		$0.5 \times T_{cy(clk)}$ + 3.3	-	$0.5 \times T_{cy(clk)}$ + 8.2	ns
		synchronous serial frame mode		$0.5 \times T_{cy(clk)}$ + 3.3	-	$0.5 \times T_{cy(clk)}$ + 8.2	ns
		microwire frame format		$T_{cy(clk)}$ + 3.3	-	$T_{cy(clk)}$ + 8.2	ns
t_{lag}	lag time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		$0.5 \times T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 0; CPHA = 1		$T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 1; CPHA = 0		$0.5 \times T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 1; CPHA = 1		$T_{cy(clk)}$	-	-	ns
		synchronous serial frame mode		$T_{cy(clk)}$	-	-	ns
		microwire frame format		$0.5 \times T_{cy(clk)}$	-	-	ns

Table 35. Static characteristics: USB0 PHY pins[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
High-speed mode							
P_{cons}	power consumption		[2]	-	68	-	mW
$I_{DDA(3V3)}$	analog supply current (3.3 V)	on pin USB0_VDDA3V3_DRIVER; total supply current	[3]	-	18	-	mA
		during transmit		-	31	-	mA
		during receive		-	14	-	mA
		with driver tri-stated		-	14	-	mA
I_{DDD}	digital supply current			-	7	-	mA
Full-speed/low-speed mode							
P_{cons}	power consumption		[2]	-	15	-	mW
$I_{DDA(3V3)}$	analog supply current (3.3 V)	on pin USB0_VDDA3V3_DRIVER; total supply current		-	3.5	-	mA
		during transmit		-	5	-	mA
		during receive		-	3	-	mA
		with driver tri-stated		-	3	-	mA
I_{DDD}	digital supply current			-	3	-	mA
Suspend mode							
$I_{DDA(3V3)}$	analog supply current (3.3 V)			-	24	-	μA
		with driver tri-stated		-	24	-	μA
		with OTG functionality enabled		-	3	-	mA
I_{DDD}	digital supply current			-	30	-	μA
VBUS detector outputs							
V_{th}	threshold voltage	for VBUS valid		4.4	-	-	V
		for session end		0.2	-	0.8	V
		for A valid		0.8	-	2	V
		for B valid		2	-	4	V
V_{hys}	hysteresis voltage	for session end		-	150	10	mV
		A valid		-	200	10	mV
		B valid		-	200	10	mV

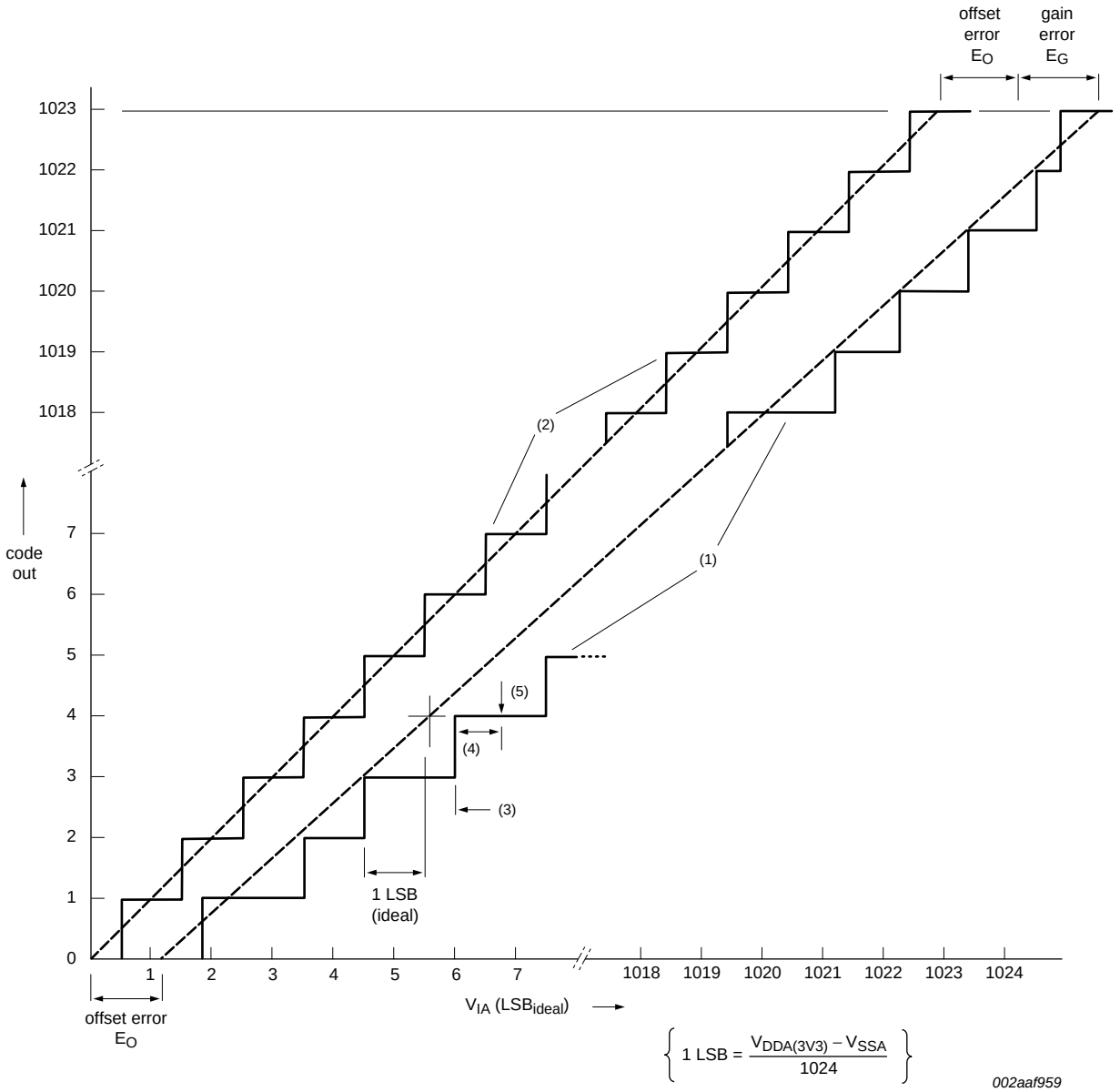
[1] Characterized but not implemented as production test.

[2] Total average power consumption.

[3] The driver is active only 20 % of the time.

11.19 Ethernet

Remark: The timing characteristics of the ENET_MDC and ENET_MDIO signals comply with the *IEEE standard 802.3*.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 40. 10-bit ADC characteristics

18. Revision history

Table 47. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC436x v.1.2	20160314	Product data sheet	-	LPC436x v.1.1
	• Updated Table 32 “Dynamic characteristics: Dynamic external memory interface”: Read cycle parameters $t_{h(D)}$ min value is 2.2 ns and max value is “-”. • Fixed the number of ADC channels for LPC4367JET100 in Table 2 “Ordering options” to 4.			
LPC436x v.1.1	20151111	Product data sheet	2015110041	LPC436x v.1.0
Modifications:	• Added CIN number, 2015110041 for SSP timing value changes in the change notice column of the Revision history table. • Updated Table 27 “Dynamic characteristics: SSP pins in SPI mode”: – changed units of $T_{cy(clk)}$, clock cycle time, SSP slave and master from ns to s. – removed $t_{v(Q)}$, data output valid time in SPI mode, minimum value of 3 ´ (1/PCLK) from SSP slave mode. – added units to t_d, delay time, for SSP slave and master mode.			
LPC436x v.1.0	20151105	Product data sheet	-	-

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