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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l031c6t7

The Cortex-M0+ processor closely integrates a configurable Nested Vectored Interrupt Controller (NVIC), to deliver industry-leading interrupt performance. The NVIC:

- includes a Non-Maskable Interrupt (NMI)
- provides zero jitter interrupt option
- provides four interrupt priority levels

The tight integration of the processor core and NVIC provides fast execution of Interrupt Service Routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to abandon and restart load-multiple and store-multiple operations. Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that include a deep sleep function that enables the entire device to enter rapidly stop or standby mode.

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.4 Reset and supply management

3.4.1 Power supply schemes

- V_{DD} = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

3.4.2 Power supply supervisor

The devices feature an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

Two versions are available:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the VDD min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

3.12 Ultra-low-power comparators and reference voltage

The STM32L031x4/6 embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with ultra low consumption
- One comparator with rail-to-rail inputs, fast or slow mode.
- The threshold can be one of the following:
  – External I/O pins
  – Internal reference voltage (V_{REFINT})
  – submultiple of Internal reference voltage(1/4, 1/2, 3/4) for the rail to rail comparator.

Both comparators can wake up the devices from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

3.13 System configuration controller

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM21, TIM22 and LPTIM timer input captures. It also controls the routing of internal analog signals to the ADC, COMP1 and COMP2 and the internal reference voltage V_{REFINT}.

3.14 Timers and watchdogs

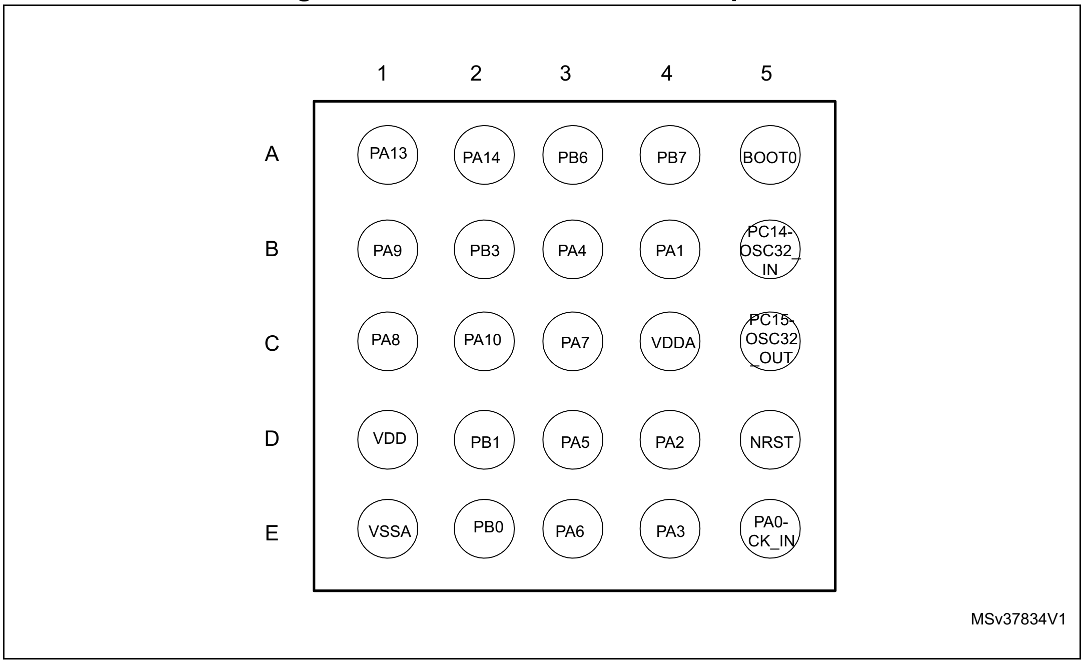
The ultra-low-power STM32L031x4/6 devices include three general-purpose timers, one low- power timer (LPTM), two watchdog timers and the SysTick timer.

Table 9 compares the features of the general-purpose and basic timers.

Table 9. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM21, TIM22	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No

Figure 9. STM32L031x4/6 WLCSP25 pinout



1. The above figure shows the package top view.

Table 14. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 15. Pin definitions (continued)

Pin Number							Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
TSSOP20	WLCSP25[(1)]	UFQFPN28	UFQFPN28 (STM32L031GxUxS only)	LQFP32	UFQFPN32[(2)]	LQFP48						
7	B4	7	7	7	7	11	PA1	I/O	FT	-	EVENTOUT, LPTIM1_IN2, TIM2_CH2, I2C1_SMBA, USART2_RTS, TIM21_ETR	COMP1_INP, ADC_IN1
8	D4	8	8	8	8	12	PA2	I/O	TC	-	TIM21_CH1, TIM2_CH3, USART2_TX, LPUART1_TX, COMP2_OUT	COMP2_INM6, ADC_IN2, RTC_TAMP3/RTC_TS/ RTC_OUT/WKUP3
9	E4	9	9	9	9	13	PA3	I/O	FT	-	TIM21_CH2, TIM2_CH4, USART2_RX, LPUART1_RX	COMP2_INP, ADC_IN3
10	B3	10	10	10	10	14	PA4	I/O	TC	-	SPI1_NSS, LPTIM1_IN1, USART2_CK, TIM22_ETR	COMP1_INM4, COMP2_INM4, ADC_IN4
11	D3	11	11	11	11	15	PA5	I/O	TC	-	SPI1_SCK, LPTIM1_IN2, TIM2_ETR, TIM2_CH1	COMP1_INM5, COMP2_INM5, ADC_IN5
12	E3	12	12	12	12	16	PA6	I/O	FT	-	SPI1_MISO, LPTIM1_ETR, LPUART1_CTS, TIM22_CH1, EVENTOUT, COMP1_OUT	ADC_IN6

Table 15. Pin definitions (continued)

Pin Number							Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
TSSOP20	WLCSP25[1]	UFQFPN28	UFQFPN28 (STM32L031GxUxS only)	LQFP32	UFQFPN32[2]	LQFP48						
-	-	-	-	-	-	27	PB14	I/O	FT	-	SPI1_MISO, RTC_OUT, TIM21_CH2, LPUART1_RTS	-
-	-	-	-	-	-	28	PB15	I/O	FT	-	SPI1_MOSI, RTC_REFIN	-
-	C1	18	18	18	18	29	PA8	I/O	FT	-	MCO, LPTIM1_IN1, EVENTOUT, USART2_CK, TIM2_CH1	-
17	B1	19	19	19	19	30	PA9	I/O	FTf	-	MCO, I2C1_SCL, USART2_TX, TIM22_CH1	-
18	C2	20	20	20	20	31	PA10	I/O	FTf	-	I2C1_SDA, USART2_RX, TIM22_CH2	-
-	-	-	-	21	21	32	PA11	I/O	FT	-	SPI1_MISO, EVENTOUT, USART2_CTS, TIM21_CH2, COMP1_OUT	-
-	-	-	-	22	22	33	PA12	I/O	FT	-	SPI1_MOSI, EVENTOUT, USART2_RTS, COMP2_OUT	-
19	A1	21	21	23	23	34	PA13	I/O	FT	-	SWDIO, LPTIM1_ETR, LPUART1_RX	-

Table 15. Pin definitions (continued)

Pin Number							Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
TSSOP20	WLCSP25[1]	UFQFPN28	UFQFPN28 (STM32L031GxUxS only)	LQFP32	UFQFPN32[2]	LQFP48						
-	-	-	-	-	-	35	VSS	S	-	-	-	-
-	D1	-	-	-	-	36	VDD	S	-	-	-	-
20	A2	22	22	24	24	37	PA14	I/O	FT	-	SWCLK, LPTIM1_OUT, I2C1_SMBA, USART2_TX, LPUART1_TX	-
-	-	23	23	25	25	38	PA15	I/O	FT	-	SPI1_NSS, TIM2_ETR, EVENTOUT, USART2_RX, TIM2_CH1	--
-	B2	24	24	26	26	39	PB3	I/O	FT	-	SPI1_SCK, TIM2_CH2, EVENTOUT	COMP2_INN
-	-	-	25	27	27	40	PB4	I/O	FT	-	SPI1_MISO, EVENTOUT, TIM22_CH1	COMP2_INP
-	-	-	26	28	28	41	PB5	I/O	FT	-	SPI1_MOSI, LPTIM1_IN1, I2C1_SMBA, TIM22_CH2	COMP2_INP
-	A3	25	27	29	29	42	PB6	I/O	FTf	-	USART2_TX, I2C1_SCL, LPTIM1_ETR, TIM21_CH1	COMP2_INP
-	A4	26	28	30	30	43	PB7	I/O	FTf	-	USART2_RX, I2C1_SDA, LPTIM1_IN2	COMP2_INP, VREF_PVD_IN

Table 16. Alternate functions

Ports		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/USART2 /LPTIM/TIM21 /EVENTOUT/ SYS_AF	SPI1/I2C1/ LPTIM	LPTIM/TIM2/ EVENTOUT/ SYS_AF	I2C1/ EVENTOUT	I2C1/USART2/ LPUART1/ TIM22/ EVENTOUT	TIM2/21/22	LPUART1/ EVENTOUT	COMP1/2
Port A	PA0	-	LPTIM1_IN1	TIM2_CH1	-	USART2_CTS	TIM2_ETR	-	COMP1_OUT
	PA1	EVENTOUT	LPTIM1_IN2	TIM2_CH2	I2C1_SMBA	USART2_RTS	TIM21_ETR	-	-
	PA2	TIM21_CH1	-	TIM2_CH3	-	USART2_TX	-	LPUART1_TX	COMP2_OUT
	PA3	TIM21_CH2	-	TIM2_CH4	-	USART2_RX	-	LPUART1_RX	
	PA4	SPI1_NSS	LPTIM1_IN1	-	-	USART2_CK	TIM22_ETR	-	-
	PA5	SPI1_SCK	LPTIM1_IN2	TIM2_ETR	-	-	TIM2_CH1	-	-
	PA6	SPI1_MISO	LPTIM1_ETR	-	-	LPUART1_CTS	TIM22_CH1	EVENTOUT	COMP1_OUT
	PA7	SPI1_MOSI	LPTIM1_OUT	-	-	USART2_CTS	TIM22_CH2	EVENTOUT	COMP2_OUT
	PA8	MCO	-	LPTIM1_IN1	EVENTOUT	USART2_CK	TIM2_CH1	-	-
	PA9	MCO	I2C1_SCL	-	-	USART2_TX	TIM22_CH1	-	-
	PA10	-	I2C1_SDA	-	-	USART2_RX	TIM22_CH2	-	-
	PA11	SPI1_MISO	-	EVENTOUT	-	USART2_CTS	TIM21_CH2	-	COMP1_OUT
	PA12	SPI1_MOSI	-	EVENTOUT	-	USART2_RTS	-	-	COMP2_OUT
	PA13	SWDIO	LPTIM1_ETR	-	-	-	-	LPUART1_RX	-
	PA14	SWCLK	LPTIM1_OUT	-	I2C1_SMBA	USART2_TX	-	LPUART1_TX	-
	PA15	SPI1_NSS	-	TIM2_ETR	EVENTOUT	USART2_RX	TIM2_CH1	-	-

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 14: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code if not specified otherwise.

The current consumption values are derived from the tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20: General operating conditions* unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time and prefetch is adjusted depending on fHCLK frequency and voltage range to provide the best CPU performance unless otherwise specified.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{APB}$
- When PLL is on, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used)
- The HSE user clock is applied to OSCI_IN input (LQFP48 package) and to CK_IN (other packages). It follows the characteristic specified in *Table 37: High-speed external user clock characteristics*
- For maximum current consumption $V_{DD} = V_{DDA} = 3.6$ V is applied to all supply pins
- For typical current consumption $V_{DD} = V_{DDA} = 3.0$ V is applied to all supply pins if not specified otherwise

The parameters given in *Table 44*, *Table 20* and *Table 21* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20*.

Table 24. Current consumption in Run mode, code with data processing running from Flash memory

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Run from Flash)	Supply current in Run mode, code executed from Flash	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = $f_{HCLK}/2$ above 16 MHz (PLL on)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0]=11	1 MHz	140	200	µA
				2 MHz	245	310	
				4 MHz	460	540	
			Range 2, V_{CORE}=1.5 V, VOS[1:0]=10,	4 MHz	0.56	0.63	mA
				8 MHz	1.1	1.2	
				16 MHz	2.1	2.3	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	8 MHz	1.25	1.4	
				16 MHz	2.5	2.7	
				32 MHz	5	5.6	
		HSI clock	Range 2, V_{CORE}=1.5 V, VOS[1:0]=10,	16 MHz	2.1	2.4	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	32 MHz	5.1	5.7	
		MSI clock	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	65 kHz	34.5	110	µA
				524 kHz	86	150	
				4.2 MHz	505	570	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 25. Current consumption in Run mode vs code type, code with data processing running from Flash memory

Symbol	Parameter	Conditions			f_{HCLK}	Typ	Unit
I_{DD} (Run from Flash)	Supply current in Run mode, code executed from Flash memory	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = $f_{HCLK}/2$ above 16 MHz (PLL ON)(1)	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	Dhrystone	4 MHz	460	µA
				CoreMark		455	
				Fibonacci		330	
				while(1)		305	
				while(1), prefetch OFF		320	
			Range 1, VOS[1:0]=01, V_{CORE}=1.8 V	Dhrystone	32 MHz	5	mA
				CoreMark		5.15	
				Fibonacci		5	
				while(1)		4.35	
				while(1), prefetch OFF		3.85	

1. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 28. Current consumption in Sleep mode

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Sleep)	Supply current in Sleep mode, Flash memory OFF	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = $f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	1 MHz	36.5	87	µA
				2 MHz	58	100	
				4 MHz	100	170	
			Range 2, V_{CORE}=1.5 V, VOS[1:0]=10	4 MHz	125	190	
				8 MHz	230	310	
				16 MHz	450	540	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	8 MHz	275	360	
				16 MHz	555	650	
				32 MHz	1350	1600	
		HSI16 clock source (16 MHz)	Range 2, V_{CORE}=1.5 V, VOS[1:0]=10	16 MHz	585	690	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	32 MHz	1500	1700	
		MSI clock	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	65 kHz	17	43	
				524 kHz	28	55	
				4.2 MHz	115	190	
	Supply current in Sleep mode, Flash memory ON	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = $f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	1 MHz	49	160	
				2 MHz	69	190	
				4 MHz	115	230	
			Range 2, $_{CORE}$=1.5 V, VOS[1:0]=10	4 MHz	135	200	
				8 MHz	240	320	
				16 MHz	460	550	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	8 MHz	290	370	
				16 MHz	565	670	
				32 MHz	1350	1600	
		HSI16 clock source (16 MHz)	Range 2, V_{CORE}=1.5 V, VOS[1:0]=10	16 MHz	600	700	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	32 MHz	1500	1700	
		MSI clock	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	65 kHz	28	55	
				524 kHz	39.5	67	
				4.2 MHz	125	200	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

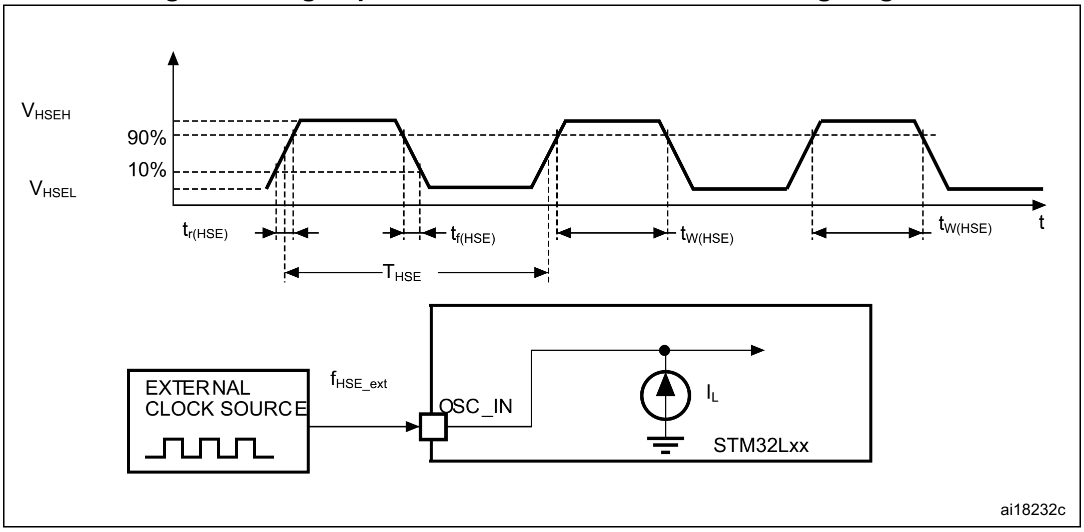
In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.The external clock signal has to respect the I/O characteristics in *Section 6.3.12*. However, the recommended clock input waveform is shown in *Figure 20*.

Table 37. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is on or PLL is used	1	8	32	MHz
		CSS is off, PLL not used	0	8	32	MHz
V_{HSEH}	OSC_IN/CK_IN(2) input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN/CK_IN(2) input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN/CK_IN(2) high or low time	-	12	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN/CK_IN(2) rise or fall time		-	-	20	
$C_{in(HSE)}$	OSC_IN/CK_IN(2) input capacitance		-	2.6	-	pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	OSC_IN/CK_IN(2) Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.
2. HSE external user clock is applied to OSC_IN on LQFP48 package and to CK_IN on other packages.

Figure 20. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 20*.

Table 38. Low-speed external user clock characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency		1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time		465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Figure 21. Low-speed external clock source AC timing diagram

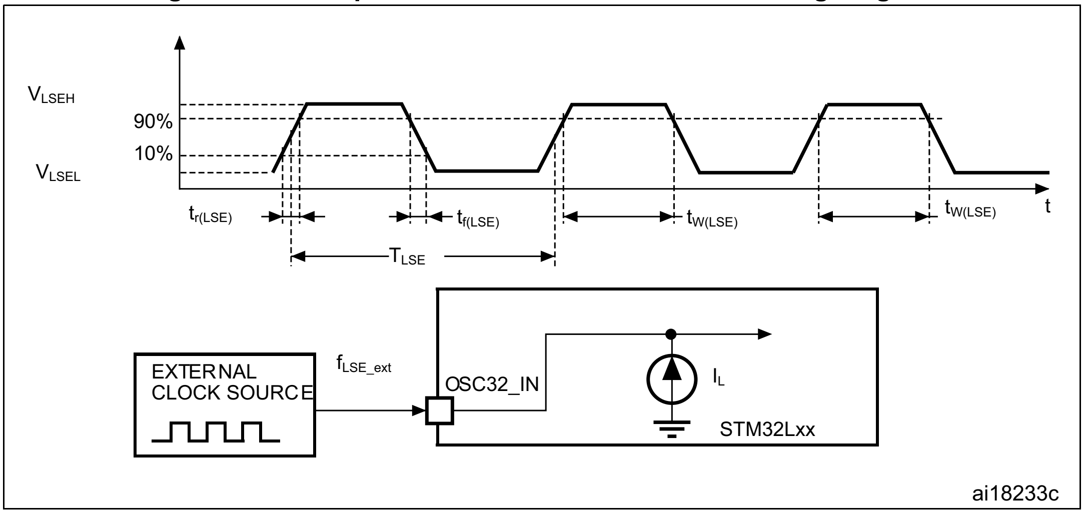
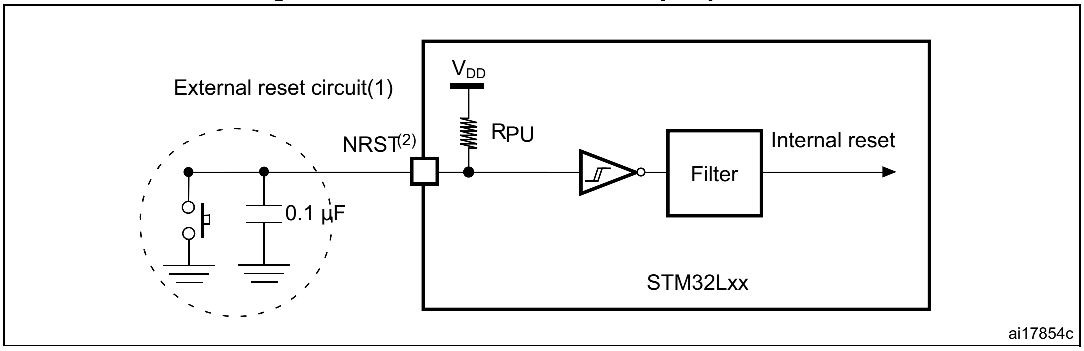


Figure 28. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 56*. Otherwise the reset will not be taken into account by the device.

6.3.15 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 57* are values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 20: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 57. ADC characteristics

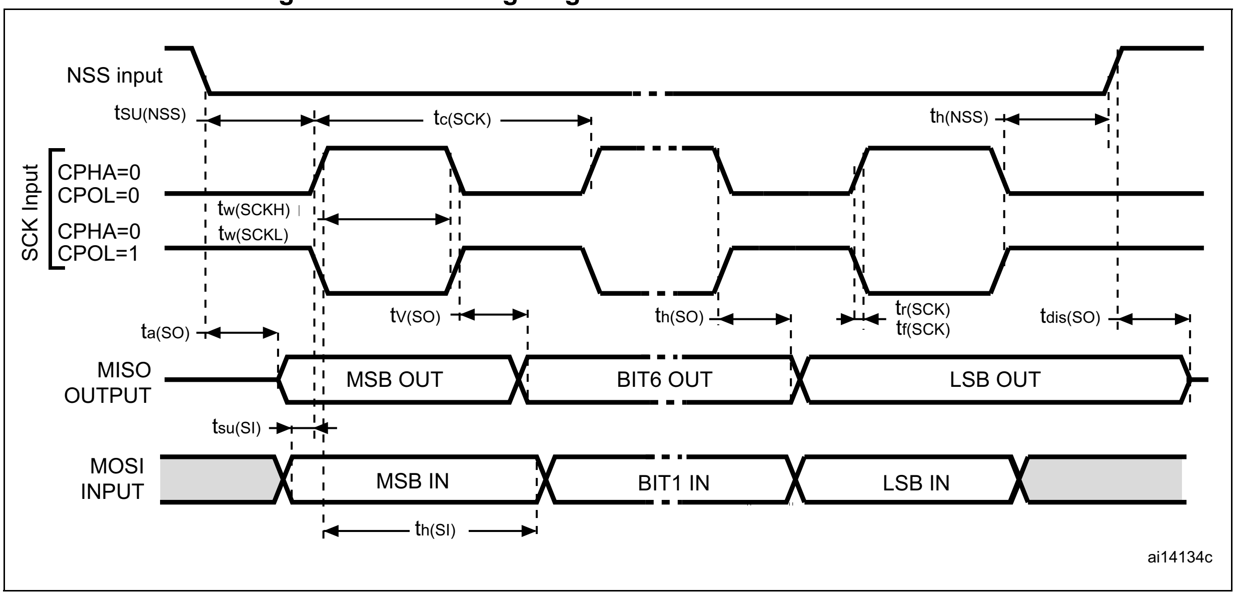
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC on	Fast channel	1.65	-	3.6	V
		Standard channel	1.75(1)	-	3.6	
$I_{DDA (ADC)}$	Current consumption of the ADC on V_{DDA}	1.14 Msps	-	200	-	µA
		10 ksps	-	40	-	
	Current consumption of the ADC on V_{DD}(2)	1.14 Msps	-	70	-	
		10 ksps	-	1	-	
f_{ADC}	ADC clock frequency	Voltage scaling Range 1	0.14	-	16	MHz
		Voltage scaling Range 2	0.14	-	8	
		Voltage scaling Range 3	0.14	-	4	
f_S(3)	Sampling rate		0.05	-	1.14	MHz
f_{TRIG}(3)	External trigger frequency	f_{ADC} = 16 MHz	-	-	941	kHz
			-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range		0	-	V_{DDA}	V
R_{AIN}(3)	External input impedance	See *Equation 1* and *Table 58* for details	-	-	50	kΩ
R_{ADC}(3)(4)	Sampling switch resistance		-	-	1	kΩ
C_{ADC}(3)	Internal sample and hold capacitor		-	-	8	pF

Table 69. SPI characteristics in voltage Range 3 [(1)]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	2	MHz
		Slave mode			2[(2)]	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	28.5	-	-	
$t_{su(SI)}$		Slave mode	22	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	7	-	-	
$t_{h(SI)}$		Slave mode	5	-	-	
$t_{a(SO}$	Data output access time	Slave mode	30	-	70	
$t_{dis(SO)}$	Data output disable time	Slave mode	40	-	80	
$t_{v(SO)}$	Data output valid time	Slave mode	-	53	86	
		Master mode	-	30	54	
$t_{v(MO)}$	Data output hold time	Slave mode	18	-	-	
$t_{h(SO)}$		Master mode	8	-	-	

1. Guaranteed by characterization results.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

Figure 31. SPI timing diagram - slave mode and CPHA = 0

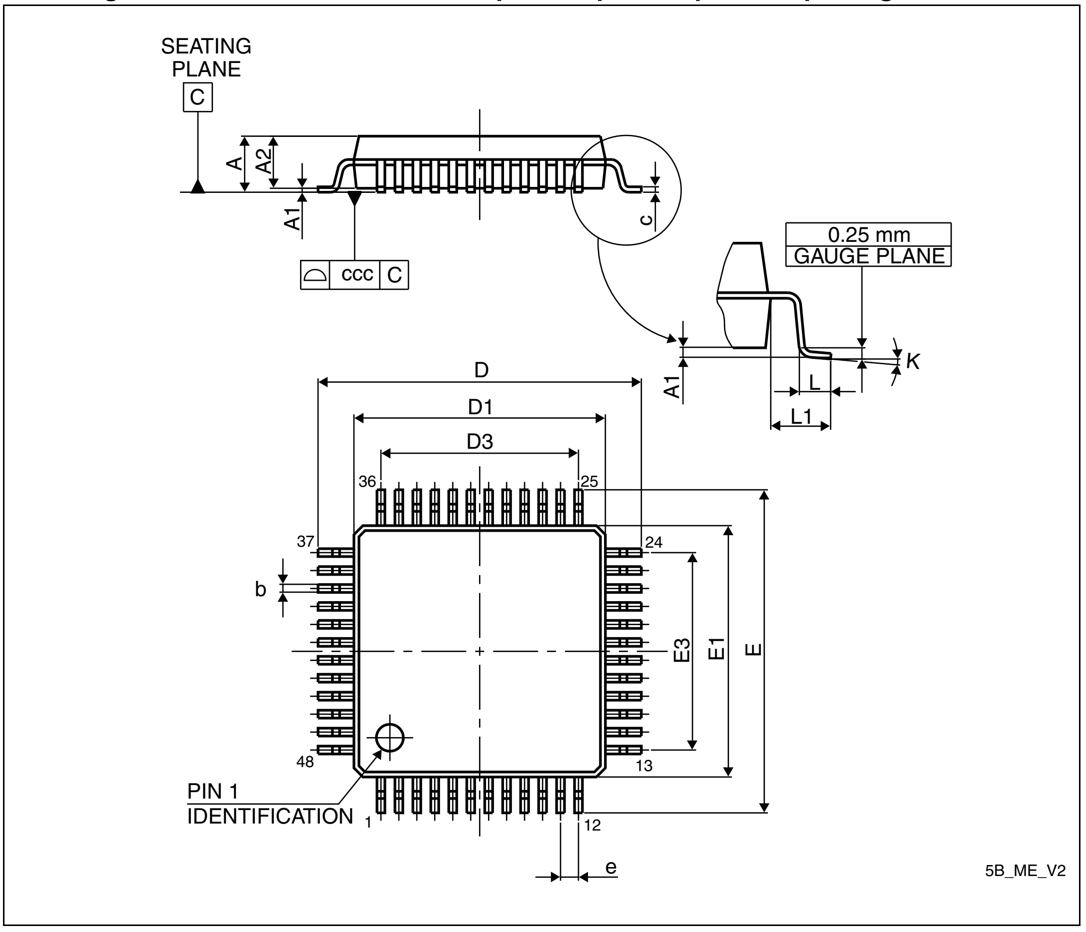


7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status *are available at http://www.st.com.* ECOPACK® is an ST trademark.

7.1 LQFP48 package information

Figure 34. LQFP48, 7 x 7 mm, 48-pin low-profile quad flat package outline



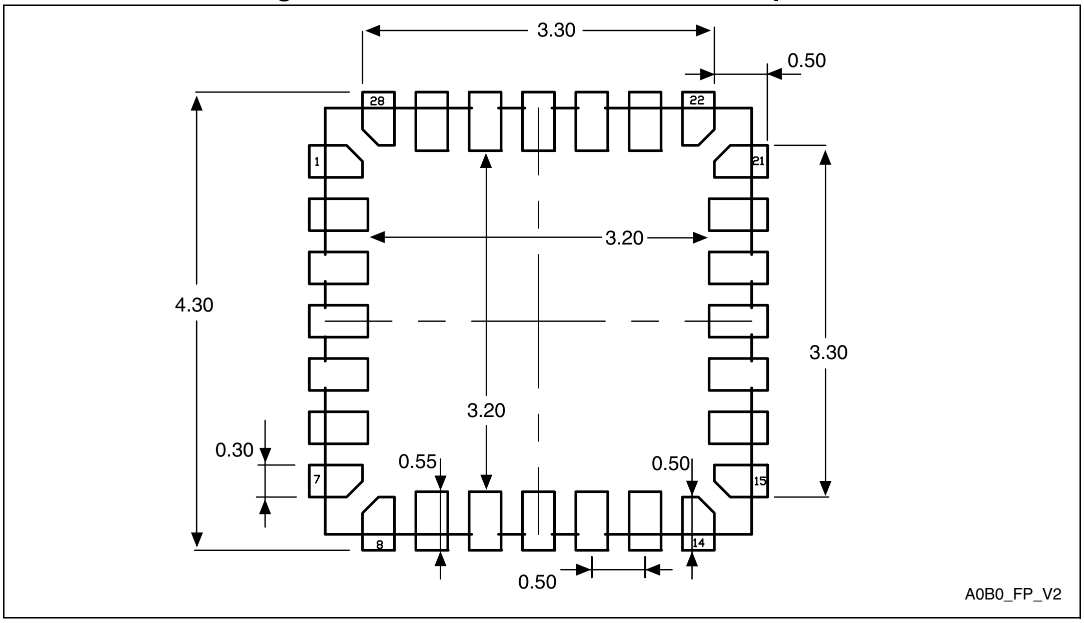
1. Drawing is not to scale.

Table 70. LQFP48 - 48-pin low-profile quad flat package, 7 x 7 mm, package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 44. UFQFPN28 recommended footprint

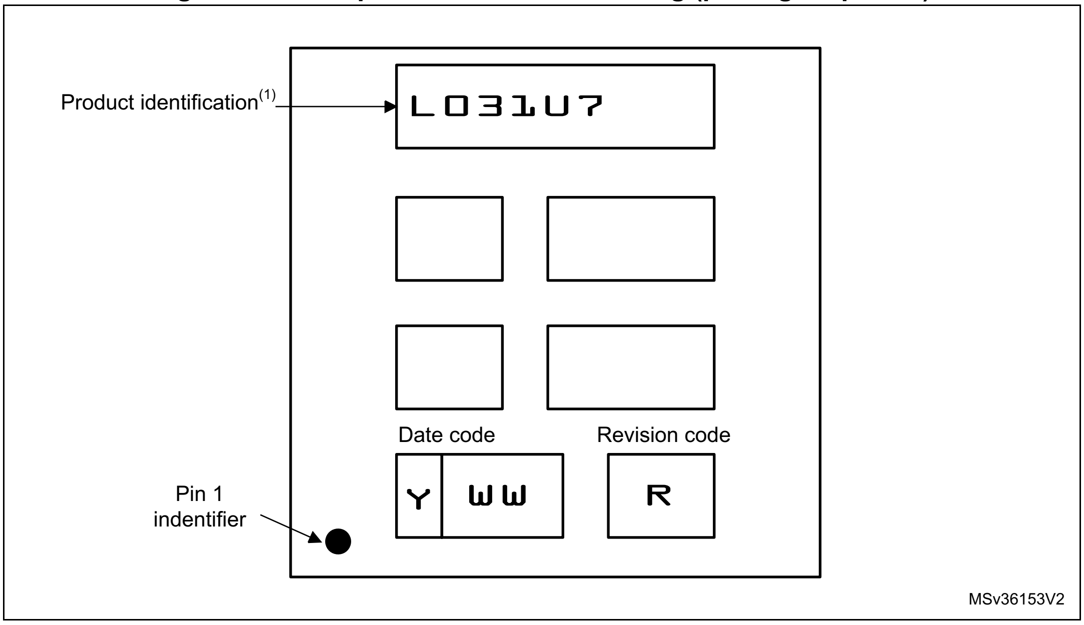


1. Dimensions are expressed in millimeters.

UFQFPN28 device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

Figure 45. Example of UFQFPN28 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 74. WLCSP25 - 2.097 x 2.493 mm, 0.400 mm pitch wafer level chip scale mechanical data

Symbol	Milimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
aaa	0.1000	-	-	0.0039	-	-
bbb	0.1000	-	-	0.0039	-	-
ccc	0.1000	-	-	0.0039	-	-
ddd	0.0500	-	-	0.0020	-	-
eee	0.0500	-	-	0.0020	-	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 47. WLCSP25 - 2.097 x 2.493 mm, 0.400 mm pitch wafer level chip scale recommended footprint

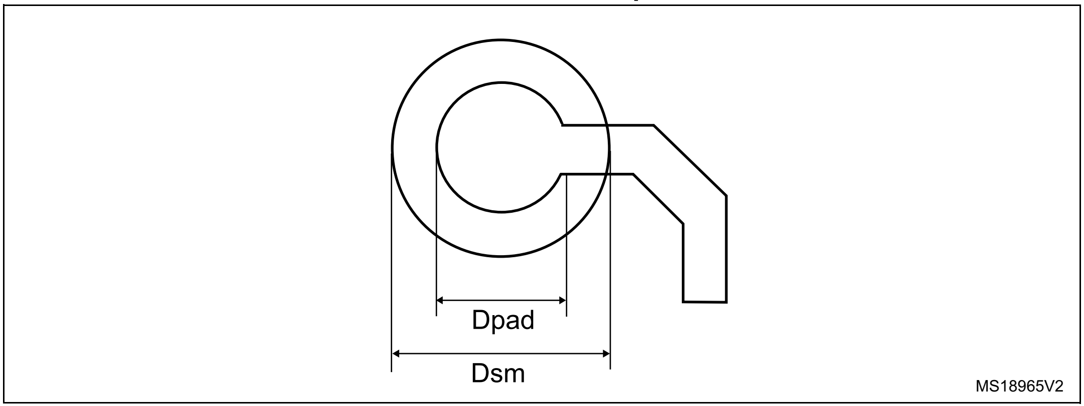


Table 75. WLCSP25 recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
Dpad	260 µm max. (circular) 220 µm recommended
Dsm	300 µm min. (for 260 µm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed

7.7 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max × Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 77. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP48 - 7 x 7 mm / 0.5 mm pitch	57	°C/W
	Thermal resistance junction-ambient LQFP32 - 7 x 7 mm / 0.8 mm pitch	60	
	Thermal resistance junction-ambient UFQFPN32 - 5 x 5 mm / 0.5 mm pitch	39	
	Thermal resistance junction-ambient UFQFPN28 - 4 x 4 mm / 0.5 mm pitch	120	
	Thermal resistance junction-ambient WLCSP25 - 0.4 mm pitch	70	
	Thermal resistance junction-ambient TSSOP20 - 169 mils	60	