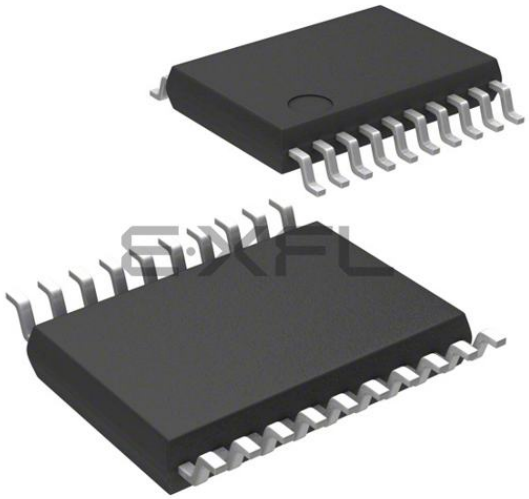

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 15 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 10x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-TSSOP (0.173", 4.40mm Width) |
| Supplier Device Package | 20-TSSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l031f4p3 |

**Table 2. Ultra-low-power STM32L031x4/x6 device features and peripheral counts (continued)**

| Peripheral | STM32 L031F4 | STM32 L031E4 | STM32 L031G4 | STM32 L031K4 | STM32 L031C4 | STM32 L031F6 | STM32 L031E6 | STM32 L031G6 | STM32 L031K6 | STM32 L031C6 |
|---|---|---|---|---|---|---|---|---|---|---|
| **Operating temperatures** | Ambient temperature: –40 to +125 °C<br>Junction temperature: –40 to +130 °C | | | | | | | | | |
| **Packages** | TSSOP 20 | WLCSP 25 | UFQFPN 28 | LQFP32, UFQFPN 32 | LQFP48 | TSSOP 20 | WLCSP 25 | UFQFPN 28 | LQFP32, UFQFPN 32 | LQFP48 |

1. 1 SPI interface is a USART operating in SPI master mode.
2. LQFP32 has two GPIOs, less than UFQFPN32 (27).
3. 23 GPIOs are available only on STM32L031GxUxS part number.
4. HSE external quartz connexion available only on LQFP48.

**Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)(1)**

| IPs | Run/Active | Sleep | Low-power run | Low-power sleep | Stop | | Standby | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Wakeup capability | | Wakeup capability |
| Power-on/down reset (POR/PDR) | Y | Y | Y | Y | Y | Y | Y | Y |
| High Speed Internal (HSI) | O | O | -- | -- | (2) | | -- | |
| High Speed External (HSE) | O | O | O | O | -- | | -- | |
| Low Speed Internal (LSI) | O | O | O | O | O | | O | |
| Low Speed External (LSE) | O | O | O | O | O | | O | |
| Multi-Speed Internal (MSI) | O | O | Y | Y | -- | | -- | |
| Inter-Connect Controller | Y | Y | Y | Y | Y | | -- | |
| RTC | O | O | O | O | O | O | O | |
| RTC Tamper | O | O | O | O | O | O | O | O |
| Auto WakeUp (AWU) | O | O | O | O | O | O | O | O |
| USART | O | O | O | O | O(3) | O | -- | |
| LPUART | O | O | O | O | O(3) | O | -- | |
| SPI | O | O | O | O | -- | | -- | |
| I2C | O | O | O | O | O(4) | O | -- | |
| ADC | O | O | -- | -- | -- | | -- | |
| Temperature sensor | O | O | O | O | O | | -- | |
| Comparators | O | O | O | O | O | O | -- | |
| 16-bit timers | O | O | O | O | -- | | -- | |
| LPTIMER | O | O | O | O | O | O | | |
| IWDG | O | O | O | O | O | O | O | O |
| WWDG | O | O | O | O | -- | | -- | |
| SysTick Timer | O | O | O | O | | | -- | |
| GPIOs | O | O | O | O | O | O | | 2 pins |
| Wakeup time to Run mode | 0 µs | 0.36 µs | 3 µs | 32 µs | 3.5 µs | | 65 µs | |

The Cortex-M0+ processor closely integrates a configurable Nested Vectored Interrupt Controller (NVIC), to deliver industry-leading interrupt performance. The NVIC:

- includes a Non-Maskable Interrupt (NMI)
- provides zero jitter interrupt option
- provides four interrupt priority levels

The tight integration of the processor core and NVIC provides fast execution of Interrupt Service Routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to abandon and restart load-multiple and store-multiple operations. Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that include a deep sleep function that enables the entire device to enter rapidly stop or standby mode.

This hardware block provides flexible interrupt management features with minimal interrupt latency.

## 3.4 Reset and supply management

### 3.4.1 Power supply schemes

- $V_{DD}$ = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through $V_{DD}$ pins.
- $V_{SSA}$, $V_{DDA}$ = 1.65 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL. $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively.

### 3.4.2 Power supply supervisor

The devices feature an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

Two versions are available:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the $V_{DD}$ threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the VDD min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the power ramp-up should guarantee that 1.65 V is reached on $V_{DD}$ at least 1 ms after it exits the POR area.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage ($V_{REFINT}$) in Stop mode. The device remains in reset mode when $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$ or $V_{BOR}$, without the need for any external reset circuit.

Table 11. STM32L031x4/6 I²C implementation

| I2C features(1) | I2C1 |
|---|---|
| 7-bit addressing mode | X |
| 10-bit addressing mode | X |
| Standard mode (up to 100 kbit/s) | X |
| Fast mode (up to 400 kbit/s) | X |
| Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s) | X(2) |
| Independent clock | X |
| SMBus | X |
| Wakeup from STOP | X |

1. X = supported.
2. See *Table 15: Pin definitions on page 38* for the list of I/Os that feature Fast Mode Plus capability

### 3.15.2 Universal synchronous/asynchronous receiver transmitter (USART)

The USART interface (USART2) is able to communicate at speeds of up to 4 Mbit/s.

it provides hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART2 also supports Smartcard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock that allows to wake up the MCU from Stop mode using baudrates up to 42 Kbaud.

USART2 interface can be served by the DMA controller.

*Table 12* for the supported modes and features of USART interface.

Table 12. USART implementation

| USART modes/features(1) | USART2 |
|---|---|
| Hardware flow control for modem | X |
| Continuous communication using DMA | X |
| Multiprocessor communication | X |
| Synchronous mode(2) | X |
| Smartcard mode | X |
| Single-wire half-duplex communication | X |
| IrDA SIR ENDEC block | X |
| LIN mode | X |
| Dual clock domain and wakeup from Stop mode | X |
| Receiver timeout interrupt | X |
| Modbus communication | X |
| Auto baud rate detection (4 modes) | X |
| Driver Enable | X |

1. X = supported.

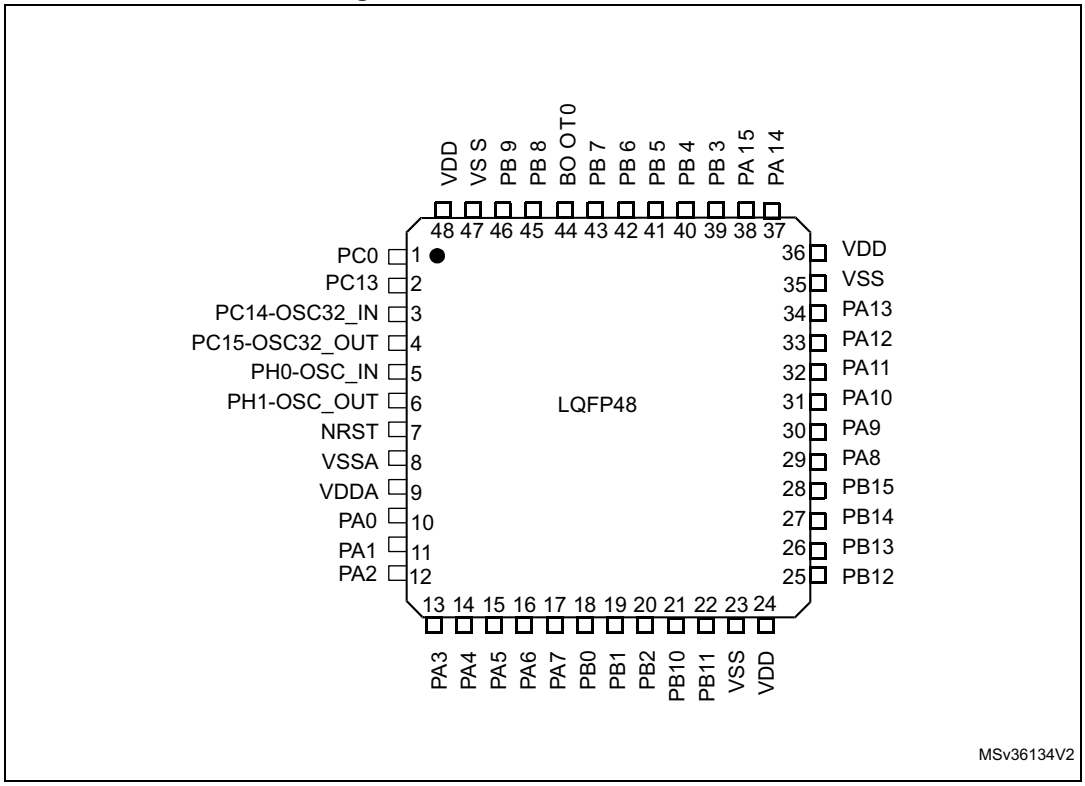
the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

## 3.17 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

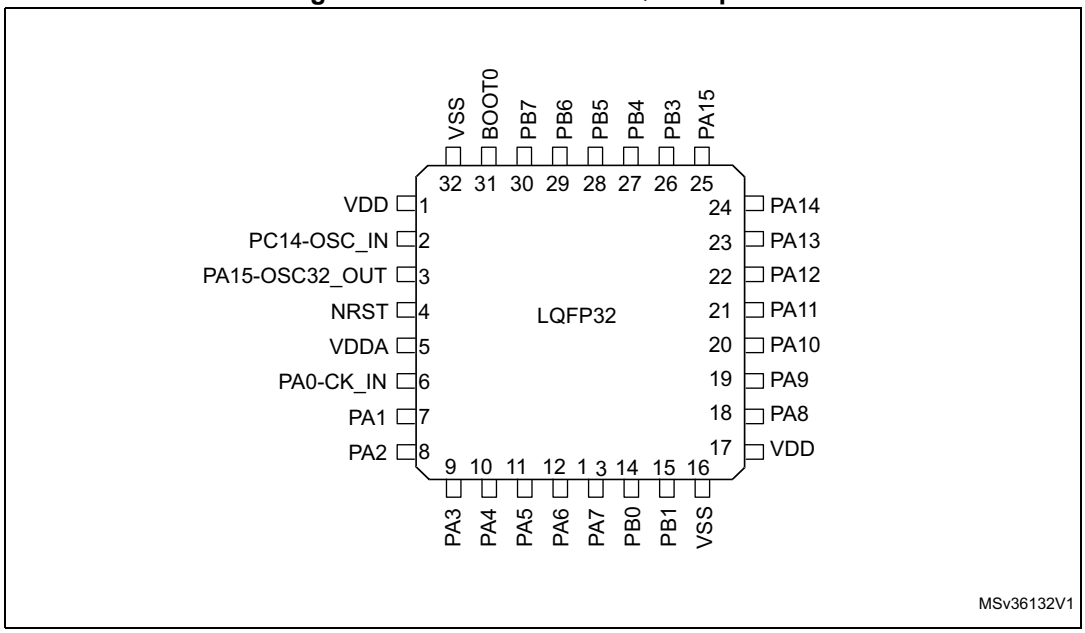
# 4 Pin descriptions

**Figure 3. STM32L031x4/6 LQFP48**



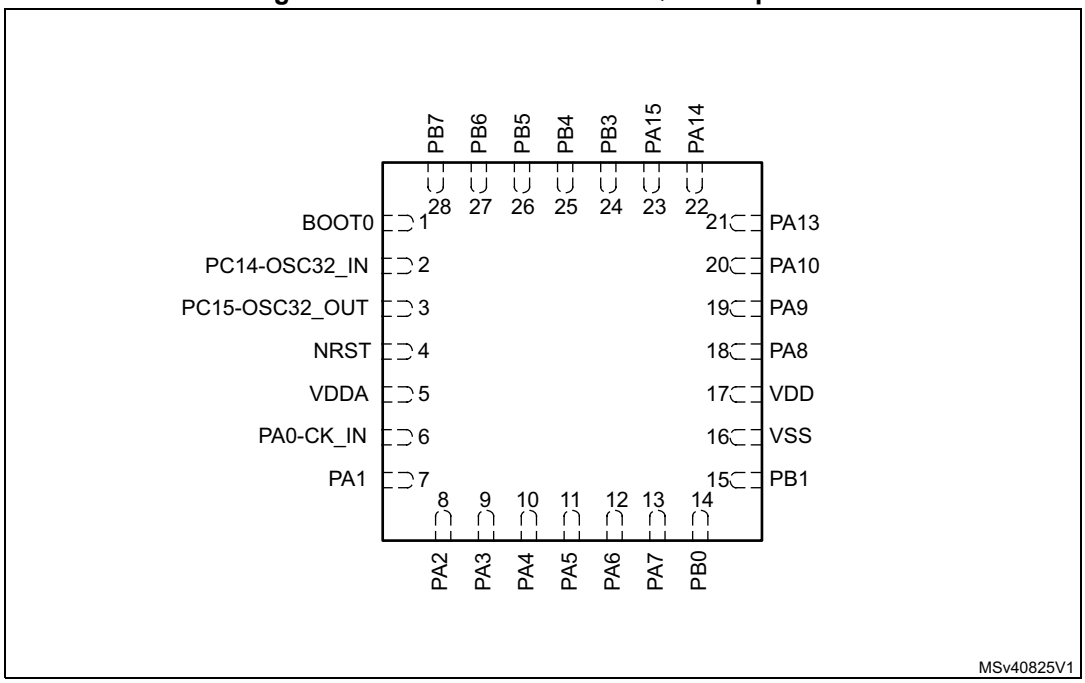

1. The above figure shows the package bump view.

**Figure 4. STM32L031x4/6 LQFP32 pinout**



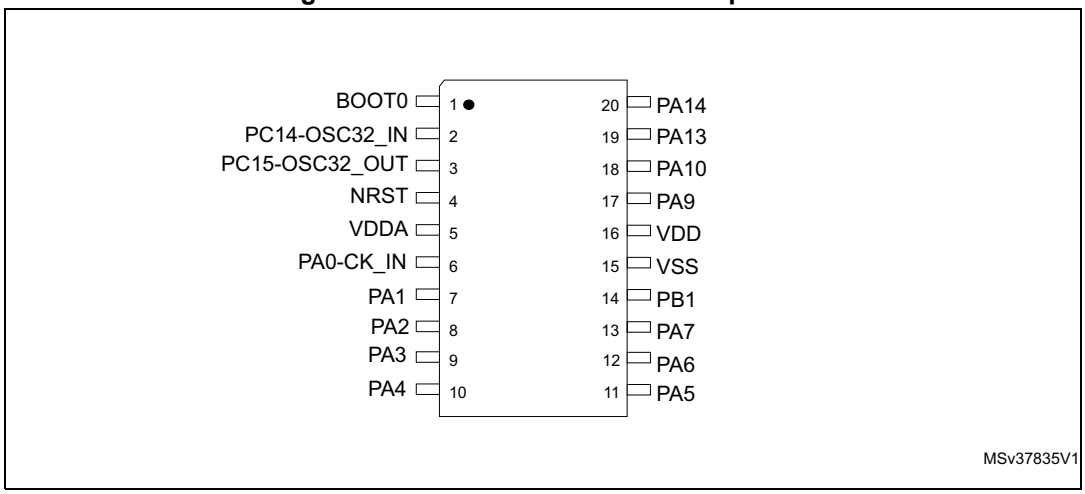

1. The above figure shows the package top view.

**Figure 7. STM32L031GxUxS UFQFPN28 pinout**




1. The above figure shows the package top view.
2. This pinout applies only to STM32L031GxUxS part number.

**Figure 8. STM32L031x4/6 TSSOP20 pinout**




1. The above figure shows the package top view.

Table 15. Pin definitions (continued)

| Pin Number | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Note | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TSSOP20 | WLCSP25[1] | UFQFPN28 | UFQFPN28 (STM32L031GxUxS only) | LQFP32 | UFQFPN32[2] | LQFP48 | | | | | | |
| 1 | A5 | 27 | 1 | 31 | 31 | 44 | BOOT0 | I | - | - | - | - |
| - | - | - | - | - | 32 | 45 | PB8 | I/O | FTf | - | I2C1_SCL | - |
| - | - | - | - | - | - | 46 | PB9 | I/O | FTf | - | EVENTOUT, I2C1_SDA | - |
| - | - | 28 | - | 32 | - | 47 | VSS | S | - | - | - | - |
| - | - | 1 | - | 1 | 1 | 48 | VDD | S | - | - | - | - |

1. WLCSP25 package is in development. Its ballout is subject to change.
2. VSS pins are connected to the exposed pad (see *Figure 40: UFQFPN32, 5 x 5 mm, 32-pin package outline*).

**Table 20. General operating conditions (continued)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $T_A$ | Temperature range | Maximum power dissipation (range 6) | –40 | 85 | °C |
| | | Maximum power dissipation (range 7) | –40 | 105 | |
| | | Maximum power dissipation (range 3) | –40 | 125 | |
| $T_J$ | Junction temperature range (range 6) | -40 °C ≤ $T_A$ ≤ 85 ° | –40 | 105 | |
| | Junction temperature range (range 7) | -40 °C ≤ $T_A$ ≤ 105 °C | –40 | 125 | |
| | Junction temperature range (range 3) | -40 °C ≤ $T_A$ ≤ 125 °C | –40 | 130 | |

1. It is recommended to power $V_{DD}$ and $V_{DDA}$ from the same source. A maximum difference of 300 mV between $V_{DD}$ and $V_{DDA}$ can be tolerated during power-up and normal operation.
2. To sustain a voltage higher than $V_{DD}$+0.3V, the internal pull-up/pull-down resistors must be disabled.
3. If $T_A$ is lower, higher $P_D$ values are allowed as long as $T_J$ does not exceed $T_J$ max (see *Table 19: Thermal characteristics on page 50*).

## 6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in *Table 20*.

**Table 21. Embedded reset and power control block characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{VDD}$(1) | $V_{DD}$ rise time rate | BOR detector enabled | 0 | - | ∞ | µs/V |
| | | BOR detector disabled | 0 | - | 1000 | |
| | $V_{DD}$ fall time rate | BOR detector enabled | 20 | - | ∞ | |
| | | BOR detector disabled | 0 | - | 1000 | |
| $T_{RSTTEMPO}$(1) | Reset temporization | $V_{DD}$ rising, BOR enabled | - | 2 | 3.3 | ms |
| | | $V_{DD}$ rising, BOR disabled(2) | 0.4 | 0.7 | 1.6 | |
| $V_{POR/PDR}$ | Power on/power down reset threshold | Falling edge | 1 | 1.5 | 1.65 | V |
| | | Rising edge | 1.3 | 1.5 | 1.65 | |
| $V_{BOR0}$ | Brown-out reset threshold 0 | Falling edge | 1.67 | 1.7 | 1.74 | |
| | | Rising edge | 1.69 | 1.76 | 1.8 | |
| $V_{BOR1}$ | Brown-out reset threshold 1 | Falling edge | 1.87 | 1.93 | 1.97 | |
| | | Rising edge | 1.96 | 2.03 | 2.07 | |
| $V_{BOR2}$ | Brown-out reset threshold 2 | Falling edge | 2.22 | 2.30 | 2.35 | |
| | | Rising edge | 2.31 | 2.41 | 2.44 | |

**Figure 15. $I_{DD}$ vs $V_{DD}$, at $T_A$= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSE = 16 MHz, 1WS**

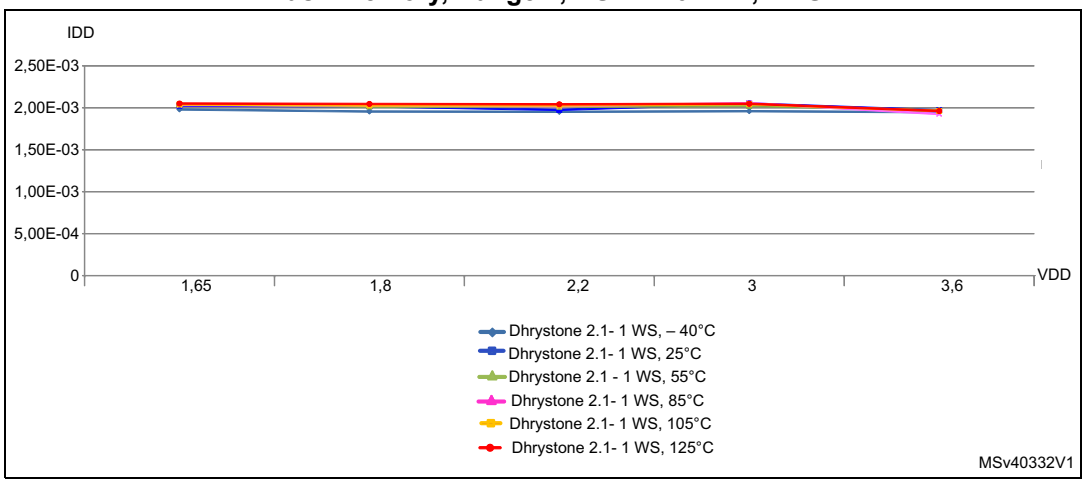



**Figure 16. $I_{DD}$ vs $V_{DD}$, at $T_A$= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSI16, 1WS**

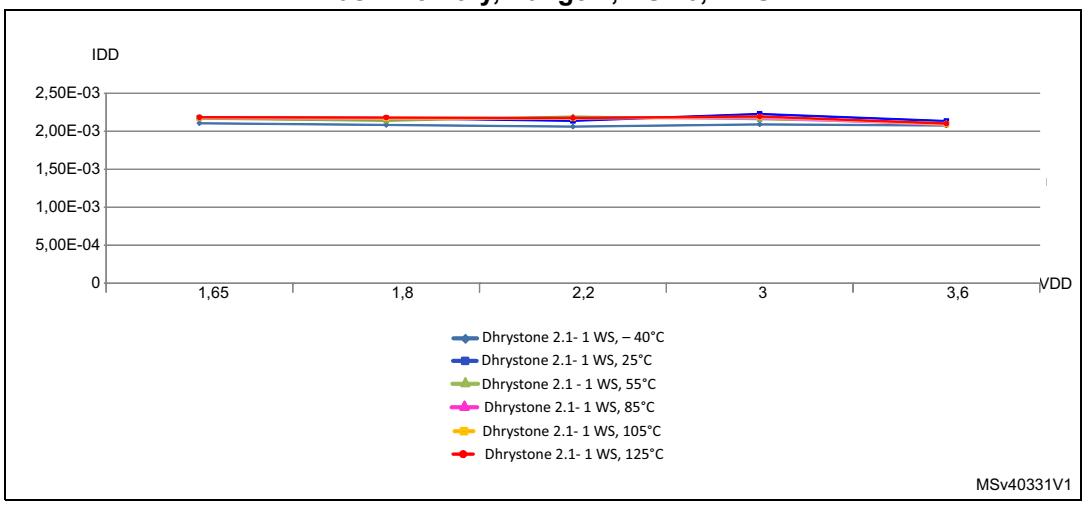


**Table 32. Typical and maximum current consumptions in Standby mode**

| Symbol | Parameter | Conditions | | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ (Standby) | Supply current in Standby mode | Independent watchdog and LSI enabled | $T_A$ = -40 °C to 25 °C | 0.8 | 1.6 | µA |
| | | | $T_A$ = 55 °C | 0.9 | 1.8 | |
| | | | $T_A$= 85 °C | 1 | 2 | |
| | | | $T_A$ = 105 °C | 1.3 | 3 | |
| | | | $T_A$ = 125 °C | 2.15 | 7 | |
| | | Independent watchdog and LSI off | $T_A$ = -40 °C to 25 °C | 0.255 | 0.6 | |
| | | | $T_A$ = 55 °C | 0.28 | 0.7 | |
| | | | $T_A$ = 85 °C | 0.405 | 1 | |
| | | | $T_A$ = 105 °C | 0.7 | 1.7 | |
| | | | $T_A$ = 125 °C | 1.55 | 5 | |

1. Guaranteed by characterization results at 125 °C, unless otherwise specified

**Table 33. Average current consumption during wakeup**

| Symbol | parameter | System frequency | Current consumption during wakeup | Unit |
|---|---|---|---|---|
| $I_{DD}$ (WU from Stop) | Supply current during wakeup from Stop mode | HSI | 1 | mA |
| | | HSI/4 | 0.7 | |
| | | MSI 4,2 MHz | 0.7 | |
| | | MSI 1,05 MHz | 0.4 | |
| | | MSI 65 KHz | 0.1 | |
| $I_{DD}$ (Reset) | Reset pin pulled down | - | 0.21 | |
| $I_{DD}$ (Power Up) | BOR on | - | 0.23 | |
| $I_{DD}$ (WU from StandBy) | With Fast wakeup set | MSI 2,1 MHz | 0.5 | |
| | With Fast wakeup disabled | MSI 2,1 MHz | 0.12 | |

**Table 35. Peripheral current consumption in Stop and Standby mode(1)**

| Symbol | Peripheral | Typical consumption, $T_A$ = 25 °C | | Unit |
|---|---|---|---|---|
| | | $V_{DD}$=1.8 V | $V_{DD}$=3.0 V | |
| $I_{DD(PVD / BOR)}$ | - | 0.7 | 1.2 | µA |
| $I_{REFINT}$ | - | 1.3 | 1.4 | |
| - | LSE Low drive(2) | 0.1 | 0.1 | |
| - | LSI | 0.27 | 0.31 | |
| - | IWDG | 0.2 | 0.3 | |
| - | LPTIM1, Input 100 Hz | 0.01 | 0.01 | |
| - | LPTIM1, Input 1 MHz | 6 | 6 | |
| - | LPUART1 | 0.2 | 0.2 | |
| - | RTC (LSE in Bypass mode) | 0.2 | 0.2 | |

1. LPTIM, LPUART peripherals can operate in Stop mode but not in Standby mode
2. LSE Low drive consumption is the difference between an external clock on OSC32_IN and a quartz between OSC32_IN and OSC32_OUT.-

### 6.3.5 Wakeup time from low-power mode

The wakeup times given in the following table are measured with the MSI or HSI16 RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is either the MSI oscillator in the range configured before entering Stop mode, the HSI16 or HSI16/4.
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 20*.

**Table 43. MSI oscillator characteristics (continued)**

| Symbol | Parameter | Condition | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{SU(MSI)}$ | MSI oscillator startup time | MSI range 0 | 30 | - | µs |
| | | MSI range 1 | 20 | - | |
| | | MSI range 2 | 15 | - | |
| | | MSI range 3 | 10 | - | |
| | | MSI range 4 | 6 | - | |
| | | MSI range 5 | 5 | - | |
| | | MSI range 6, Voltage range 1 and 2 | 3.5 | - | |
| | | MSI range 6, Voltage range 3 | 5 | - | |
| $t_{STAB(MSI)}$(2) | MSI oscillator stabilization time | MSI range 0 | - | 40 | µs |
| | | MSI range 1 | - | 20 | |
| | | MSI range 2 | - | 10 | |
| | | MSI range 3 | - | 4 | |
| | | MSI range 4 | - | 2.5 | |
| | | MSI range 5 | - | 2 | |
| | | MSI range 6, Voltage range 1 and 2 | - | 2 | |
| | | MSI range 3, Voltage range 3 | - | 3 | |
| $f_{OVER(MSI)}$ | MSI oscillator frequency overshoot | Any range to range 5 | - | 4 | MHz |
| | | Any range to range 6 | - | 6 | |

1. This is a deviation for an individual part, once the initial frequency has been measured.
2. Guaranteed by characterization results.

### 6.3.8 PLL characteristics

The parameters given in *Table 44* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 20*.

**Table 44. PLL characteristics**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max(1) | |
| $f_{PLL\_IN}$ | PLL input clock(2) | 2 | - | 24 | MHz |
| | PLL input clock duty cycle | 45 | - | 55 | % |

**Table 44. PLL characteristics (continued)**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max(1) | |
| $f_{PLL\_OUT}$ | PLL output clock | 2 | - | 32 | MHz |
| $t_{LOCK}$ | PLL input = 16 MHz<br>PLL VCO = 96 MHz | - | 115 | 160 | µs |
| Jitter | Cycle-to-cycle jitter | - | | ± 600 | ps |
| $I_{DDA}$(PLL) | Current consumption on $V_{DDA}$ | - | 220 | 450 | µA |
| $I_{DD}$(PLL) | Current consumption on $V_{DD}$ | - | 120 | 150 | |

1. Guaranteed by characterization results.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by $f_{PLL\_OUT}$.

## 6.3.9 Memory characteristics

### RAM memory

**Table 45. RAM and hardware registers**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VRM | Data retention mode(1) | STOP mode (or RESET) | 1.65 | - | - | V |

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

### Flash memory and data EEPROM

**Table 46. Flash memory and data EEPROM characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage<br>Read / Write / Erase | - | 1.65 | - | 3.6 | V |
| $t_{prog}$ | Programming time for word or half-page | Erasing | - | 3.28 | 3.94 | ms |
| | | Programming | - | 3.28 | 3.94 | |
| $I_{DD}$ | Average current during the whole programming / erase operation | $T_A$ = 25 °C, $V_{DD}$ = 3.6 V | - | 500 | 700 | µA |
| | Maximum current (peak) during the whole programming / erase operation | | - | 1.5 | 2.5 | mA |

1. Guaranteed by design.

**Table 47. Flash memory and data EEPROM endurance and retention**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| | | | Min(1) | |
| $N_{CYC}$(2) | Cycling (erase / write) Program memory | $T_A$ = -40°C to 105 °C | 10 | kcycles |
| | Cycling (erase / write) EEPROM data memory | | 100 | |
| | Cycling (erase / write) Program memory | $T_A$ = -40°C to 125 °C | 0.2 | |
| | Cycling (erase / write) EEPROM data memory | | 2 | |
| $t_{RET}$(2) | Data retention (program memory) after 10 kcycles at $T_A$ = 85 °C | $T_{RET}$ = +85 °C | 30 | years |
| | Data retention (EEPROM data memory) after 100 kcycles at $T_A$ = 85 °C | | 30 | |
| | Data retention (program memory) after 10 kcycles at $T_A$ = 105 °C | $T_{RET}$ = +105 °C | 10 | |
| | Data retention (EEPROM data memory) after 100 kcycles at $T_A$ = 105 °C | | | |
| | Data retention (program memory) after 200 cycles at $T_A$ = 125 °C | $T_{RET}$ = +125 °C | | |
| | Data retention (EEPROM data memory) after 2 kcycles at $T_A$ = 125 °C | | | |

1. Guaranteed by characterization results.
2. Characterization is done according to JEDEC JESD22-A117.

**Table 61. Temperature sensor characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_L$(1) | $V_{SENSE}$ linearity with temperature | - | ±1 | ±2 | °C |
| Avg_Slope(1) | Average slope | 1.48 | 1.61 | 1.75 | mV/°C |
| $V_{130}$ | Voltage at 130°C ±5°C(2) | 640 | 670 | 700 | mV |
| $I_{DDA(TEMP)}$(3) | Current consumption | - | 3.4 | 6 | µA |
| $t_{START}$(3) | Startup time | - | - | 10 | µs |
| $T_{S\_temp}$(4)(3) | ADC sampling time when reading the temperature | 10 | - | - | |

1. Guaranteed by characterization results.
2. Measured at $V_{DD}$ = 3 V ±10 mV. V130 ADC conversion result is stored in the TS_CAL2 byte.
3. Guaranteed by design.
4. Shortest sampling time can be determined in the application by multiple iterations.

## 6.3.17 Comparators

**Table 62. Comparator 1 characteristics**

| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | 1.65 | | 3.6 | V |
| $R_{400K}$ | $R_{400K}$ value | - | - | 400 | - | kΩ |
| $R_{10K}$ | $R_{10K}$ value | - | - | 10 | - | |
| $V_{IN}$ | Comparator 1 input voltage range | - | 0.6 | - | $V_{DDA}$ | V |
| $t_{START}$ | Comparator startup time | - | - | 7 | 10 | µs |
| td | Propagation delay(2) | - | - | 3 | 10 | |
| Voffset | Comparator offset | - | - | ±3 | ±10 | mV |
| $d_{Voffset}/dt$ | Comparator offset variation in worst voltage stress conditions | $V_{DDA}$ = 3.6 V<br>$V_{IN+}$ = 0 V<br>$V_{IN-}$ = $V_{REFINT}$<br>$T_A$ = 25 °C | 0 | 1.5 | 10 | mV/1000 h |
| $I_{COMP1}$ | Current consumption(3) | - | - | 160 | 260 | nA |

1. Guaranteed by characterization.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

**Table 64. TIMx(1) characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{COUNTER}$ | 16-bit counter clock period when internal clock is selected (timer's prescaler disabled) | - | 1 | 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 32 MHz | 0.0312 | 2048 | µs |
| $t_{MAX\_COUNT}$ | Maximum possible count | - | - | 65536 × 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 32 MHz | - | 134.2 | s |

1. TIMx is used as a general term to refer to the TIM2, TIM21, and TIM22 timers.

## 6.3.19 Communications interfaces

### I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm) : with a bit rate up to 100 kbit/s
- Fast-mode (Fm) : with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+) : with a bit rate up to 1 Mbit/s.

The I²C timing requirements are guaranteed by design when the I²C peripheral is properly configured (refer to the reference manual for details). The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement (refer to *Section 6.3.13: I/O port characteristics* for the I2C I/Os characteristics).

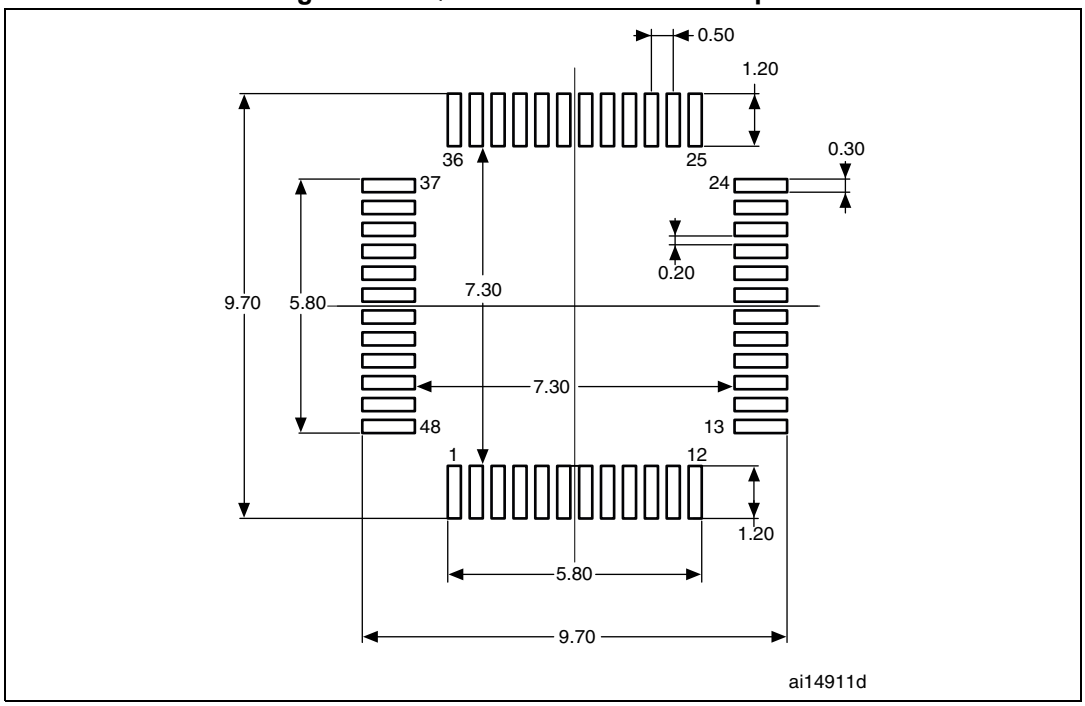
All I²C SDA and SCL I/Os embed an analog filter (see *Table 65* for the analog filter characteristics).

**Table 65. I2C analog filter characteristics(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{AF}$ | Maximum pulse width of spikes that are suppressed by the analog filter | 50(2) | 260(3) | ns |

1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

Figure 35. LQFP48 recommended footprint

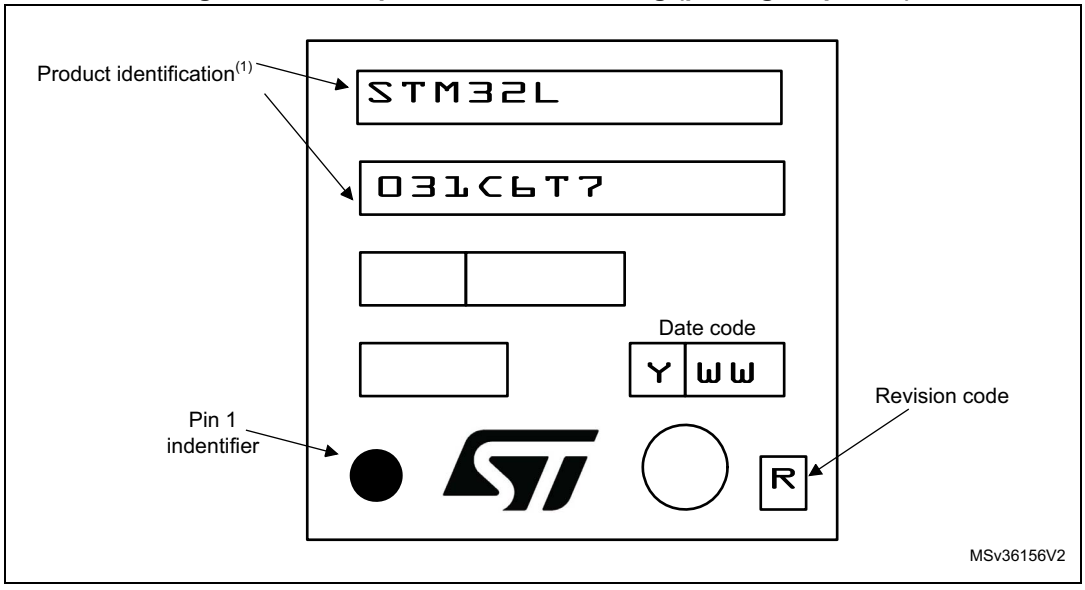



1. Dimensions are expressed in millimeters.

## LQFP48 device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

Figure 36. Example of LQFP48 marking (package top view)




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.